4

Electromigration

The power current requirements of integrated circuits are rapidly rising, as discussed in Chapter 1. The current density in on-chip power and ground lines can reach several hundred thousands of amperes per square centimeter. At these current densities, electromigration becomes significant. Electromigration is the transport of metal atoms under the force of an electron flux. The depletion and accumulation of the metal material resulting from the atomic flow can lead to the formation of extrusions (or hillocks) and voids in the metal structures. The hillocks and voids can lead to short circuit and open circuit faults [72], respectively, as shown in Fig. 4.1, degrading the reliability of an integrated circuit.

The significance of electromigration has been established early in the development of integrated circuits [73], [74]. Electromigration should be considered in the design process of an integrated circuit to ensure reliable operation over the target lifetime. Electromigration reliability and related design implications are the subject of this chapter. A more detailed discussion of the topic of electromigration can be found in the literature [75], [76].

The chapter is organized as follows. The physical mechanism of electromigration is described in Section 4.1. The role of mechanical stress in electromigration reliability is discussed in Section 4.2. The steady state conditions of electromigration damage in interconnect lines are established in Section 4.3. The dependence of electromigration reliability on the dimensions of the interconnect line is discussed in Section 4.4. The statistical distribution of the electromigration lifetime is presented in Section 4.5. Electromigration reliability under an AC current is discussed in Section 4.6. Electromigration reliability in novel interconnect

(a) (b)

Fig. 4.1. Electromigration induced circuit faults. (a) Line extrusions formed due to metal accumulation can short circuit the adjacent line. (b) The voids formed due to metal depletion increase the line resistance and can lead to an open circuit.

technologies using copper metalization and low-k dielectrics is discussed in Section 4.7. Certain approaches to designing for electromigration reliability are briefly reviewed in Section 4.8. The chapter concludes with a summary.

4.1 Physical mechanism of electromigration

Electromigration is a microscopic mass transport of metal ions through diffusion under an electrical driving force. An atomic flux under a driving force F is

$$J_{\mathrm{a}} = C_a \mu F, \tag{4.1}$$

where C_a is the atomic concentration and μ is the mobility of the atoms. From the Einstein relationship, the mobility can be expressed in terms of the atomic diffusivity D_{a} and the thermal energy kT,

$$\mu = \frac{D_{\mathrm{a}}}{kT}\,. \tag{4.2}$$

Two forces act on metal ions: an electric field force and an electron wind force. The electric field force is proportional to the electric field E and acts in the direction of the field. The electric field also accelerates the conduction electrons in the direction opposite to the electric field. The electrons transfer the momentum to the metal ions in the course of scattering, exerting the force in the direction opposite to the field E. This force is commonly referred to as the electron wind force. The electron wind force equals the force exerted by the electric field on the conduction electrons, which is proportional to the electric field intensity E.

In the metals of interest, such as aluminum and copper, the electron wind force dominates and the net force acts in the direction opposite

to the electric current. The resulting atomic flux is therefore in the direction opposite to the electric current j, as shown in Fig. 4.2. The net

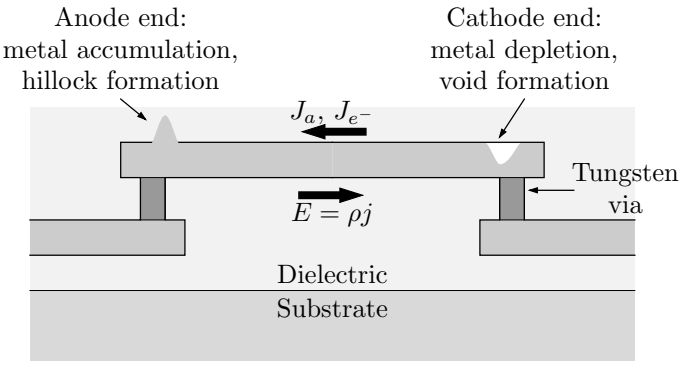

Fig. 4.2. Electromigration mass transport in an interconnect line. An electron flux J_{e^-} flowing in the opposite direction to the electric field $E = \rho j$ induces an atomic flow J_{a} in the direction of the electron flow. Diffusion barriers, such as tungsten vias, create an atomic flux divergence, leading to electromigration damage in the form of voids and hillocks.

force acting on the metal atoms is proportional to the electric field and is typically expressed as $-Z^*eE$ or $-Z^*e\rho j$, where Z^*e is the effective charge of the metal ions, j is the current density, and ρ is the resistivity of the metal. The electromigration atomic flux is therefore

$$J_{\mathrm{a}} = -C_a \frac{D_{\mathrm{a}} Z^* e \rho j}{kT}, \tag{4.3}$$

where the minus sign indicates the direction opposite to the field E. The diffusivity D_{a} has an Arrhenius dependence on temperature, $D_{\mathrm{a}} = D_0 \exp(-Q/kT)$, where Q is the activation energy of diffusion. Substituting this relationship into (4.3), the atomic flux becomes

$$J_{\mathrm{a}} = -C_a \frac{Z^* e \rho j}{kT} D_0 \exp\left(-\frac{Q}{kT}\right). \tag{4.4}$$

The material properties C_a, ρ, and Z^*e are difficult to change. The diffusion coefficient D_0 and the activation energy Q, although also material specific, vary significantly depending on the processing conditions and the resulting microstructure of the metal film. There are several paths for electromigration in interconnect lines, such as diffusion

through the lattice, along the grain boundary, and along the metal surface. Each path is characterized by the individual diffusion coefficient and activation energy. The atomic flux depends exponentially on the activation energy Q and is therefore particularly sensitive to variations in Q. The diffusion path with the lowest activation energy dominates the overall atomic flux.

The on-chip metal films are polycrystalline, consisting of individual crystals of various size. The individual crystals are commonly referred to as grains. The activation energy Q is relatively low for diffusion along the grain boundary, as low as 0.5 eV for aluminum, while the activation energy for diffusion through the lattice is the highest, up to 1.4 eV in aluminum. Diffusion along the grain boundary is the primary path of electromigration in relatively wide aluminum interconnect lines, as discussed in Section 4.4.

An atomic flux does not cause damage to on-chip metal structures where the influx of the atoms is balanced by the atom outflow. The depletion and accumulation of metal (and the associated damage) develop at those sites where the influx and outflux are not equal, *i.e.*, the flux divergence is not zero, $\nabla \cdot J_{\mathrm{a}} \neq 0$. Flux divergence can be caused by several factors, including an interface between materials with dissimilar diffusivity and resistivity, inhomogeneity in microstructure, and a temperature gradient.

Consider, for example, the current flow in an aluminum metal line segment connected to two tungsten vias at the ends, as shown in Fig. 4.2. At the current densities of interest, tungsten is not susceptible to electromigration and can be considered as an ideal barrier for the diffusion of aluminum atoms. The tungsten-aluminum interface at the anode line end, where the electric current enters the line (*i.e.*, the electron flux exits the line), prevents the outflow of the aluminum atoms from the line. The incoming atomic flux causes an accumulation of aluminum atoms. At the cathode end of the line, the tungsten-aluminum interface blocks the atomic flux from entering the line. The electron flux enters the line at this end and carries away aluminum atoms, leading to metal depletion and, potentially, formation of a void.

In a similar manner, an inhomogeneity in the microstructure can cause flux divergence. As has been discussed, grain boundaries have significantly lower activation energy, facilitating atomic flow. The electromigration atomic flux is enhanced at the locations with small grains, where the grain boundaries provide numerous paths of facilitated

diffusion. At those sites where the grain size changes abruptly, the high atomic flux in the region of the smaller grain size is mismatched with the relatively low atomic flux in the larger grain region. The atomic flux divergence leads to a material depletion or accumulation, depending upon the direction of current flow. These sites are particularly susceptible to electromigration damage [77].

4.2 Electromigration-induced mechanical stress

The depletion and accumulation of material at the sites of atomic flux divergence induce a mechanical stress gradient in the metal structures. At the sites of metal accumulation the stress is compressive, while at the sites of metal depletion the stress is tensile. The resulting stress gradient in turn induces a flux of metal atoms J_a^{stress},

$$J_a^{\text{stress}} = C_a \frac{D_{\text{a}}}{kT} \Omega \frac{\partial \sigma}{\partial l}, \tag{4.5}$$

where σ is the mechanical stress, assumed positive in tension, Ω is the atomic volume, and l is the line length. The atomic flux due to the stress gradient is opposite in direction to the electromigration atomic flux, counteracting the electromigration mass transport. This flux is therefore often referred to as an atomic backflow. The distribution of the mechanical stress and the net atomic flux are therefore interrelated. Accurate modeling of the mechanical stress is essential in predicting electromigration reliability. Mechanical stress can also have components unrelated to electromigration atomic flux, such as a difference in the thermal expansion rates of the materials.

The on-chip metal structures are encapsulated in a dielectric material, typically silicon dioxide. The stiffness of the dielectric material significantly affects the electromigration reliability. A rigid dielectric, such as silicon dioxide, limits the variation in metal volume at the sites of the metal depletion and accumulation, resulting in greater electromigration-induced mechanical stress as compared to a metal line in a less rigid environment. The greater mechanical stress induces a greater atomic flux in the direction opposite to the electromigration atomic flux, limiting the net atomic flux and the related structural damage. Rigid encapsulation therefore significantly improves the electromigration reliability of the metal interconnect.

A rigid dielectric can however lead to structural defects due to a mismatch in the thermal expansion rate of the materials. As the silicon wafer is cooled from the temperature of silicon dioxide deposition, the rigid and well adhering silicon dioxide prevents the aluminum lines from contracting according to the thermal expansion rate of aluminum. The resulting tensile stress in the aluminum lines can cause void formation [78]. This effect is exacerbated in narrow lines.

4.3 Steady state limit of electromigration damage

Under certain conditions, the stress induced atomic flux can fully compensate the atomic flux due to electromigration, preventing further damage. In this case, the atomic concentration along a metal line is stationary, $\frac{\partial C_a}{\partial t} = 0$. The net atomic flow is related to the atomic concentration by the continuity equation,

$$\frac{\partial C_a}{\partial t} = -\nabla J_{\mathrm{a}} = \frac{\partial J_{\mathrm{a}}}{\partial l} = 0. \tag{4.6}$$

The atomic flow is uniform along the line length l, $J_{\mathrm{a}}(l) = \text{const}$. In a line segment confined by diffusion barriers, the steady state atomic flux is zero. Under this condition, the diffusion due to the electrical driving force is compensated by the diffusion due to the mechanical driving force. The net atomic flux J_{a} is the sum of the electromigration and stress induced fluxes,

$$J_{\mathrm{a}} = J_{\mathrm{a}}^{\mathrm{em}} + J_{\mathrm{a}}^{\mathrm{stress}} = C_a \frac{D_{\mathrm{a}}}{kT} \left(\Omega \frac{\partial \sigma}{\partial l} - Z^* e \rho j \right). \tag{4.7}$$

The steady state condition is established where

$$\Omega \frac{\partial \sigma}{\partial l} = Z^* e \rho j. \tag{4.8}$$

High mechanical stress gradients are required to compensate the electromigration atomic flow at high current densities. The magnitude of the stress gradient depends upon the formation of voids and hillocks.

Consider a line segment of length l_0 between two sites of flux divergence, such as tungsten vias or severe microstructural irregularities. The compressive stress at the anode end should reach a certain yield stress σ_y to develop the extrusion damage [79]. Assuming a near zero stress at the cathode end of the segment, the damage critical stress

gradient is $\left(\frac{\partial\sigma}{\partial l}\right)_{\max} = \sigma_y/l_0$. Substituting this expression for the stress gradient into (4.8) yields the maximum current density,

$$j_{\max}^{\text{hillock}} = \frac{\Omega\sigma_y}{Z^*e\rho}\,\frac{1}{l_0}\,. \tag{4.9}$$

If the current density is lower than the limit determined by (4.9), the steady state condition is reached before formation of the hillocks at the anode, and the interconnect line is highly resistive to electromigration damage. Resistance to electromigration damage below a certain current threshold was first experimentally observed by Blech [80]

Void formation also causes mechanical stress that counteracts electromigration atomic flow. As the stress becomes sufficiently high to fully compensate the electromigration flow, the void stops growing and remains at the steady state size [81]. The steady state void size is well described by [82], [83]

$$\Delta l = \frac{Z^*e\rho}{2B\Omega}\,jl_0^2\,, \tag{4.10}$$

where B is the elastic modulus relating the line strain to the line stress. Equation (4.10) can be obtained from (4.8) by assuming that a void of size Δl induces a line stress $2B\frac{\Delta l}{l_0}$.

If the steady state void does not lead to a circuit failure, the electromigration lifetime of the line is practically unlimited. A formation of a void in a line does not necessarily lead to a circuit failure. Metal lines in modern semiconductor processes are covered with a thin refractory metal film, such as Ti, TiN, or $TiAl_3$, in the case of aluminum interconnect. These metal films are highly resistant to electromigration damage, providing an alternative current path in parallel to the metal core of the line. A void spanning the line width will therefore increase the resistance of the line, rather than lead to an open circuit fault. The increase in line resistance is proportional to the void size Δl. An increase in the line resistance from 10% to 20% is typically considered critical, leading to a circuit failure. A critical increase in the resistance occurs when the void size reaches a certain critical value Δl_{crit}. The current density resulting in a void of critical steady state size is determined from (4.10),

$$j_{\max}^{\text{void}} = \frac{2B\Omega}{Z^*e\rho}\,\frac{\Delta l_{\text{crit}}}{l_0^2}\,. \tag{4.11}$$

If the current density of the line is lower than $j_{\max}^{\text{void}}$, the void damage saturates at a subcritical size and the lifetime of the line becomes practically unlimited.

The critical current density as determined by (4.9) for hillock formation and (4.11) for void formation increases with shorter line length l_0. For a given current density there exists a certain critical line length l_{crit}. Lines shorter than l_{crit} are highly resistant to electromigration damage. This phenomenon is referred to as the electromigration threshold or Blech effect.

4.4 Dependence of electromigration lifetime on the line dimensions

While the electromigration reliability depends upon many parameters, as expressed by (4.4), most of these parameters cannot be varied due to material properties and manufacturing process characteristics. The parameters that can be flexibly varied at the circuit design phase are the line width, length, and current. Varying the current is often restricted by circuit performance considerations. The dependence of electromigration reliability on the line width and length are discussed in this section.

The dependence of the electromigration lifetime on the width of a line is relatively complex [84], [85], as illustrated in Fig. 4.3. In relatively wide lines, *i.e.*, where the average grain size is much smaller than the line width, the grain boundaries form a continuous diffusion path along the line length, as shown in Fig. 4.4(b). Although the grain boundary diffusion path enhances the electromigration atomic flow due to a higher diffusion coefficient along the grain boundary, the probability of abrupt microstructural inhomogeneity along the line length is small, due to a large number of grains spanning the width of the line. The probability of an atomic flux divergence in these polygranular lines is relatively low and the susceptibility of the line to electromigration damage is moderate.

As the line width approaches the average grain size, the polygranular line structure is likely to be interrupted by grains spanning the entire width of the line, disrupting the boundary diffusion path, as shown in Fig. 4.4(c). Electromigration transport in the spanning grain can occur only through the lattice or along the surface of the line. The diffusivity of these paths is significantly lower than the diffusivity of

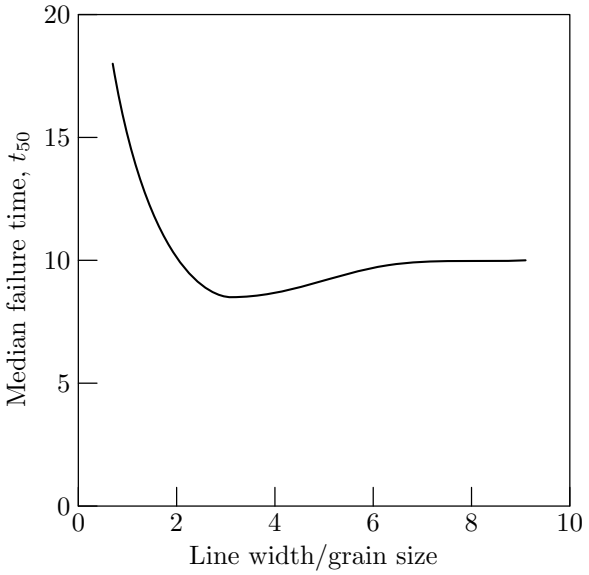

Fig. 4.3. Representative variation of the median electromigration lifetime with line width (based on data obtained from [85]).

the polycrystalline segments. The spanning grains therefore present a barrier to an atomic flux in relatively long polygranular segments of the line. The atomic flux discontinuity at the boundary of the spanning grains renders such lines more susceptible to electromigration damage, shortening the electromigration lifetime.

As the line width is reduced below the average grain size, the spanning grains dominate the line microstructure, forming the so-called "bamboo" pattern, as shown in Fig. 4.4(d). The polygranular segments become sparse and short. The shorter polygranular segments are resistant to electromigration damage, increasing the expected lifetime of the narrow lines.

The electromigration lifetime also varies with line length. Shorter lines have a longer lifetime than longer lines [84]. The longer lines are more likely to contain a significant microstructural discontinuity, such as a spanning grain in wide lines or a long polygranular segment in narrow lines. The longer lines are therefore more susceptible to electromigration damage.

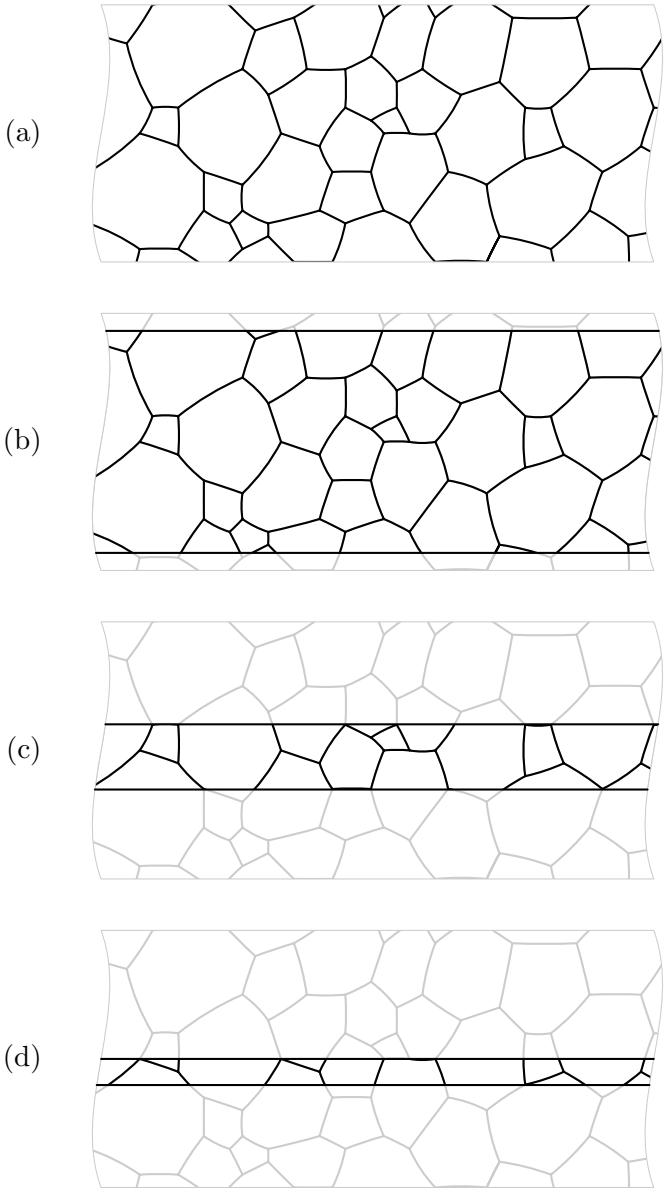

Fig. 4.4. Grain structure of interconnect lines. (a) Grain structure of an unpatterned thin metalization film. (b) The structure of the wide lines is polygranular along the entire line length. (c) In lines with a width close to the average grain size, the polygranular segments are interrupted by the grains spanning the entire line width. (d) In narrow lines, most of the grains span the entire line width, forming a "bamboo" pattern.

4.5 Statistical distribution of electromigration lifetime

Electromigration failure is a statistical process. Identically designed interconnect structures fail at different times due to variations in the microstructure. Failure times are typically described by a log-normal distribution. A variable distribution is log-normal if the distribution of the logarithm of the variable is normal. The log-normal probability density function $p(t)$ is

$$p(t) = \frac{1}{\sqrt{2\pi}\sigma t} \exp\left(-\frac{(\ln(t/t_{50}))^2}{2\sigma^2}\right). \tag{4.12}$$

The log-normal distribution is characterized by the median time to failure t_{50} and the shape factor σ. The probability density function for several values of σ are shown in Fig. 4.5.

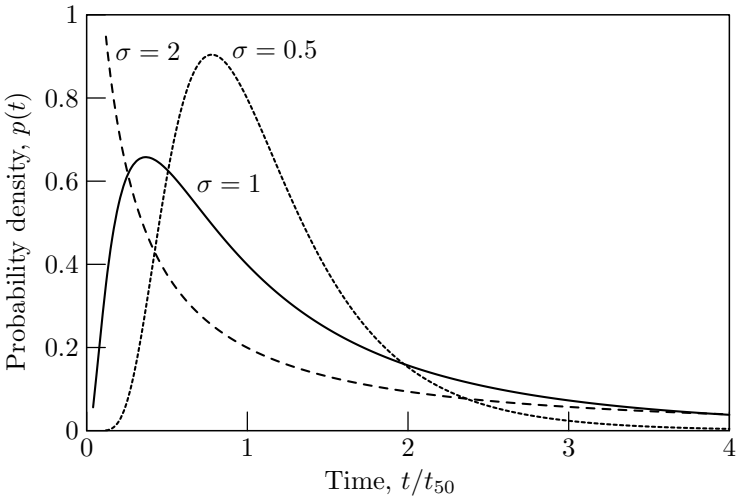

Fig. 4.5. Log-normal distribution of electromigration failures. The distribution is unimodal and is determined by the median time to failure t_{50} and the shape parameter σ.

Accelerated electromigration testing is performed to evaluate the lifetime distribution parameters for a specific manufacturing process. The interconnect structures are subjected to a current and temperature significantly greater than the target specifications to determine the statistical characteristics of the interconnect failures within a limited time period. The following relationship, first proposed by Black in

1967 [74], [86], is commonly used to estimate the median time to failure at different temperatures and current densities,

$$t_{50} = \frac{A}{j^n} \exp\left(\frac{Q}{kT}\right), \tag{4.13}$$

where A and n are empirically determined parameters. In the absence of Joule heating effects, the value of n varies from one to two, depending on the characteristics of the manufacturing process [72]. As demonstrated by models of the electromigration process, $n = 1$ corresponds to the case of void induced failures, and $n = 2$ represents the case of hillock induced failures [87].

4.6 Electromigration lifetime under AC current

On-chip interconnect lines typically carry time-varying AC current. It is necessary to determine the electromigration lifetime under AC conditions based on accelerated testing, which is typically performed under DC current.

Consider a train of current square pulses with a duty ratio $d = t_{\text{on}}/T$, as shown in Fig. 4.6, versus a DC current of the same magnitude. Assuming that a linear accumulation of the electromigration damage

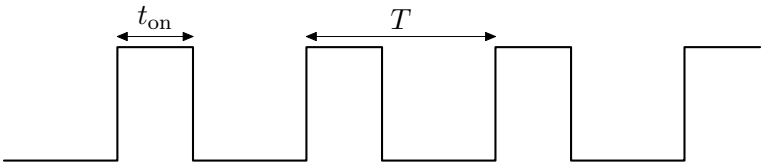

Fig. 4.6. A train of current pulses.

during the active phase t_{on} of the pulses results in the pulsed current lifetime t_{50}^{pulsed} that is $1/d$ times longer than the DC current lifetime t_{50}^{dc}, *i.e.*, $t_{50}^{\text{dc}}/t_{50}^{\text{pulsed}} = d$. This estimate is, however, overly conservative, suggesting a certain degree of electromigration damage repair during the quiet phase of the pulses. This "self-healing" effect significantly extends the lifetime of a line. Experimental studies [88], [89], [90] have demonstrated that, in the absence of Joule heating effects, the pulsed current lifetime is determined by the average current j_{avg},

$$t_{50}^{\text{pulsed}} = \frac{A}{j_{\text{avg}}^{n}} \exp\left(\frac{Q}{kT}\right). \tag{4.14}$$

As $j_{\text{avg}} = dj_{\text{dc}}$, the pulsed current lifetime is related to the DC current lifetime as $t_{50}^{\text{dc}}/t_{50}^{\text{pulsed}} = d^n$.

Electromigration reliability is greatly enhanced under bidirectional current flow. Accurate characterization of electromigration reliability becomes difficult due to the long lifetimes. Available experimental data are in agreement with the average current model, as expressed by (4.14). According to (4.14), the lifetime becomes infinitely long as the DC component of the current approaches zero. The current density these lines can carry, however, is also limited. As the magnitude of the bidirectional current becomes sufficiently high, the Joule heating becomes significant, degrading the self-healing process and, consequently, the electromigration lifetime.

Clock and data lines in integrated circuits are usually connected to a single driver. The average current in these lines is zero and the lines are typically highly resistant to electromigration failure in the absence of significant Joule heating. Power and ground lines carry a high unidirectional current. Power and ground lines are therefore particularly susceptible to electromigration damage.

4.7 Electromigration in novel interconnect technologies

Heretofore, this discussion is largely specific to standard interconnect technologies based on aluminum and silicon dioxide. Electromigration effects in these technologies have been extensively studied and are relatively well understood. Advanced interconnect technologies using novel materials, such as copper and low-k dielectrics, have been recently introduced to enhance the electrical characteristics of interconnect structures. The electromigration characteristics of these advanced interconnect processes are different as compared to aluminum based technologies, as demonstrated by early studies [91]. The electromigration characteristics of advanced interconnect technologies are currently an area of intensive study [91].

The electromigrational atomic flux in copper interconnect is significantly lower than in aluminum interconnect mainly due to the higher activation energies of the diffusion paths. The threshold effect has been observed in copper lines [92], [93], [94], with threshold current densities several times higher than in aluminum lines. Experimental results

suggest that surface diffusion and diffusion along the interface between copper and silicon nitride covering the top of the line dominate electromigration transport. The silicon nitride film serves as a diffusion barrier at the upper surface of the line. Several features of the copper interconnect structure, however, exacerbate the detrimental effects of electromigration [91].

The sides and bottom of a copper line are covered with a refractory metal film (Ta, Ti, TaN, or TiN) to prevent copper from diffusing into the dielectric. The thickness of this film is much smaller than the thickness of the film covering the aluminum interconnect. The formation of a void in a copper line therefore leads to a higher relative increase in the line resistance. Thin redundant layers can also lead to an abrupt open-circuit failure rather than a gradual increase in the line resistance [95].

The via structure in dual-damascene copper interconnect is susceptible to failure due to void formation [96]. The refractory metal film lining the bottom of the via forms a diffusion barrier between the via and the lower metal line, as shown in Fig. 4.7. The resistance of dual-damascene interconnect is particularly sensitive to void formation at the bottom of the via. The structural characteristics of the via contact are crucial to interconnect reliability [97].

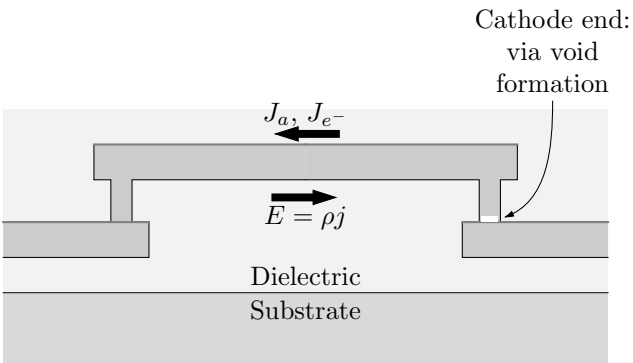

Fig. 4.7. A dual-damascene interconnect structure. A diffusion barrier is formed by the refractory metal film lining the side and lower surfaces of the lines and vias. The via bottom at the cathode end is the site of metal depletion and is susceptible to void formation. The resistance of the line is particularly sensitive to void formation at the bottom of the via.

Low-k dielectric materials decrease the distributed capacitance of the metal line and are a desirable complement to low resistivity copper metalization. Low-k dielectrics are significantly less rigid than silicon dioxide. Metal depletion and accumulation therefore result in a smaller mechanical stress, decreasing stress-induced backflow and electromigration reliability [98], [99], [100]. Low-k dielectrics also have a lower thermal conduction coefficient, exacerbating detrimental Joule heating effects.

The dominant failure mechanisms of advanced copper interconnect are therefore different than in aluminum based technologies. A statistical distribution of failure times is also more complex and cannot be described by a unimodal probability density distribution [96], [101].

The accumulated experience in understanding the electromigration characteristics of aluminum based interconnect structures therefore has limited applicability to novel interconnect technologies. Further investigation is required to ensure high yield and reliability of circuits with advanced interconnect technologies.

4.8 Designing for electromigration reliability

The electromigration reliability of integrated circuits has traditionally been ensured by requiring the average current density of each interconnect line to be below a predetermined design rule specified threshold. The cross-sectional dimensions of on-chip interconnect decrease with technology scaling, while the current increases. Simply limiting the line current density by a design rule threshold becomes increasingly restrictive under these conditions.

To ensure a target reliability, the current density threshold is selected under the implicit assumption that the current density threshold is reached with a certain number of interconnect lines. If the number of lines with a critical current density is fewer than the assumed estimate, the design rule is overly conservative. Alternatively, if the number of critical lines is larger than the estimate, the design rule does not guarantee the target reliability characteristics.

The "one size fits all" threshold approach can be replaced with a more flexible statistical electromigration budgeting methodology [102]. If the failure probability of the i^{th} line is estimated as $p_i(t)$ based on the line dimensions and average current, the probability that none of the lines in a circuit fails at time t is $\prod_i (1 - p_i(t))$. The failure probability

of the overall system $P(t)$ is therefore

$$P(t) = 1 - \prod_i (1 - p_i(t)). \tag{4.15}$$

A system with a few lines carrying current exceeding the threshold design rule [and therefore exhibiting a relatively high failure probability $p(t)$] can be as reliable as a system with a larger number of lines carrying current at the threshold level.

This statistical approach permits individual budgeting of the line failure probabilities $p_i(t)$, while maintaining the target reliability of the overall system $P(t)$. This flexibility supports more efficient use of interconnect resources, particularly in congested areas, reducing circuit area.

4.9 Summary

The electromigration reliability of integrated circuits has been discussed in this chapter. The primary conclusions of the chapter are the following.

- Electromigration damage develops near the sites of atomic flux divergence, such as vias and microstructural discontinuities
- Electromigration reliability depends upon the mechanical properties of the interconnect structures
- Electromigration reliability of short lines is greatly enhanced due to stress gradient induced backflow, which compensates the electromigration atomic flow
- Power and ground lines are particularly susceptible to electromigration damage as these lines carry a unidirectional current