16

Decoupling Capacitors for Multi-Voltage Power Distribution Systems

Power dissipation has become a critical design issue in high performance microprocessors as well as battery powered and wireless electronics, multimedia and digital signal processors, and high speed networking. The most effective way to reduce power consumption is to lower the supply voltage. Reducing the supply voltage, however, increases the circuit delay [295], [297], [330]. The increased delay can be compensated by changing the critical paths with behavioral transformations such as parallelization or pipelining [331]. The resulting circuit consumes less power while satisfying global throughput constraints at the cost of increased circuit area.

Recently, the use of multiple on-chip supply voltages has become common practice [310]. This strategy has the advantage of permitting modules along the critical paths to operate with the highest available voltage level (in order to satisfy target timing constraints) while permitting modules along the non-critical paths to use a lower voltage (thereby reducing the energy consumption). A multi-voltage scheme lowers the speed of those circuits operating at a lower power supply voltage without affecting the overall frequency, thereby reducing power without decreasing the system frequency. In this manner, the energy consumption is decreased without affecting circuit speed. This scheme results in a smaller area as compared to parallel architectures. The problem of using multiple supply voltages for reducing the power requirements has been investigated in the area of high level synthesis for low power [306], [327]. While it is possible to provide many supply voltages, in practice such a scenario is expensive. Practically, the availability of a small number of voltage supplies (two or three) is reasonable, as discussed in Chapter 14.

The design of the power distribution system has become an increasingly difficult challenge in modern CMOS circuits [28]. As CMOS technologies are scaled, the power supply voltage is lowered. As clock rates rise and more functions are integrated on-chip, the power consumed has greatly increased. Assuming that only a small per cent of the power supply voltage (about 10%) is permitted as ripple voltage (noise), a target impedance for an example power distribution system is [107]

$$Z_{\text{target}} = \frac{V_{\text{dd}} \times \zeta}{I} = \frac{1.8 \text{ volts} \times 10\%}{100 \text{ ampers}} \approx 0.002 \text{ ohms}, \tag{16.1}$$

where V_{dd} is the power supply voltage, ζ is the allowed ripple voltage, and I is the current. With general scaling theory [286], the current I is increasing and the power supply voltage is decreasing. The impedance of a power distribution system should therefore be decreased to satisfy power noise constraints. The target impedance of a power distribution system is falling at an alarming rate, a factor of five per computer generation [332]. The target impedance must be satisfied not only at DC, but also at all frequencies where current transients exist [134]. Several major components of a power delivery system are used to satisfy a target impedance over a broad frequency range. A voltage regulator module is effective up to about 1 kHz. Bulk capacitors supply current and maintain a low power distribution system impedance from 1 kHz to 1 MHz. High frequency ceramic capacitors maintain the power distribution system impedance from 1 MHz to several hundred MHz. On-chip decoupling capacitors can be effective above 100 MHz.

By introducing a second power supply, the power supplies are coupled through a decoupling capacitor effectively placed between the two power supply networks. Assuming a power delivery system with dual power supplies and only a small per cent of the power supply voltage is permitted as ripple voltage (noise), the following inequality for the magnitude of a voltage transfer function K_V should be satisfied,

$$|K_V| \leq \frac{\chi V_{\text{dd1}}}{V_{\text{dd2}}}, \tag{16.2}$$

where V_{dd1} is a lower voltage power supply, χ is the allowed ripple voltage on a lower voltage power supply, and V_{dd2} is a higher voltage power supply. Since the higher voltage power supply is applied to the high speed paths, as for example a clock distribution network, V_{dd2} can be noisy. To guarantee that noise from the higher voltage supply

does not affect the quiet power supply, (16.2) should be satisfied. For typical values of the power supply voltages and allowed ripple voltage for a CMOS 0.18 μm technology, $|K_V|$ is chosen to be less than or equal to 0.1 to effectively decouple a noisy power supply from a quiet power supply.

The design of a power distribution system with multiple supply voltages is the primary focus of this chapter. The influence of a second supply voltage on a system of decoupling capacitors is investigated. Noise coupling among multiple power distribution systems is also discussed in this chapter. A criterion for producing an overshoot-free voltage response is determined. It is shown that to satisfy a target specification in order to decouple multiple power supplies, it is necessary to maintain the magnitude of the voltage transfer function below 0.1. In certain cases, it is difficult to satisfy this criterion over the entire range of operating frequencies. In such a scenario, the frequency range of an overshoot-free voltage response can be traded off with the magnitude of the response [26]. Case studies are also presented in the chapter to quantitatively illustrate this methodology for designing a system of decoupling capacitors.

The chapter is organized as follows. The impedance of a power distribution system with multiple supply voltages is described in Section 16.1. A case study of the dependence of the impedance on the power distribution system parameters is presented in Section 16.2. The voltage transfer function of a power distribution system with multiple supply voltages is discussed in Section 16.3. Case studies examining the dependence of the magnitude of the voltage transfer function on the parameters of the power distribution system are illustrated in Section 16.4. Some specific conclusions are summarized in Section 16.5.

16.1 Impedance of a power distribution system

The impedance of a power distribution network is an important issue in modern high performance ICs such as microprocessors. The impedance should be maintained below a target level to guarantee the power and signal integrity of a system, as described in Chapter 5. The impedance of a power distribution system with multiple power supplies is described in Section 16.1.1. The antiresonance of capacitors connected in parallel is addressed in Section 16.1.2. The dependence of the impedance on the power distribution system is investigated in Section 16.1.3.

16.1.1 Impedance of a power distribution system

A model of the impedance of a power distribution system with two supply voltages is shown in Fig. 16.1. The impedance seen from the load of the power supply V_{dd1} is illustrated. The model of the impedance is applicable for the load of the power supply V_{dd2} if Z_1 is substituted for Z_2. The impedance of the power distribution system shown in Fig. 16.1 can be modeled as

$$Z = \frac{Z_1 Z_{12} + Z_1 Z_2}{Z_1 + Z_{12} + Z_2}. \tag{16.3}$$

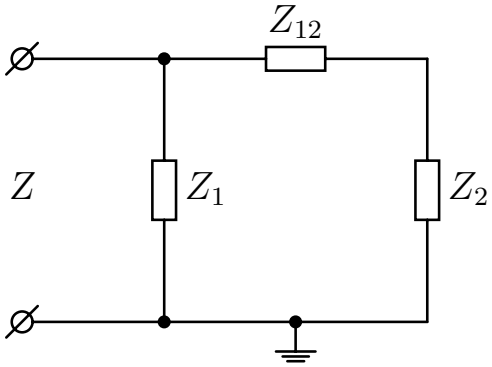


Fig. 16.1. Impedance of power distribution system with two supply voltages seen from the load of the power supply V_{dd1}.

Decoupling capacitors have traditionally been modeled as a series *RLC* network [132]. A schematic representation of a power distribution network with two supply voltages and the decoupling capacitors represented by *RLC* series networks is shown in Fig. 16.2.

In this case, the impedance of the power distribution network is

$$Z = \frac{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s}, \tag{16.4}$$

where

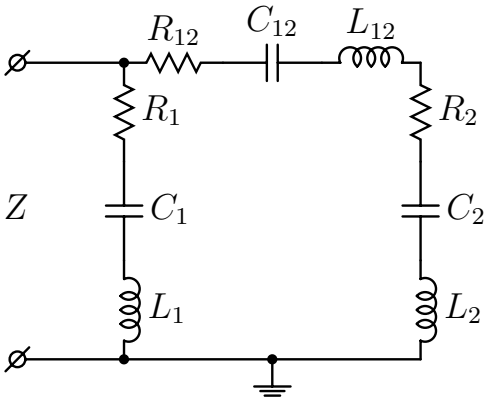


Fig. 16.2. Impedance of power distribution system with two supply voltages and the decoupling capacitors represented as series RLC networks.

$$a_4 = L_1(L_{12} + L_2), \tag{16.5}$$

$$a_3 = R_1L_{12} + R_{12}L_1 + R_1L_2 + R_2L_1, \tag{16.6}$$

$$a_2 = R_1R_{12} + R_1R_2 + \frac{L_1}{C_{12}} + \frac{L_{12}}{C_1} + \frac{L_1}{C_2} + \frac{L_2}{C_1}, \tag{16.7}$$

$$a_1 = \frac{R_1}{C_2} + \frac{R_2}{C_1} + \frac{R_1}{C_{12}} + \frac{R_{12}}{C_1}, \tag{16.8}$$

$$a_0 = \frac{C_{12} + C_2}{C_1C_{12}C_2}, \tag{16.9}$$

$$b_3 = L_1 + L_{12} + L_2, \tag{16.10}$$

$$b_2 = R_1 + R_{12} + R_2, \tag{16.11}$$

$$b_1 = \frac{1}{C_1} + \frac{1}{C_{12}} + \frac{1}{C_2}, \tag{16.12}$$

and $s = j\omega$ is a complex frequency.

The frequency dependence of the closed form expression for the impedance of a power distribution system with dual power supply voltages is illustrated in Fig. 16.3. The minimum power distribution system impedance is limited by the ESR of the decoupling capacitors. For on-chip applications, the ESR includes the parasitic resistance of the decoupling capacitor and the resistance of the power distribution network connecting a decoupling capacitor to a load. The resistance of the on-chip power distribution network is greater than the parasitic resistance of the on-chip decoupling capacitors. For on-chip applications, therefore, the ESR is represented by the resistance of the power

delivery system. Conversely, for printed circuit board applications, the resistance of the decoupling capacitors dominates the resistance of the power delivery system. In this case, therefore, the ESR is primarily the resistance of the decoupling capacitors. In order to achieve a target impedance as described by (16.1), multiple decoupling capacitors are placed at different levels of the power grid hierarchy [107].

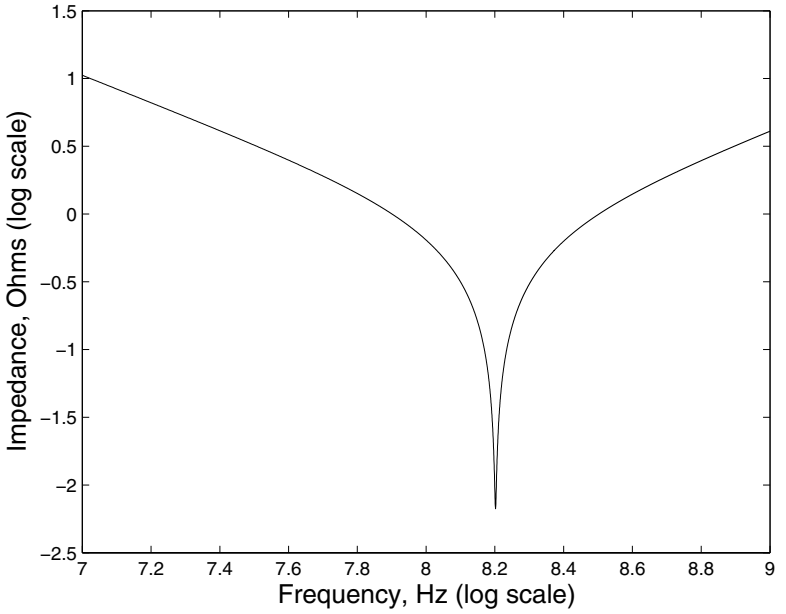


Fig. 16.3. Frequency dependence of the impedance of a power distribution system with dual supply voltages, $R_1 = R_{12} = R_2 = 10\,\mathrm{m\Omega}$, $C_1 = C_{12} = C_2 = 1\,\mathrm{nF}$, and $L_1 = L_{12} = L_2 = 1\,\mathrm{nH}$. Since all of the parameters of a power distribution system are identical, the system behaves as a single capacitor with one minimum at the resonant frequency. The minimum power distribution system impedance is limited by the ESR of the decoupling capacitors.

As described in [109], the ESR of the decoupling capacitors does not change the location of the poles and zeros of the power distribution system impedance, only the damping factor of the RLC system formed by the decoupling capacitor is affected. Representing a decoupling capacitor with a series LC network, the impedance of the power distribution system with dual power supply voltages is

$$Z = \frac{a_4 s^4 + a_2 s^2 + a_0}{b_3 s^3 + b_1 s}, \tag{16.13}$$

where

$$a_4 = L_1(L_{12} + L_2), \tag{16.14}$$

$$a_2 = \frac{L_1}{C_{12}} + \frac{L_{12}}{C_1} + \frac{L_1}{C_2} + \frac{L_2}{C_1}, \tag{16.15}$$

$$a_0 = \frac{C_{12} + C_2}{C_1 C_{12} C_2}, \tag{16.16}$$

$$b_3 = L_1 + L_{12} + L_2, \tag{16.17}$$

$$b_1 = \frac{1}{C_1} + \frac{1}{C_{12}} + \frac{1}{C_2}. \tag{16.18}$$

16.1.2 Antiresonance of parallel capacitors

To maintain the impedance of a power distribution system below a specified level, multiple decoupling capacitors are placed in parallel at different levels of the power grid hierarchy. The ESR affects the quality factor of the *RLC* system by acting as a damping element. The influence of the ESR on the impedance is therefore ignored. If all of the parameters of the circuit shown in Fig. 16.2 are equal, the impedance of the power distribution system can be described as a series *RLC* circuit. Expression (16.13) has four zeros and three poles. Two zeros are located at the same frequency as the pole when all of the parameters of the circuit are equal. The pole is therefore canceled for this special case and the circuit behaves as a series *RLC* circuit with one resonant frequency.

If the parameters of the power distribution system are not equal, the zeros of (16.13) are not paired. In this case, the pole is not canceled by a zero. For instance, in the case of two capacitors connected in parallel as shown in Fig. 16.4, in the frequency range from f_1 to f_2, the impedance of the capacitor C_1 has become inductive whereas the impedance of the capacitor C_2 remains capacitive. In this case, an *LC* tank will produce a peak at a resonant frequency located between f_1 and f_2. Such a phenomenon is called *antiresonance* [107] and is described in greater detail in Chapter 6.

The location of the antiresonant spike depends on the ratio of the ESL of the decoupling capacitors. Depending upon the parasitic inductance, the peak impedance caused by the decoupling capacitor is shifted to a different frequency, as shown in Fig. 16.4. For instance, if

the parasitic inductance of C_1 is greater than the parasitic inductance of C_2, the antiresonance will appear at a frequency ranging from f_1 to f_2, *i.e.*, before the self-resonant frequency f_2 of the capacitor C_2. If the parasitic inductance of C_1 is lower than the parasitic inductance of C_2, the antiresonance will appear at a frequency ranging from f_2 to f_3, *i.e.*, after the self-resonant frequency of the capacitor C_2. The ESL of the decoupling capacitors, therefore, determines the frequency (location) of the antiresonant spike of the system [27].

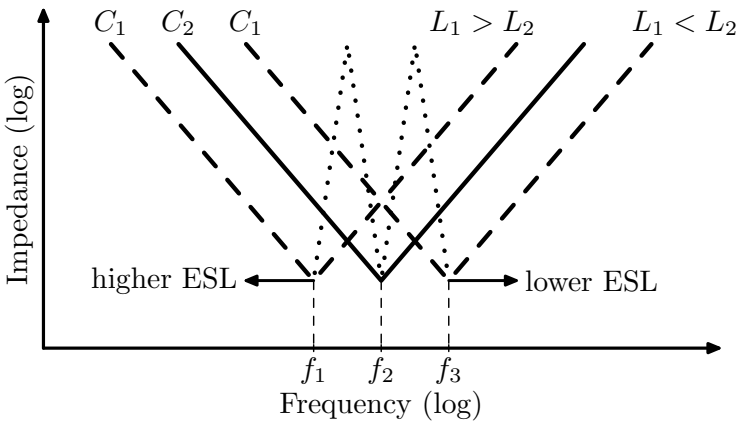


Fig. 16.4. Antiresonance of the two capacitors connected in parallel, $C_2 = C_1$. Two antiresonant spikes appear between frequencies f_1 and f_2 and f_2 and f_3 (dotted lines).

16.1.3 Dependence of impedance on power distribution system parameters

In practical applications, a capacitor C_{12} placed between V_{dd1} and V_{dd2} exists either as a parasitic capacitance or as a decoupling capacitor. Intuitively, from Fig. 16.2, by decreasing the impedance Z_{12} (increasing C_{12}), the greater part of Z_2 is connected in parallel with Z_1, reducing the impedance of the power distribution system as seen from the load of the power supply V_{dd1}. The value of a parasitic capacitance is typically much smaller than a decoupling capacitor such as C_1 and C_2. The decoupling capacitor C_{12} can be chosen to be equal to or greater

than C_1 and C_2. Depending upon the placement of the decoupling capacitors, ESL can vary from 50 nH at the power supply to almost negligible values on-chip. The ESL includes both the parasitic inductance of the decoupling capacitors and the inductance of the power delivery system. For on-chip applications, the inductance of the decoupling capacitors is much smaller than the inductance of the power distribution network and can be ignored. At the board level, however, the parasitic inductance of the decoupling capacitors dominates the overall inductance of a power delivery system. For these reasons, the model depicted in Fig. 16.2 is applicable to any hierarchical level of a power distribution system from the circuit board to on-chip.

Assuming $C_1 = C_2$, if $C_{12} > C_1$, an antiresonance spike occurs at a lower frequency than the resonance frequency of an RLC series circuit. If $C_{12} < C_1$, the antiresonance spike occurs at a higher frequency than the resonance frequency of an RLC series circuit. This phenomenon is illustrated in Fig 16.5.

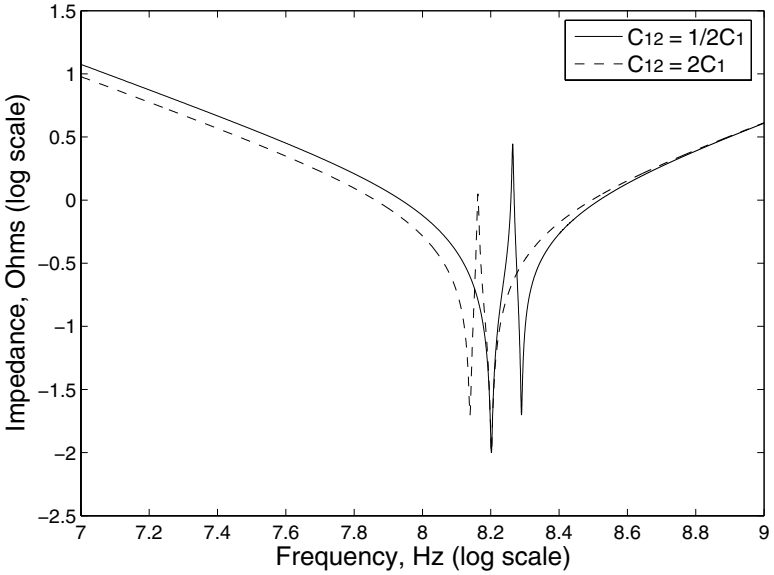


Fig. 16.5. Antiresonance of a power distribution system with dual power supply voltages, $R_1 = R_{12} = R_2 = 10\,\text{m}\Omega$, $C_1 = C_2 = 1\,\text{nF}$, and $L_1 = L_{12} = L_2 = 1\,\text{nH}$. Depending upon the ratio of C_{12} to C_1, the antiresonance appears before or after the resonant frequency of the system (the impedance minimum).

Antiresonance is highly undesirable because at a particular frequency, the impedance of a power distribution network can become unacceptably high. To cancel the antiresonance at a given frequency, a smaller decoupling capacitor is placed in parallel, shifting the antiresonance spike to a higher frequency. This procedure is repeated until the antiresonance spike appears at a frequency out of range of the operating frequencies of the system, as shown in Fig. 16.6.

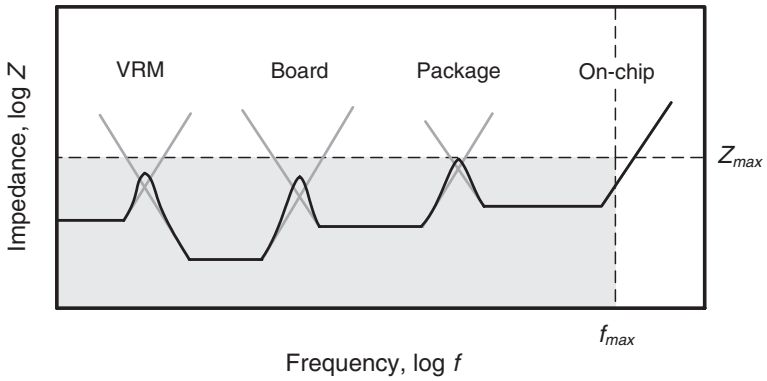


Fig. 16.6. Impedance of the power distribution system as a function of frequency. Decoupling capacitors are placed at different hierarchical levels to shift an antiresonant spike above the maximum operating frequency of the system.

Another technique for shifting the antiresonance spike to a higher frequency is to decrease the ESL of the decoupling capacitor. The dependence of the impedance of a power distribution system on the ESL is discussed below.

To determine the location of the antiresonant spikes, the roots of the denominator of (16.13) are evaluated. One pole is located at $\omega = 0$. Two other poles are located at frequencies,

$$\omega = \pm\sqrt{\frac{C_2 + C_1C_2/C_{12} + C_1}{C_1C_2(L_1 + L_{12} + L_2)}}. \tag{16.19}$$

To shift the poles to a higher frequency, the ESL of the decoupling capacitors must be decreased. If the ESL of the decoupling capacitors is close to zero, the impedance of a power delivery network will

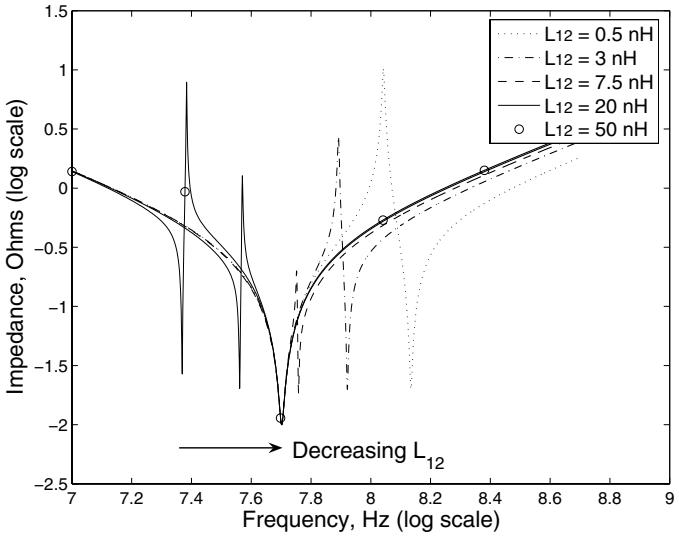
not produce overshoots over a wide range of operating frequencies. Expression (16.19) shows that by minimizing the decoupling capacitor C_{12} between the two supply voltages, the operating frequency of the overshoot-free impedance of a power delivery network can be increased.

The dependence of the power distribution system impedance on the ESL of C_{12} is shown in Fig. 16.7(a). Note the strong dependence of the antiresonant frequency on the ESL of the decoupling capacitor located between V_{dd1} and V_{dd2}. As discussed above, the location of the antiresonant spike is determined by the ESL ratio of the decoupling capacitors. The magnitude of the antiresonance spike is determined by the total ESL of C_1, C_{12}, and C_2, as shown in Fig. 16.7(b).

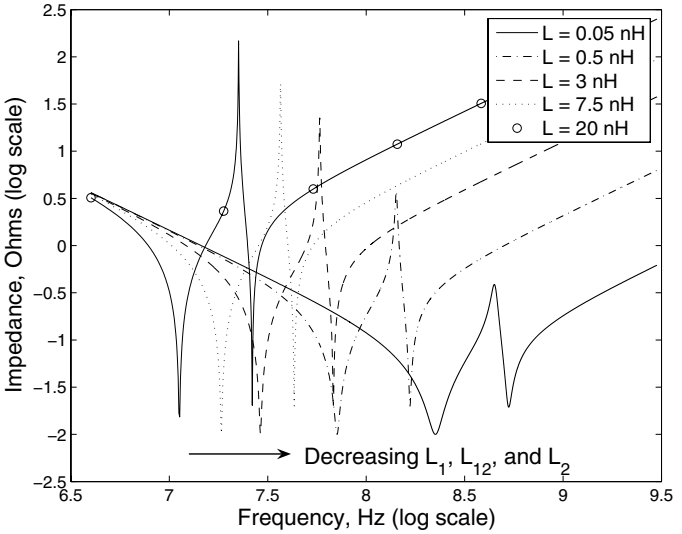
By lowering the system inductance, the quality factor is decreased. The peaks become wider in frequency and lower in magnitude. The amplitude of the antiresonant spikes can be decreased by lowering the ESL of all of the decoupling capacitors within the power distribution system. As shown in Fig. 16.7(b), decreasing the parasitic inductance of all of the decoupling capacitors of the system reduces the peak magnitude. When the parasitic inductance of C_{12} is similar in magnitude to the other decoupling capacitors, from (16.4), the poles and zeros do not cancel, affecting the behavior of the circuit. The zero at the resonant frequency of a system (the minimum value of the impedance) decreases the antiresonant spike. The closer the location of an antiresonant spike is to the resonant frequency of a system, the greater the influence of a zero on the antiresonance behavior. From a circuits perspective, the more similar the ESL of each capacitor, the smaller the amplitude of the antiresonant spike. Decreasing the inductance of the decoupling capacitors has the same effect as increasing the resistance. Increasing the parasitic resistance of a decoupling capacitor is limited by the target impedance of the power distribution system. Decreasing the inductance of a power distribution system is highly desirable and, if properly designed, the inductance of a power distribution system can be significantly reduced [70].

16.2 Case study of the impedance of a power distribution system

The dependence of the impedance on the power distribution system parameters is described in this section to quantitatively illustrate the concepts presented in Section 16.1. An on-chip power distribution



(a) $R_1 = R_{12} = R_2 = 10\,\mathrm{m\Omega}$, $C_1 = C_2 = 10\,\mathrm{nF}$, $C_{12} = 1\,\mathrm{nF}$, and $L_1 = L_2 = 1\,\mathrm{nH}$.



(b) $R_1 = R_{12} = R_2 = 10\,\mathrm{m\Omega}$, $C_1 = C_2 = 10\,\mathrm{nF}$, $C_{12} = 1\,\mathrm{nF}$, and $L_1 = L_{12} = L_2 = L$.

Fig. 16.7. Dependence of a dual V_{dd} power distribution system impedance on frequency for different ESL of the decoupling capacitors. The ESL of capacitors C_1, C_{12}, and C_2 is represented by L_1, L_{12}, and L_2, respectively.

system is assumed in this example. The total budgeted on-chip decoupling capacitance is distributed among the low voltage power supply ($C_1 = 10\,\text{nF}$), high voltage power supply ($C_2 = 100\,\text{nF}$), and the capacitance placed between the two power supplies ($C_{12} = 1\,\text{nF}$). The ESR and ESL of the power distribution network are chosen to be equal to 0.1 ohms and 1 nH, respectively. The target impedance is 0.4 ohms.

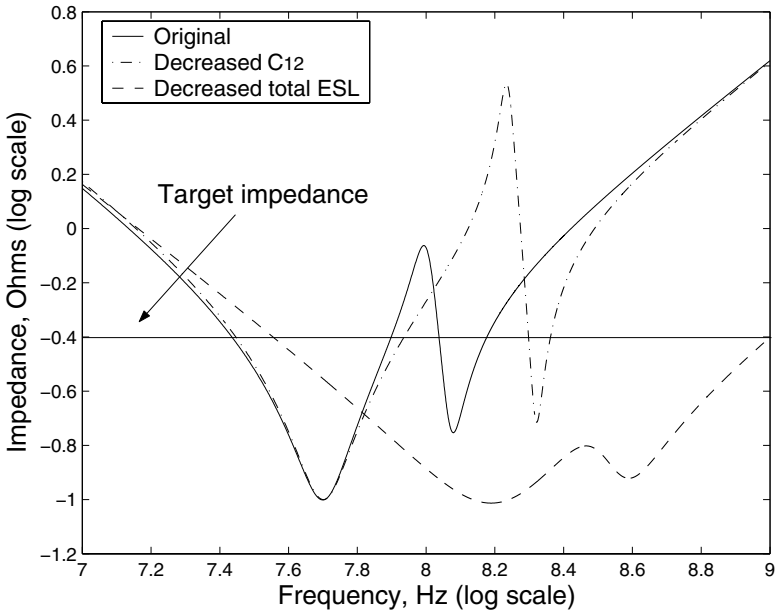


Fig. 16.8. The impedance of a power distribution system with dual power supply voltages as a function of frequency, $R_1 = R_{12} = R_2 = 100\,\text{m}\Omega$, $C_1 = C_2 = 10\,\text{nF}$, $C_{12} = 1\,\text{nF}$, and $L_1 = L_{12} = L_2 = 1\,\text{nH}$. The impedance of the example power distribution network produces an antiresonant spike with a magnitude greater than the target impedance (the solid line). The antiresonant spike is shifted to a higher frequency with a larger magnitude by decreasing C_{12} to 0.3 nF (the dashed-dotted line). By decreasing the total ESL of the system, the impedance can be maintained below the target impedance over a wide frequency range, from approximately 40 MHz to 1 GHZ (the dashed line).

For typical values of an example power distribution system, an antiresonant spike is produced at approximately 100 MHz with a magnitude greater than the target impedance, as shown in Fig. 16.8. According to (16.19), to shift the antiresonant spike to a higher frequency, the capacitor C_{12} should be decreased. As C_{12} is decreased to 0.3 nF,

Table 16.1. Case study of the impedance of a power distribution system

Tradeoff Scenario	Power Distribution System	Minimum frequency	Maximum frequency	Frequency range Δf
I	Original	4 kHz	35.48 kHz	31.48 kHz
	Decreased C_{12}	4 kHz	50.1 kHz	46.1 kHz
	Decreased L_1, L_{12}, L_2	4 kHz	1.26 MHz	1.256 MHz
II	Original	100 kHz	1 MHz	900 kHz
	Decreased C_{12}	100 kHz	2.82 MHz	2.72 MHz
	Decreased L_1, L_{12}, L_2	100 kHz	79 MHz	78.9 MHz
III	Original	560 MHz	1 GHz	440 MHz
	Decreased C_{12}	560 MHz	1.12 GHz	560 MHz
	Decreased L_1, L_{12}, L_2	890 MHz	7.9 GHz	7.01 GHz
Scenario I Board	Original system: $R_1 = R_{12} = R_2 = 1\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 50\,\mathrm{nH}$, $C_{12} = 100\,\mu\mathrm{F}$, $C_1 = C_2 = 1\,\mathrm{mF}$			
	Decreased C_{12}: $R_1 = R_{12} = R_2 = 1\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 50\,\mathrm{nH}$, $C_{12} = 20\,\mu\mathrm{F}$, $C_1 = C_2 = 1\,\mathrm{mF}$			
	Decreased L_1, L_{12}, L_2: $R_1 = R_{12} = R_2 = 1\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 5\,\mathrm{nH}$, $C_{12} = 100\,\mu\mathrm{F}$, $C_1 = C_2 = 1\,\mathrm{mF}$			
Scenario II Package	Original system: $R_1 = R_{12} = R_2 = 1\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 1\,\mathrm{nH}$, $C_{12} = 3\,\mu\mathrm{F}$, $C_1 = C_2 = 50\,\mu\mathrm{F}$			
	Decreased C_{12}: $R_1 = R_{12} = R_2 = 1\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 1\,\mathrm{nH}$, $C_{12} = 1\,\mu\mathrm{F}$, $C_1 = C_2 = 50\,\mu\mathrm{F}$			
	Decreased L_1, L_{12}, L_2: $R_1 = R_{12} = R_2 = 1\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 100\,\mathrm{pH}$, $C_{12} = 3\,\mu\mathrm{F}$, $C_1 = C_2 = 50\,\mu\mathrm{F}$			
Scenario III On-chip	Original system: $R_1 = R_{12} = R_2 = 10\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 10\,\mathrm{pH}$, $C_{12} = 1\,\mathrm{nF}$, $C_1 = C_2 = 4\,\mathrm{nF}$			
	Decreased C_{12}: $R_1 = R_{12} = R_2 = 10\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 10\,\mathrm{pH}$, $C_{12} = 0.3\,\mathrm{nF}$, $C_1 = C_2 = 4\,\mathrm{nF}$			
	Decreased L_1, L_{12}, L_2: $R_1 = R_{12} = R_2 = 10\,\mathrm{m\Omega}$, $L_1 = L_{12} = L_2 = 1\,\mathrm{pH}$, $C_{12} = 1\,\mathrm{nF}$, $C_1 = C_2 = 4\,\mathrm{nF}$			

the antiresonant spike appears at a higher frequency, approximately 158 MHz, and is of higher magnitude. To further decrease the impedance of a power distribution system with multiple power supply voltages, the total ESL of the decoupling capacitors should be decreased. As the total ESL of the system is decreased to 0.1 nH, the impedance of the power distribution system is below the target impedance over a wide frequency range, from approximately 40 MHz to 1 GHz. Three different tradeoff scenarios similar to the case study illustrated in Fig. 16.8 are summarized in Table 16.1. The design parameters for each scenario represent typical values of board, package, and on-chip power distribution

systems with decoupling capacitors, as shown in Fig. 16.9. The minimum and maximum frequencies denote the frequency range in which the impedance of a power delivery network seen from the load of V_{dd1} does not exceed the target level of 400 mΩ. Note that by decreasing the decoupling capacitor placed between V_{dd1} and V_{dd2}, the range of operating frequencies, where the target impedance is met, is slightly increased. Alternatively, if the total ESL of the system is lowered by an order of magnitude, the frequency range Δf is increased by significantly more than an order of magnitude (for tradeoff scenario III, Δf increases from 560 MHz to 7.01 GHz).

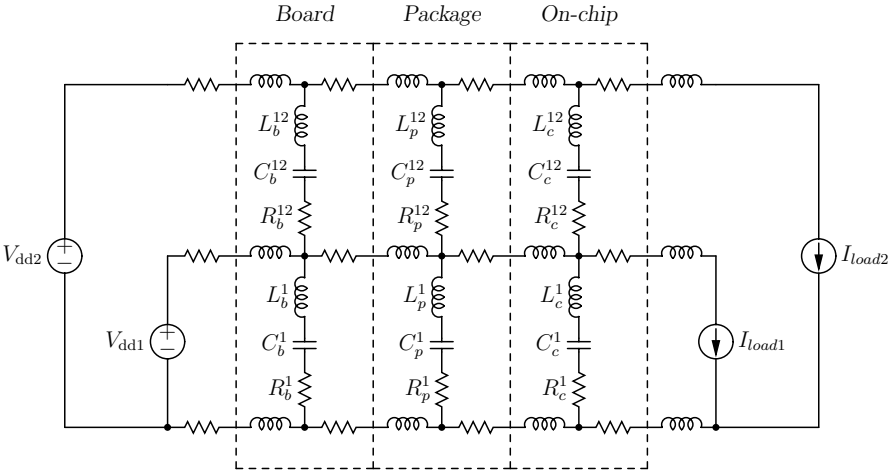


Fig. 16.9. Hierarchical model of a power distribution system with dual supply voltages and a single ground. The decoupling capacitors are represented by the series connected resistance, capacitance, and inductance. For simplicity, the decoupling capacitors placed between V_{dd2} and ground are not illustrated. Subscripts b, p, and c denote the board, package, and on-chip power delivery systems, respectively. Superscript 1 denotes the decoupling capacitors placed between V_{dd1} and ground and superscript 12 denotes the decoupling capacitors placed between V_{dd1} and V_{dd2}.

The design of a power distribution system with multiple power supply voltages is a complex task and requires many iterative steps. In general, to maintain the impedance of a power delivery system below a target level, the proper combination of design parameters needs to be determined. In on-chip applications, the ESL and C_{12} can be chosen

to satisfy specific values. At the board level, the ESR and C_{12} can be adjusted to satisfy target impedance specifications. At the package level, the ESL, C_{12}, and ESR are the primary design parameters of the system. Usually, the total decoupling capacitance is constrained by the technology and application. In certain cases, it is possible to increase the decoupling capacitance. From (16.13), note that by increasing the decoupling capacitance, the overall impedance of a power distribution system with multiple power supply voltages can be significantly decreased.

16.3 Voltage transfer function of power distribution system

Classical methodologies for designing power distribution systems with a single power supply voltage typically only consider the target output impedance of the network. By introducing a second power supply voltage, a decoupling capacitor is effectively placed between the two power supply voltages [26], [199]. The problem of noise propagating from one power supply to the other power supply is aggravated if multiple power supply voltages are employed in a power distribution system. Since multiple power supplies are naturally coupled, the voltage transfer function of a multi-voltage power distribution network should be considered [333], [334]. The voltage transfer function of a power distribution system with dual power supplies is described in Section 16.3.1. The dependence of the magnitude of the voltage transfer function on certain parameters of the power distribution system is described in subsection 16.3.2.

16.3.1 Voltage transfer function of a power distribution system

A power distribution system with two power supply voltages and the decoupling capacitors represented by an RLC series network is shown in Fig. 16.10. All of the following formulae describing this system are symmetric in terms of the power supply voltages. The ESR and ESL of the three decoupling capacitors are represented by R_1, R_{12}, R_2 and L_1, L_{12}, L_2, respectively.

The voltage transfer function K_V of a power distribution system with two power supply voltages and decoupling capacitors, represented by an RLC network, is

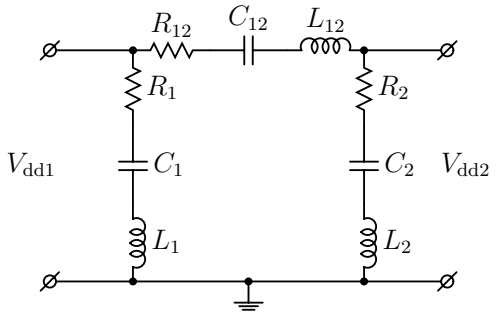


Fig. 16.10. Voltage transfer function of a power distribution network with two supply voltages and the decoupling capacitors represented as series *RLC* networks.

$$K_V = \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0}, \tag{16.20}$$

where

$$a_2 = L_2 C_2, \tag{16.21}$$
$$a_1 = R_2 C_2, \tag{16.22}$$
$$a_0 = C_{12}, \tag{16.23}$$
$$b_2 = C_{12} C_2 (L_{12} + L_2), \tag{16.24}$$
$$b_1 = C_{12} C_2 (R_{12} + R_2), \tag{16.25}$$
$$b_0 = C_{12} + C_2. \tag{16.26}$$

Rearranging, (16.20) can be written as

$$K_V = \frac{1}{\dfrac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} + 1}, \tag{16.27}$$

where

$$a_2 = L_{12} C_{12} C_2, \tag{16.28}$$
$$a_1 = R_{12} C_{12} C_2, \tag{16.29}$$
$$a_0 = C_2, \tag{16.30}$$
$$b_2 = L_2 C_{12} C_2, \tag{16.31}$$
$$b_1 = R_2 C_{12} C_2, \tag{16.32}$$
$$b_0 = C_{12}. \tag{16.33}$$

Equations (16.20) and (16.27) are valid only for non-zero frequency, *i.e.,* for $s > 0$. Note from (16.20) that if all of the parameters of a power distribution system are identical, the transfer function equals 0.5 and is independent of frequency. The dependence of the voltage transfer function on the parameters of the power distribution system is discussed below.

16.3.2 Dependence of voltage transfer function on power distribution system parameters

In power distribution systems with two supply voltages, the higher power supply is usually provided for the high speed circuits while the lower power supply is used in the non-critical paths [316], [299]. The two power supplies are often strongly coupled, implying that voltage fluctuations on one power supply propagate to the other power supply. The magnitude of the voltage transfer function should be sufficiently small in order to decouple the noisy power supply from the quiet power supply. The objective is therefore to achieve a transfer function K_V such that the two power supplies are effectively decoupled.

The dependence of the magnitude of the voltage transfer function on frequency for different values of the ESR of the power distribution network with decoupling capacitors is shown in Fig. 16.11. Reducing the ESR of a decoupling capacitor decreases the magnitude and range of the operating frequency of the transfer function. Note that to maintain $|K_V|$ below or equal to 0.5, the following inequality has to be satisfied,

$$R_2 \leq R_{12}. \tag{16.34}$$

This behavior can be explained as follows. From (16.27), to maintain $|K_V|$ below or equal to 0.5,

$$\frac{L_{12}C_{12}C_2s^2 + R_{12}C_{12}C_2s + C_2}{L_2C_{12}C_2s^2 + R_2C_{12}C_2s + C_{12}} + 1 \geq 2. \tag{16.35}$$

For equal decoupling capacitors and parasitic inductances, (16.35) leads directly to (16.34). Generally, to maintain $|K_V|$ below or equal to 0.5,

$$L_2C_2C_3s^2 + R_2C_2C_3s + C_3 \geq L_3C_2C_3s^2 + R_3C_2C_3s + C_2. \tag{16.36}$$

From (16.36), in order to maintain the magnitude of the voltage transfer function below or equal to 0.5, the ESR and ESL of the decoupling capacitors should be chosen to satisfy (16.36).

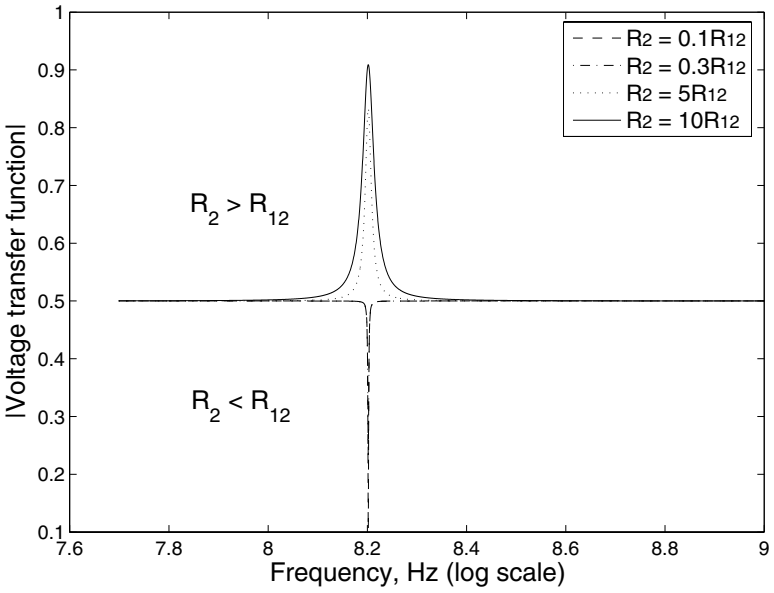


Fig. 16.11. Dependence of the magnitude of the voltage transfer function on frequency of a dual $V_{\rm dd}$ power distribution system for different values of ESR of the decoupling capacitors, $R_{12} = 10\,\mathrm{m\Omega}$, $C_{12} = C_2 = 1\,\mathrm{nF}$, and $L_{12} = L_2 = 1\,\mathrm{nH}$.

To investigate the dependence of the magnitude of the voltage transfer function on the decoupling capacitors and associated parasitic inductances, the roots of the characteristic equation, the denominator of (16.20), should be analyzed. To produce an overshoot-free response, the roots of the characteristic equation must be real, yielding

$$R_{12} + R_2 \geq 2\sqrt{\frac{(L_{12} + L_2)(C_{12} + C_2)}{C_{12}C_2}}. \tag{16.37}$$

In the case where $R_{12} = R_2 = R$, $L_{12} = L_2 = L$, and $C_{12} = C_2 = C$, (16.37) reduces to the well known formula [335],

$$R \geq 2\sqrt{\frac{L}{C}}. \tag{16.38}$$

The dependence of the magnitude of the voltage transfer function on the ESL of a power distribution system is shown in Fig. 16.12. For the power distribution system parameters listed in Fig. 16.12, the critical value of L_2 to ensure an overshoot-free response is 0.49 nH. Therefore,

in order to produce an overshoot-free response, the ESL of C_2 should be smaller than or equal to 0.49 nH.

Intuitively, if the ESL of a system is large, the system is underdamped and produces an undershoot and an overshoot. By decreasing L_2, the resulting inductance of the system in (16.37) is lowered and the system becomes more damped. As a result, the undershoots and overshoots of the voltage response are significantly smaller. If L_2 is decreased to the critical value, the system becomes overdamped, producing an overshoot-free voltage response.

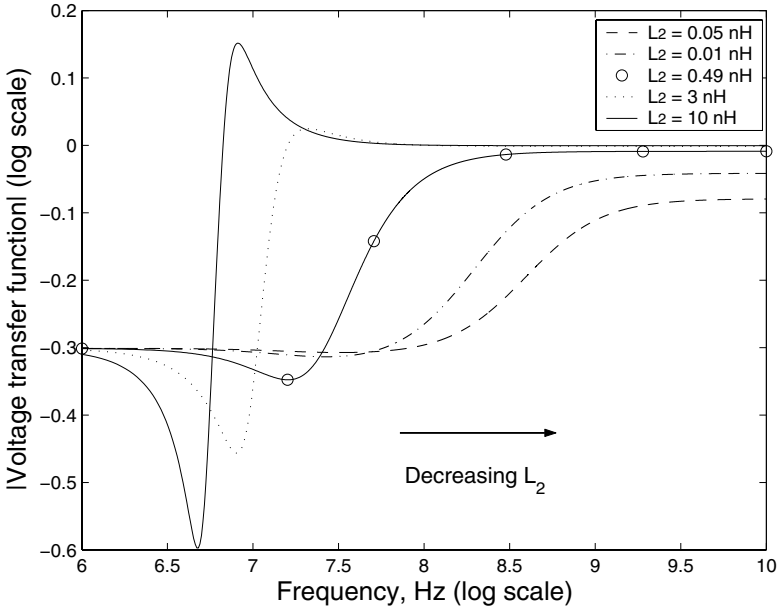


Fig. 16.12. Frequency dependence of the voltage transfer function of a dual $V_{\rm dd}$ power distribution system for different values of ESL of the decoupling capacitors, $R_{12} = R_2 = 100\,\mathrm{m\Omega}$, $C_{12} = C_2 = 100\,\mathrm{nF}$, and $L_{12} = 10\,\mathrm{pH}$.

As shown in Fig. 16.12, the magnitude of the voltage transfer function is strongly dependent on the ESL, decreasing with smaller ESL. It is highly desirable to maintain the ESL as low as possible to achieve a small overshoot-free response characterizing a dual $V_{\rm dd}$ power distribution system over a wide range of operating frequencies. Criterion (16.37) is strict and produces an overshoot-free voltage response. In most

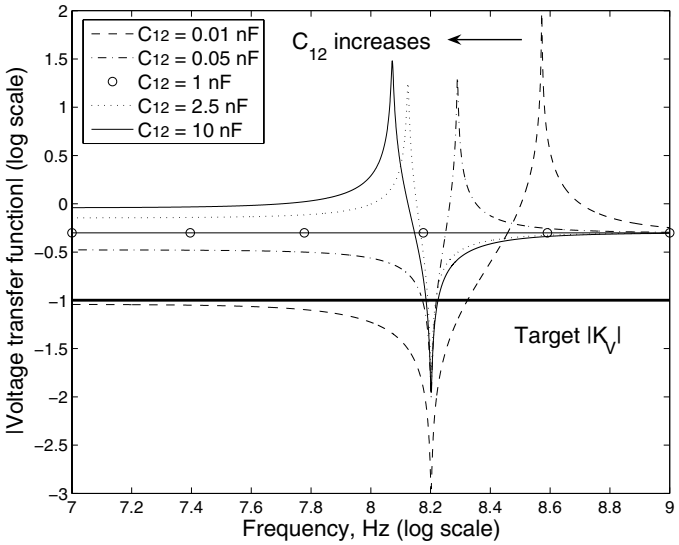
applications, if small overshoots (about 1%) are permitted, (16.37) is less strict, permitting the parameters of a power distribution network to vary over a wider range.

For the parameters listed in Fig. 16.12, the minimum overshoot-free voltage response equals 0.5. It is often necessary to maintain an extremely low magnitude voltage transfer function over a specific frequency range. This behavior can be achieved by varying one of the three design parameters (ESR, ESL or C) characterizing a decoupling capacitor while maintaining the other parameters at predefined values. In this case, for different decoupling capacitors, the magnitude of the voltage transfer function is maintained as low as 0.1 over the frequency range from DC to the self-resonant frequency of the decoupling capacitor induced by the RLC series circuit (hereafter called the *break frequency*).

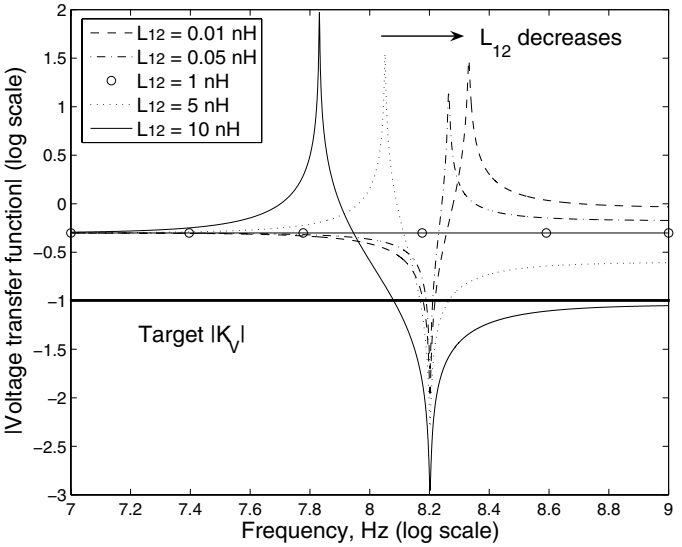
The inductance of the decoupling capacitor has an opposite effect on the magnitude of the voltage transfer function. By increasing the ESL of a dual V_{dd} power distribution system, the magnitude of the voltage transfer function can be maintained below 0.1 from the self-resonant frequency (or break frequency) of the decoupling capacitor to the maximum operating frequency. From (16.27), for frequencies smaller than the break frequency, the magnitude of the voltage transfer function is approximately $\frac{C_{12}}{C_2}$. For frequencies greater than the break frequency, the magnitude of the voltage transfer function is approximately $\frac{L_2}{L_{12}}$. To maintain $|K_V|$ below 0.1, it is difficult to satisfy (16.37), and the range of operating frequency is divided by the break frequency into two ranges. This phenomenon is illustrated in Figs. 16.13(a) and 16.13(b).

16.4 Case study of the voltage response of a power distribution system

The dependence of the voltage transfer function on the parameters of a power distribution system is described in this section to quantitatively illustrate the concepts presented in Section 16.3. An on-chip power distribution system is assumed in this example. In modern high performance ICs, the total on-chip decoupling capacitance can exceed 300 nF, occupying about 20% of the total area of an IC [204]. In this example, the on-chip decoupling capacitance is assumed to be 160 nF. The total budgeted on-chip decoupling capacitance is arbitrarily distributed among the low voltage power supply ($C_1 = 100\,\mathrm{nF}$), high voltage power



(a) $R_{12} = R_2 = 10\,\mathrm{m\Omega}$, $C_2 = 1\,\mathrm{nF}$, and $L_{12} = L_2 = 1\,\mathrm{nH}$.



(b) $R_{12} = R_2 = 10\,\mathrm{m\Omega}$, $C_{12} = C_2 = 1\,\mathrm{nF}$, and $L_2 = 1\,\mathrm{nH}$.

Fig. 16.13. Frequency dependence of the voltage transfer function of a dual V_{dd} power distribution system. The ESR and ESL of the decoupling capacitors for each power supply are represented by R_{12}, R_2 and L_{12}, L_2, respectively.

supply ($C_2 = 40\,\text{nF}$), and the capacitance placed between the two power supplies ($C_{12} = 20\,\text{nF}$). The ESR and ESL of the decoupling capacitor are chosen to be 0.1 ohms and 1 nH, respectively.

In designing a power distribution system with dual power supply voltages, it is crucial to produce an overshoot-free voltage response over the range of operating frequencies. Depending on the system parameters, it can be necessary to further decouple the power supplies, requiring the magnitude of the voltage transfer function to be decreased. In this case, it is difficult to satisfy (16.37) and the range of operating frequencies is therefore divided into two. There are two possible scenarios: 1) the two power supplies should be decoupled as much as possible from DC to the break frequency, and 2) the two power supplies should be decoupled as much as possible from the break frequency to infinity.

Note that infinite frequency is constrained by the maximum operating frequency of a specific system. Also note that the ESR, ESL, and magnitude of the decoupling capacitors can be considered as design parameters. The ESR is limited by the target impedance of the power distribution network. The ESL, however, can vary significantly. The total budgeted decoupling capacitance is distributed among C_1, C_{12}, and C_2. Note that C_{12} can range from zero (no decoupling capacitance between the two power supplies) to $C_{12} = C_{total} - C_1 - C_2$ (the maximum available decoupling capacitance between the two power supplies), where C_{total} is the total budgeted decoupling capacitance.

16.4.1 Overshoot-free magnitude of a voltage transfer function

For typical values of an example power distribution system, (16.37) is not satisfied and the response of the voltage transfer function produces an overshoot as shown in Fig. 16.14. To produce an overshoot-free voltage response, the capacitor placed between the two power supplies should be significantly increased, permitting the ESR and ESL to be varied. Increasing the ESR of the decoupling capacitors to 0.5 ohms produces an overshoot-free response. By decreasing the ESL of C_2, the overshoot-free voltage response can be further decreased, also shown in Fig. 16.14. As described in Section 16.3.2, at low frequency the magnitude of the voltage transfer function is approximately $\frac{C_{12}}{C_2}$. Note that all curves start from the same point. By increasing the ESR, the system becomes overdamped and produces an overshoot-free voltage response. Since the ESR does not change the $\frac{L_2}{L_{12}}$ ratio, the voltage response of

the overdamped system is the same as the voltage response of the initial underdamped system. Note that the dashed line and solid line converge to the same point at high frequencies, where the magnitude of the voltage transfer function is approximately $\frac{L_2}{L_{12}}$. By decreasing L_2, the total ESL of the system is lowered and the system becomes overdamped, producing an overshoot-free voltage response. Also, since the $\frac{L_2}{L_{12}}$ ratio is lowered, the magnitude of the voltage response is significantly reduced at high frequencies.

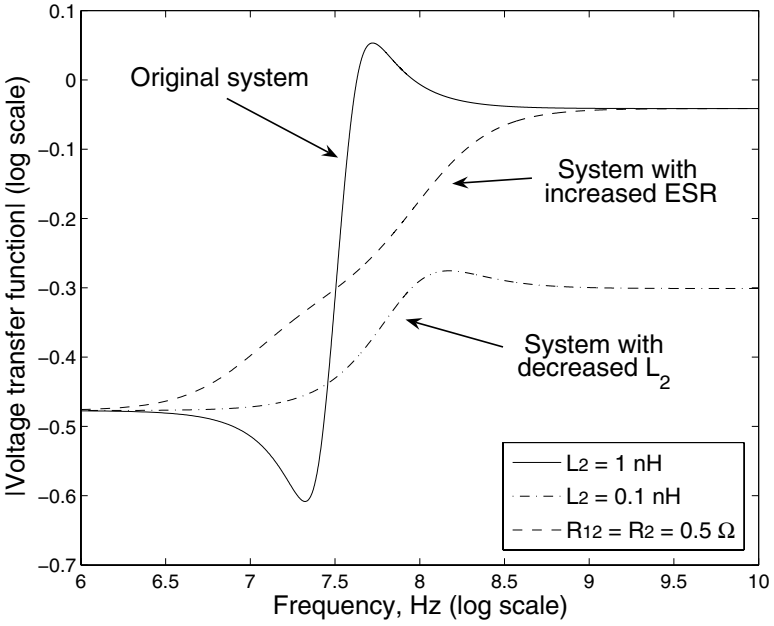


Fig. 16.14. Dependence of the magnitude of the voltage transfer function of a dual $V_{\rm dd}$ power distribution system on frequency for different values of the ESR and ESL of the decoupling capacitors, $R_{12} = R_2 = 0.1\,\Omega$, $C_{12} = 20\,\text{nF}$, $C_2 = 40\,\text{nF}$, and $L_{12} = L_2 = 1\,\text{nH}$. The initial system with $L_2 = 1\,\text{nH}$ produces an overshoot (solid line). To produce an overshoot-free voltage response, either the ESR of the system should be increased (dashed line) or the ESL should be decreased (dash-dotted line).

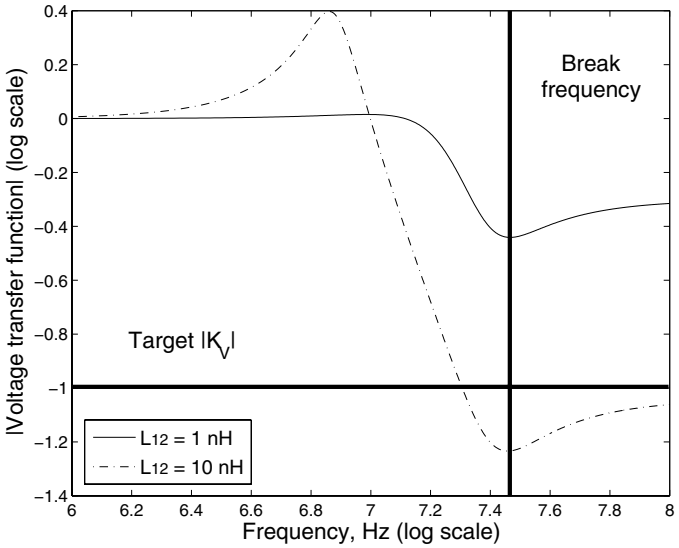
In general, a design methodology for producing an overshoot-free response of a power distribution system with dual power supply voltages is as follows. Based on the available decoupling capacitance for each power supply, the value of the decoupling capacitor placed between the

two power supplies is determined by $C_{12} = C_{total} - C_1 - C_2$. The ESR is chosen to be less than or equal to the target impedance to satisfy the impedance constraint. The critical ESL of the capacitors C_{12} and C_2 is determined from (16.37). If the parasitic inductance of C_{12} and C_2 is less than or equal to the critical ESL, the system will produce an overshoot-free voltage response and no adjustment is required. Otherwise, the total decoupling capacitance budget should be redistributed among C_1, C_{12}, and C_2 until (16.37) is satisfied. In certain cases, the total budgeted decoupling capacitance should be increased to satisfy (16.37).

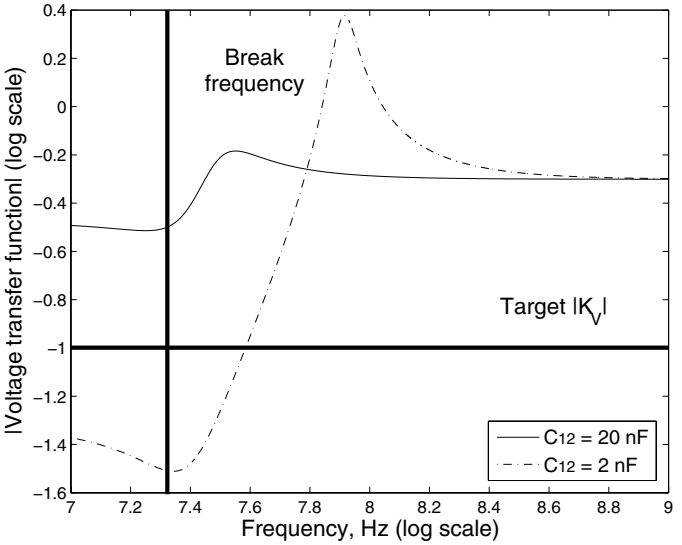
16.4.2 Tradeoff between the magnitude and frequency range

If it is necessary to further decouple the power supplies, the frequency range of the overshoot-free voltage response can be traded off with the magnitude of the voltage response, as described in Section 16.3.2. There are two ranges of interest. The magnitude of the voltage transfer function can be decreased over the frequency range from DC to the break frequency or from the break frequency to the highest operating frequency [26]. For the example power distribution system, as shown in Fig. 16.15(a), the magnitude of the voltage transfer function is overshoot-free from the break frequency to the highest operating frequency. To further decrease the magnitude of the voltage transfer function over a specified frequency range, the ESL of the decoupling capacitor placed between the two power supply voltages should be increased and C_{12} should be the maximum available decoupling capacitance, $C_{12} = C_{total} - C_1 - C_2$.

To decrease the magnitude of the voltage transfer function of a power distribution system with dual power supply voltages for frequencies less than the break frequency, the ESL of all of the decoupling capacitors and the value of C_{12} should be decreased, as shown in Fig. 16.15(b). If it is necessary to completely decouple the two power supply voltages, C_{12} should be minimized. This behavior can be explained as follows. The initial system produces an overshoot-free voltage response in the frequency range from DC to the highest operating frequency of the system. In order to satisfy the target $|K_V|$ at high frequencies, L_{12} should be increased in order to decrease the $\frac{L_2}{L_{12}}$ ratio. By increasing L_{12}, the magnitude of the voltage response falls below the target $|K_V|$ in the frequency range from the break frequency to the highest operating frequency of the system. At the same time, the



(a) $R_{12} = R_2 = 0.1\,\Omega$, $C_{12} = 20\,\text{nF}, C_2 = 40\,\text{nF}$, and $L_2 = 1\,\text{nH}$.



(b) $R_{12} = R_2 = 0.1\,\Omega$, $C_2 = 40\,\text{nF}$, and $L_{12} = L_2 = 1\,\text{nH}$.

Fig. 16.15. Magnitude of the voltage transfer function of an example dual V_{dd} power distribution system as a function of frequency. The ESR and ESL of the decoupling capacitors are represented by R_{12} and R_2 and L_{12} and L_2, respectively.

system becomes underdamped and produces an overshoot as shown in Fig. 16.15(a). Similarly, by decreasing C_{12}, the $\frac{C_{12}}{C_2}$ ratio is lowered and the magnitude of the voltage response falls below the target $|K_V|$ in the frequency range from DC to the break frequency. The system becomes underdamped and produces an overshoot as shown in Fig. 16.15(b).

Table 16.2. Tradeoff between the magnitude and frequency range of the voltage response

Tradeoff Scenario	Power Distribution System	Minimum $\lvert K_V \rvert$	Maximum $\lvert K_V \rvert$	Minimum frequency	Maximum frequency
I	Original	0.30	0.50	DC	∞
	Increased L_{12}	0.09	0.56	63 kHz	∞
	Decreased C_{12}	0.05	0.60	DC	63 kHz
II	Original	0.20	0.50	DC	∞
	Increased L_{12}	0.09	0.50	3 MHz	∞
	Decreased C_{12}	0.03	0.60	DC	3 MHz
III	Original	0.20	0.50	DC	∞
	Increased L_{12}	0.09	0.50	3 GHz	∞
	Decreased C_{12}	0.05	0.45	DC	3 GHz
Scenario I Board	Original circuit: $R_{12} = R_2 = 2\,\text{m}\Omega$, $L_{12} = L_2 = 1\,\text{nH}$, $C_{12} = 2\,\text{mF}$, $C_2 = 4\,\text{mF}$				
	Increased L_{12}: $R_{12} = R_2 = 2\,\text{m}\Omega$, $L_{12} = 10\,\text{nH}$, $L_2 = 1\,\text{nH}$, $C_{12} = 2\,\text{mF}$, $C_2 = 4\,\text{mF}$				
	Decreased C_{12}: $R_{12} = R_2 = 2\,\text{m}\Omega$, $L_{12} = L_2 = 1\,\text{nH}$, $C_{12} = 200\,\mu\text{F}$, $C_2 = 4\,\text{mF}$				
Scenario II Package	Original circuit: $R_{12} = R_2 = 10\,\text{m}\Omega$, $L_{12} = L_2 = 100\,\text{pH}$, $C_{12} = 10\,\mu\text{F}$, $C_2 = 40\,\mu\text{F}$				
	Increased L_{12}: $R_{12} = R_2 = 10\,\text{m}\Omega$, $L_{12} = 1\,\text{nH}$, $L_2 = 100\,\text{pH}$, $C_{12} = 10\,\mu\text{F}$, $C_2 = 40\,\mu\text{F}$				
	Decreased C_{12}: $R_{12} = R_2 = 10\,\text{m}\Omega$, $L_{12} = L_2 = 100\,\text{pH}$, $C_{12} = 1\,\mu\text{F}$, $C_2 = 40\,\mu\text{F}$				
Scenario III On-chip	Original circuit: $R_{12} = R_2 = 10\,\text{m}\Omega$, $L_{12} = L_2 = 100\,\text{fH}$, $C_{12} = 20\,\text{nF}$, $C_2 = 40\,\text{nF}$				
	Increased L_{12}: $R_{12} = R_2 = 10\,\text{m}\Omega$, $L_{12} = 1\,\text{pH}$, $L_2 = 100\,\text{fH}$, $C_{12} = 20\,\text{nF}$, $C_2 = 40\,\text{nF}$				
	Decreased C_{12}: $R_{12} = R_2 = 10\,\text{m}\Omega$, $L_{12} = L_2 = 100\,\text{fH}$, $C_{12} = 2\,\text{nF}$, $C_2 = 40\,\text{nF}$				

Three different tradeoff scenarios similar to the case study shown in Fig. 16.14 are summarized in Table 16.2. The design parameters for each scenario represent typical values of board, package, and on-chip

decoupling capacitors, as shown in Fig. 16.9. The original system in each scenario produces an overshoot-free voltage response over a wide range of operating frequencies from DC to the highest operating frequency of the system. By increasing the ESL of the decoupling capacitor placed between the two power supplies, the system produces an overshoot and the range of operating frequencies is divided by two. The same phenomenon takes place if the value of the decoupling capacitor placed between the two power supplies is decreased. In the first case, when the ESL is increased by an order of magnitude, the magnitude of the voltage response is lowered by more than an order of magnitude from the break frequency to infinity. When C_{12} is decreased by an order of magnitude, the magnitude of the voltage response is lowered by more than an order of magnitude from DC to the break frequency. Note from the table that the location of the break point depends upon the particular system parameters. The break frequency of the board system occurs at a lower frequency as compared to the break frequency of the package power delivery network. Similarly, the break frequency of the package power distribution system is lower than the break frequency of the on-chip system. As previously mentioned, for typical power supplies values and allowed ripple voltage, $|K_V|$ should be less than 0.1 to decouple a noisy power supply from a quiet power supply. As listed in Table 16.2, this requirement is satisfied for the power distribution system if L_{12} is increased or C_{12} is decreased. The magnitude of the overshoot falls rapidly with decreasing ESL of the decoupling capacitors. Due to the extremely low value of the ESL in an on-chip power network, typically several hundred femtohenrys, the magnitude of the overshoot does not exceed the maximum magnitude of the overshoot-free voltage response.

Unlike the design methodology for producing an overshoot-free response as described in Section 16.4.1, a design methodology to trade off the magnitude of the voltage response of the power distribution system with the frequency range of an overshoot-free response is as follows. Based upon the available decoupling capacitance, the decoupling capacitances for each power supply are determined. Depending upon the target frequency range with respect to the break frequency, the ESL of the capacitor placed between the two power supplies and the decoupling capacitors should both be increased (above the break frequency). Otherwise, the capacitor placed between the two power supplies and the ESL of all of the decoupling capacitors should both be decreased (below the break frequency).

16.5 Summary

A system of decoupling capacitors used in power distribution systems with multiple power supply voltages is described in this chapter. The primary conclusions are summarized as follows:

- Multiple on-chip power supply voltages are often utilized to reduce power dissipation without degrading system speed
- To maintain the impedance of a power distribution system below a specified impedance, multiple decoupling capacitors are placed at different levels of the power grid hierarchy
- The decoupling capacitors should be placed both with progressively decreasing value to shift the antiresonance spike beyond the maximum operating frequency and with increasing ESR to control the damping characteristics
- The magnitude of the antiresonant spikes can also be limited by reducing the ESL of each of the decoupling capacitors
- To maintain the magnitude of the voltage transfer function below 0.5, the ESR and ESL of the decoupling capacitors should be carefully chosen to satisfy the overshoot-free voltage response criterion
- To further decouple the power supplies in frequencies ranging from DC to the break frequency, both the capacitor placed between the two power supply voltages and the ESL of each of the decoupling capacitors should be decreased
- To decouple the power supplies in frequencies ranging from the break frequency to infinity, both the ESL of the capacitor placed between the two power supply voltages and the decoupling capacitors should be increased
- The frequency range of an overshoot-free voltage response can be traded off with the magnitude of the response