11

Inductance/Area/Resistance Tradeoffs

Tradeoffs among inductance, area, and resistance of power distribution grids are investigated in this chapter. As discussed in Section 1.3, design objectives, such as low impedance (low inductance and resistance), small area, and low current densities (for improved reliability), are typically in conflict. It is therefore important to make a balanced compromise among these design goals based upon application-specific constraints. A quantitative model of the inductance/area/resistance tradeoff in high performance power distribution networks is therefore necessary to achieve an efficient power distribution network. Another important goal is to provide quantitative guidelines to these tradeoffs and to bring intuition to the design of high performance power distribution networks.

Two tradeoff scenarios are considered in this chapter. The inductance versus resistance tradeoff under a constant grid area constraint in high performance power distribution grids is analyzed in Section 11.1. The inductance versus area tradeoff under a constant grid resistance constraint is analyzed in Section 11.2. The chapter concludes with a summary.

11.1 Inductance vs. resistance tradeoff under a constant grid area constraint

In the first tradeoff scenario, the fraction of the metal layer area dedicated to the power grid, called the grid area ratio and denoted as A, is assumed fixed, as shown in Fig. 11.1. The objective is to explore the tradeoff between grid inductance and resistance under the constraint of a constant area [276]. The area dedicated to the grid includes both

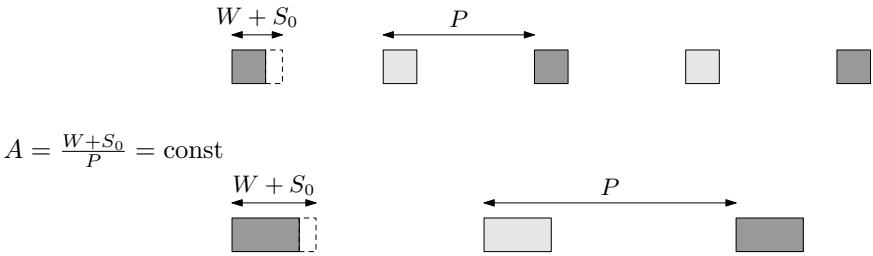

Fig. 11.1. Inductance versus resistance tradeoff scenario under a constant area constraint. As the line width varies, the grid area, including the minimum line spacing S_0, is maintained the same.

the line width W and the minimum spacing S_0 necessary to isolate the power line from any neighboring lines; therefore, the grid area ratio can be expressed as $A = \frac{W+S_0}{P}$, where P is the line pitch.

The inductance of paired grids is virtually independent of the separation between the power/ground line pairs. The effective current loop area in paired grids is primarily determined by the line spacing within each power/ground pair, which is much smaller than the separation between the power/ground pairs [69]. Therefore, only paired grids with an area ratio of 0.2 (*i.e.*, one fifth of the metal resources are allocated to the power and ground distribution) are considered here; the properties of paired grids with a different area ratio A (*i.e.*, different P/G separation) can be linearly extrapolated. In contrast, the dependence of the inductance of the interdigitated grids on the grid line pitch is substantial, since the effective current loop area is strongly dependent on the line pitch. Interdigitated grids with area ratios of 0.2 and 0.33 are analyzed here.

To investigate inductance tradeoffs in power distribution grids, the dependence of the grid inductance on line width is evaluated using FastHenry. Paired and interdigitated grids consisting of ten P/G lines are investigated. A line length of 1000 μm and a line thickness of 1 μm are assumed. The minimum spacing between the lines S_0 is 0.5 μm. The line width W is varied from 0.5 μm to 5 μm.

The grid inductance L_{grid} versus line width is shown in Fig. 11.2 for two signal frequencies: 1 GHz (the low frequency case) and 100 GHz (the high frequency case). The high frequency inductance is within 10% of the low frequency inductance for interdigitated grids, as mentioned

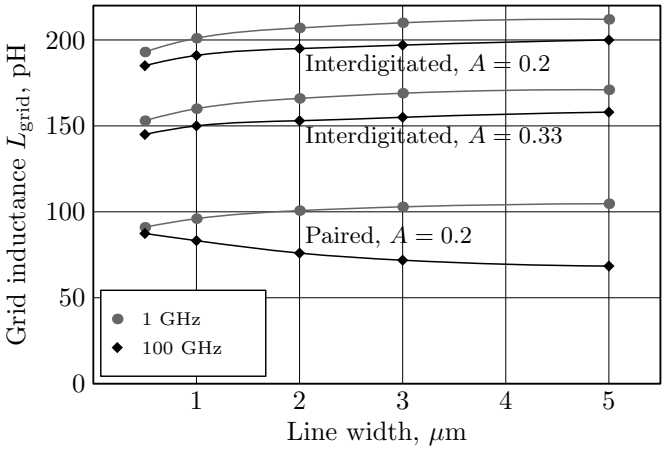

Fig. 11.2. The grid inductance versus line width under a constant grid area constraint for paired and interdigitated grids with ten P/G lines.

previously. The large change in inductance for paired grids is due to the proximity effect in closely spaced, relatively wide lines.

With increasing line width W, the grid line pitch P (and, consequently, the grid width) increases accordingly so as to maintain the desired grid area ratio $A = \frac{W+S_0}{P}$. Therefore, the inductance of a grid with a specific line width cannot be directly compared to the inductance of a grid with a different line width due to the difference in grid width. To perform a meaningful comparison of the grid inductance, the dimension specific data shown in Fig. 11.2 is converted to a dimension independent sheet inductance. The sheet inductance of a grid with a fixed area ratio A, $L_{\square}^{A}$, can be determined from L_{grid} through the following relationship,

$$L_{\square}^{A}(W) = L_{\text{grid}} \frac{NP}{l} = L_{\text{grid}} \frac{N}{l} \frac{W + S_0}{A}, \tag{11.1}$$

where N is the number of lines (line pairs), P is the line (line pair) pitch in an interdigitated (paired) grid, and l is the grid length. For each of the six L_{grid} data sets shown in Fig. 11.2, a correspondent $L_{\square}^{A}$ versus line width data set is plotted in Fig. 11.3. As illustrated in Fig. 11.3, the sheet inductance $L_{\square}^{A}$ increases with line width; this increase with line width can be approximated as a linear dependence with high accuracy.

The low frequency sheet resistance of a grid is $R_{\square} = \rho_{\square} \frac{P}{W}$. The grid resistance under a constant area ratio constraint, $A = \frac{W+S_0}{P} = \text{const}$,

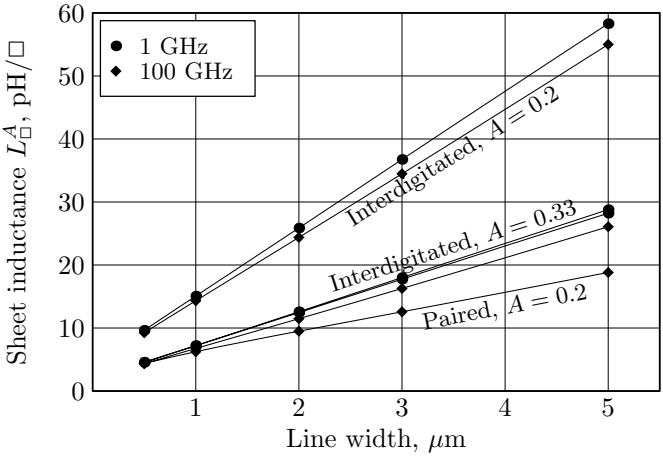

Fig. 11.3. The sheet inductance $L_\square^A$ versus line width under a constant grid area constraint.

can be expressed as a function of only the line width W,

$$R_\square^A = \frac{\rho_\square}{A}\frac{W + S_0}{W}. \tag{11.2}$$

This expression shows that as the line width W increases from the minimum line width $W_{\min} = S_0$ ($\frac{W+S_0}{W} = 2$) to a large width ($W \gg S_0$, $\frac{W+S_0}{W} \simeq 1$), the resistance decreases twofold. An intuitive explanation of this result is that at the minimum line width $W_{\min} = S_0$, only half of the grid area used for power routing is filled with metal lines (the other half is used for line spacing) while for large widths $W \gg S_0$, almost all of the grid area is metal.

In order to better observe the relative dependence of the grid sheet inductance and resistance on the line width, $L_\square^A$ and $R_\square^A$ are plotted in Fig. 11.4 normalized to the respective values at a minimum line width of $0.5\,\mu$m (such that $L_\square^A$ and $R_\square^A$ are equal to one normalized unit at $0.5\,\mu$m). As shown in Fig. 11.4, five out of six $L_\square^A$ lines have a similar slope. These lines depict the inductance of a paired grid at 1 GHz and the inductance of two interdigitated grids ($A = 0.2$ and $A = 0.33$) at 1 GHz and 100 GHz. The line with a lower slope represents a paired grid at 100 GHz. This different behavior is due to pronounced proximity effects in closely placed wide lines with very high frequency signals.

The dependence of the grid sheet inductance on line width is virtually linear and can be accurately approximated by

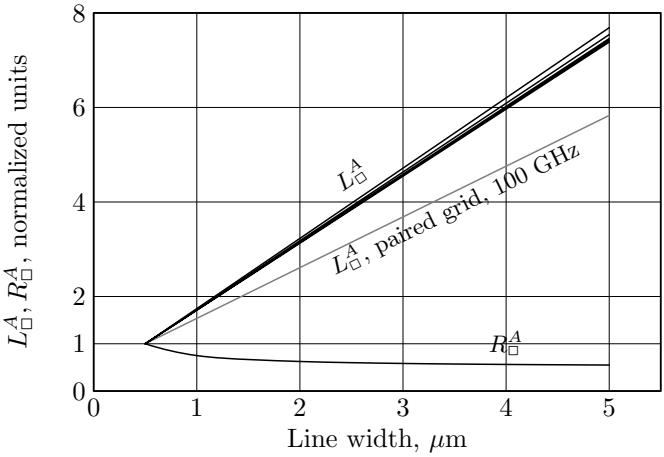

Fig. 11.4. Normalized sheet inductance and sheet resistance versus the width of the P/G line under a constant grid area constraint.

$$L^A_\square(W) = L^A_\square(W_{\min}) \cdot \{1 + K \cdot (W - W_{\min})\}\,, \tag{11.3}$$

where $L^A_\square(W_{\min})$ is the sheet inductance of a grid with a minimum line width and K is the slope of the lines shown in Fig. 11.4. Note that while $L^A_\square(W_{\min})$ depends on the grid type and area ratio (as illustrated in Fig. 11.3), the coefficient K is virtually independent of these parameters (with the exception of the special case of paired grids at 100 GHz).

The grid inductance increases with line width, as shown in Fig. 11.4. The inductance increases eightfold (sixfold for the special case of a paired grid at 100 GHz) for a tenfold increase in line width [276]. The grid resistance decreases nonlinearly with line width. As mentioned previously, this decrease in resistance is limited to a factor of two.

The inductance versus resistance tradeoff has an important implication in the case where at the minimum line width the peak power noise is determined by the resistive voltage drop IR, but at the maximum line width the inductive voltage drop $L\frac{dI}{dt}$ is dominant. As the line width decreases, the inductive $L\frac{dI}{dt}$ noise becomes smaller due to the lower grid inductance L while the resistive IR noise increases due to the greater grid resistance R, as shown in Fig. 11.4. Therefore, a minimum total power supply noise, $IR + L\frac{dI}{dt}$, exists at some target line width. The line width that produces the minimum noise depends upon the ratio and relative timing of the peak current demand I and the peak transient current demand $\frac{dI}{dt}$. The optimal line width is, therefore,

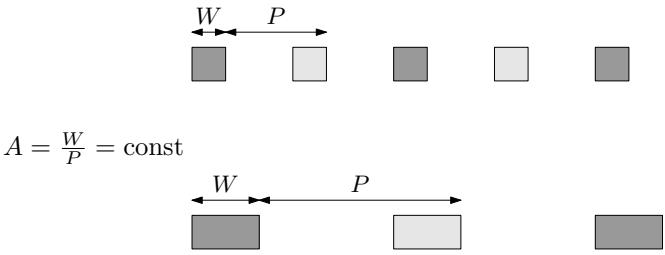

Fig. 11.5. Inductance versus area tradeoff scenario under a constant resistance constraint. As the line width varies, the metal area of the grid and, consequently, the grid resistance are maintained constant.

application dependent. This tradeoff provides guidelines for choosing the width of the power grid lines that produces the minimum noise.

11.2 Inductance vs. area tradeoff under a constant grid resistance constraint

In the second tradeoff scenario, the resistance of the power distribution grid is fixed (for example, by IR drop or electromigration constraints) [276], as shown in Fig. 11.5. The grid sheet resistance is

$$R_{\square} = \rho_{\square} \frac{P}{W} = \frac{\rho_{\square}}{M} = \text{const}, \tag{11.4}$$

where $\rho_{\square}$ is the sheet resistivity of the metal layer and $M = \frac{W}{P}$ is the fraction of the area filled with power grid metal, henceforth called the metal ratio of the grid. The constant resistance $R_{\square}$ infers a constant grid metal ratio M. The constraint of a constant grid resistance is similar to that of a constant grid area except that the line spacings are not considered as a part of the grid area. The objective is to explore tradeoffs between the grid inductance and area under the constraint of a constant grid resistance. This analysis is conducted similarly to the analysis described in the previous subsection. The grid inductance L^R_{grid} versus line width is shown in Fig. 11.6. The corresponding sheet inductance $L^R_{\square}$ versus line width data set is plotted in Fig. 11.7. The normalized sheet inductance and grid area data, analogous to the data shown in Fig. 11.4, is depicted in Fig. 11.8.

As shown in Fig. 11.8, under a constant resistance constraint, the grid inductance increases linearly with line width. Unlike in the first

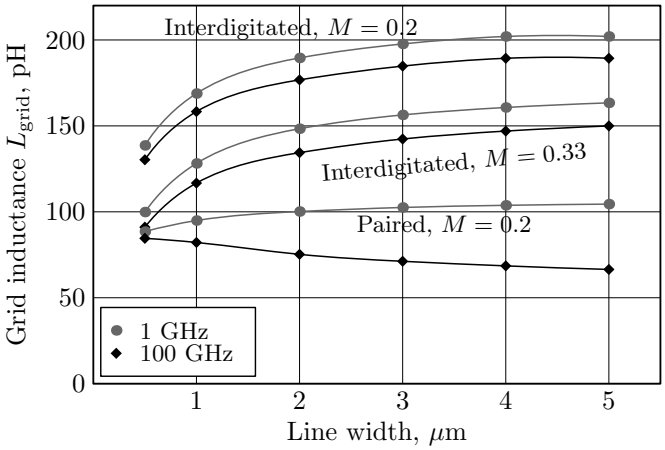

Fig. 11.6. The grid inductance versus line width under a constant grid resistance constraint for paired and interdigitated grids with ten P/G lines.

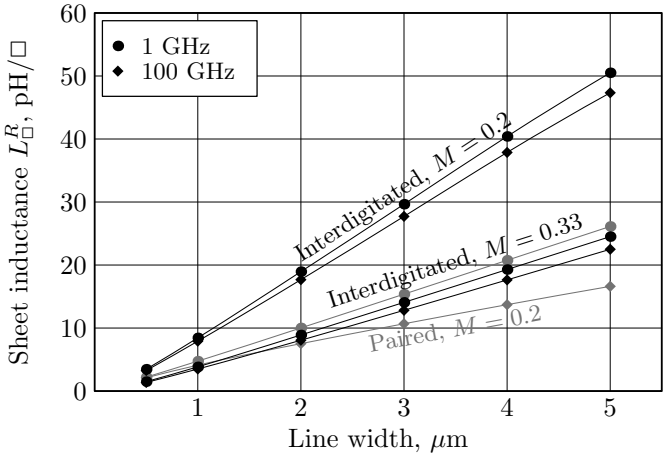

Fig. 11.7. The sheet inductance $L_{\square}^{R}$ versus line width under a constant grid resistance constraint.

scenario, the slope of the inductance increase with line width varies with the grid type and grid metal ratio. Paired grids have the lowest slope and interdigitated grids with a metal ratio of 0.33 have the highest slope. The lower slope of the inductance increase with line width is preferable, as, under a target resistance constraint, a smaller area and/or a less inductive power network implementation can be realized. The slope of the inductance increase with line width is independent

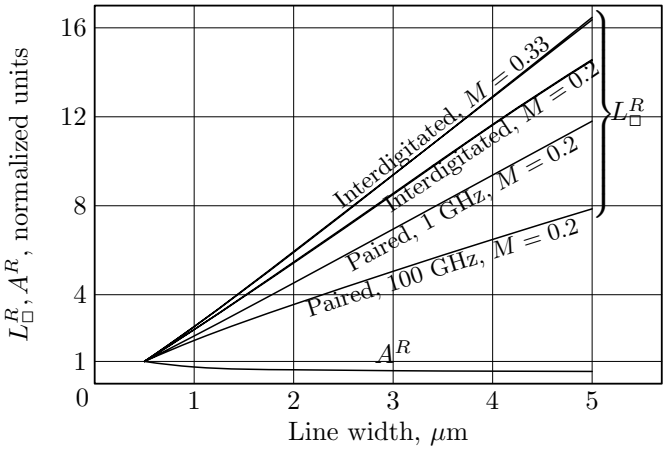

Fig. 11.8. Normalized sheet inductance $L^R_\square$ and grid area ratio A^R versus the width of the P/G line under a constant grid resistance (*i.e.*, constant grid metal ratio M) constraint.

of frequency in interdigitated grids (the lines for 1 GHz and 100 GHz coincide and are not discernible in the figure), while in paired grids the slope decreases significantly at high frequencies (100 GHz). The inductance increase varies from eight to sixteen fold, depending on grid type and grid resistance (*i.e.*, grid metal ratio), for a tenfold increase in line width. A reduction in the grid area is limited by a factor of two, similar to the decrease in resistance in the first tradeoff scenario.

11.3 Summary

Inductance/area/resistance tradeoffs in single layer power distribution grids are explored in this chapter. The primary conclusions can be summarized as follows.

- The grid inductance can be traded off against the grid resistance as the width of the grid lines is varied under a constant grid area constraint
- The grid inductance can be traded off against the grid area as the width of the grid lines is varied under a constant grid resistance constraint
- The grid inductance varies linearly with line width when either the grid resistance or the grid area is maintained constant

- The associated penalty in grid area (or resistance) is relatively small as long as the line width remains significantly greater than the minimum line spacing