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Processing and material issues related to lead-free soldering

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Abstract The European requirement for lead-free electronics has resulted in higher soldering temperature and some material and process changes. Traditional tin–lead solder melts at 183°C, where as the most common lead-free alternatives have a much higher melting temperature—tin–copper (227°C), tin–silver (221°C) and tin–silver–copper (217°C). These have challenged the ingenuity of the materials and process engineers. This chapter will explore some of the issues that have come up in this transition, and which these engineers have understood and addressed. As we enter the lead-free era, we see changes as printed wiring board (PWB) substrates which were designed for lower soldering temperatures are being replaced by newer materials. Factors such as glass transition temperature (T_g), decomposition temperature (T_d) and coefficient of thermal expansion must be considered. Many electronic components are made for lower peak temperatures than those required by the new solders. Solder flux chemistries are changing to meet the needs of the new metal systems, and cleaning of flux residues is becoming more of a challenge. Finally, there is a potential reliability problem—an increased potential for the growth of conductive anodic filament (CAF), an electrochemical failure mechanism that occurs in the use environment.

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1 Introduction

The age of lead-free soldering for electronics is upon us. Legislators in the European Union have demanded this, with few exceptions. While much research has been done on the reliability of the new solder systems, little has been said about the other materials which are affected. This chapter will review the questions and issues that must be understood relative to printed wiring substrate materials, soldering fluxes and pastes, the soldering process itself, the cleaning materials, and the changes that must take place because of the higher soldering temperatures required for most lead-free alternatives.

2 Alloy selection

The solder alloys most commonly used for electronics assembly contain tin (Sn) and lead (Pb) with a standard eutectic composition being Sn63Pb37. Compared to the tin–lead solder alloy, most lead-free alloys melt at much higher temperatures, while only a few melt at lower temperatures. Some solder replacement candidates are eutectic alloys melting at a single temperature, while others are non-eutectic alloys that melt over a temperature range. Table 1 lists the melting point or range for Sn/Pb eutectic compared with the other major alloys selected by most companies as the replacement.

3 Thermal processing requirements

Most lead-free alloys under investigation melt at temperatures that are 30–40°C higher than that of eutectic Sn/Pb solder. Several issues become important when

Table 1 Melting temperature of SnPb and Pb-free solder alloys

Alloy	Melting point (°C)
Sn–Pb37	183
Sn–Ag3.8–Cu0.7	217
Sn–Ag3.0–Cu0.5	217–220
Sn96.2Ag2.5Cu0.8Sb0.5	216
Sn–Cu0.7	227
Sn–Cu0.7 + Ni	227
Sn–Ag3.5	221
Sn–Zn9.0	198.5
Sn–Bi58	138

these higher soldering temperatures are used. These include the effect of these higher temperatures on components, soldering flux or paste chemistry, cleaning, and substrate material properties.

3.1 Printed wiring boards

Traditionally, FR-4 epoxy/glass boards have been used as the workhorse in the industry. Difunctional brominated epoxy-glass resins have a glass transition (T_g) temperature of 125–135°C. The poly functional epoxy has a T_g of 140–150°C, and the high temperature, one-component epoxy system has a T_g of ~ 180°C. Newer board materials [1] for lead-free soldering include FR-4 with phenolic (T_g 180), modified FR-4 (T_g 190–220), polyimide (T_g 250), polyphenylene oxide (T_g 180), polyphenylene ether (T_g 180) and others. The higher soldering temperatures required by lead-free processes may necessitate the use of a higher T_g laminate in most applications. These other substrate materials are available, but cost more and have other electrical and mechanical properties which provide renewed challenges.

Another property of the laminate that must also be considered is the decomposition temperature (T_d), a measure of the actual chemical physical degradation of the substrate system. Measured using a thermogravametric analysizer (TGA) T_d is defined as the temperature at which 5% of the mass of the sample is lost to decomposition [2].

The soldering process creates a difference in the expansion of the materials due to differences in their coefficient of thermal expansion (CTE). This is the fractional increase in length per unit length, over the temperature excursion range required for lead-free soldering. It is usually expressed as ppm/°C or 10^{-6}/K. The higher temperatures exacerbate those differences.

An electronic assembly contains a number of different components. The laminate is usually a composite of polymer and e-glass. This creates a material which is constrained in the X-Y direction (CTE 15–18), and thus expands in the Z direction upon heating (CTE-45–60). The base metallization on the board is copper (CTE-17), and this is also used in plating holes and vias. The silicon chip with a CTE of 2.6 may be packaged in an hermetic ceramic package (CTE 4–8) or a non-hermetic plastic package using epoxy molding compound (CTE 14–20). Alloy 42 which is used to connect the device electrically to the board has a CTE of 43. If the device is packaged as a BGA or micro-BGA, the CTE of the alloy can range between 20 and 30. Often an Underfill is used to mitigate the CTE mismatch between the chip, the package and the board. The underfill CTE is designed to match that of the solder. Table 2 lists the CTE of a few of the many materials that become part of the electronic assembly. It is clear that there are a number of thermal stresses that take place during the manufacturing process and that the higher soldering temperatures for lead-free soldering exacerbate these stresses. An increased scrap rate can be caused by board warpage, delamination, and material degradation.

Higher process temperatures will result in an increased scrap rate of FR-4 epoxy-glass printed wiring boards due to board warpage, delamination and material degradation (charring). In addition, boards processed at higher temperatures are prone to conductive anodic filament failure (CAF). In many cases new chip carrier materials will be required.

Table 2 Coefficient of thermal expansion values for a number of materials used in electronic assemblies

Material	Coefficient of thermal expansion ppm/°C	
Copper [3]	17	
Alloy 42 [4]	4.3	
Lead [3]	29	
Sn [5]	23.5	
Sn63Pb37 [6]	21.6–28.9	
Sn98.8Cu0.7Sb0.5 [6]	17.4–22.1	
Sn95.5Ag3.8Cu0.7 [6]	17.6–18.8	
Sn96.2Ag2.5Cu0.8Sb0.5 [6]	26.9	
Sn96.5Ag3.5 [7]	20.2–22.9	
Sn99.3Cu0.7 (Nihon Superior, private communication)	26.5	
Alumina [3]	7	
Silicon [3]	2.6	
Epoxy molding compound [3]	14–20	
Ceramic [8]	4–8	
Underfill	20–29	
Laminates [9]	X, Y axis	Z axis
Epoxy/e-glass	15–18	45–60
Polyimide/e-glass	15–18	45–60

Engelmaier [10] has proposed a Soldering Temperature Impact Index (STII) to take into account the relative effect of these factors.

$$\text{STII} = (T_g + T_d)/2 - \%\ \text{Z-axis expansion}\ (\Delta T)$$

where ΔT represents the temperature excursion during the soldering process (50–260°C). Engelmaier proposes a minimum index of 215 for lead-free applications. Table 3 gives an example of eight commercially available substrate materials. It can be seen that the materials A, B, C and E fall below this value and would not be suitable for lead-free applications.

Material A and B have significantly different index values because of the improved T_d for material B. Material C has a low T_g but a high T_d, while Material E has a high T_g but poor T_d. In both cases, this leads to a low STII. Material D's low Z-axis expansion and F's higher T_d make these the highest rated materials. Kelley [6] notes that materials that have high T_d values survive more thermal processing cycles.

Plated through holes, and vias become a concern as well [11]. New laminate materials make processing more difficult. In addition, it is more difficult to plate the small vias used in today's electronics. One material supplier [12] has defined the difficulty factor in plating vias as:

$$\text{Difficulty Factor} = L^2/D$$

where L is the board thickness and D is the diameter of the hole.

Another factor is the thickness of the copper in the hole or via. A minimum of 25 microns is essential to insure that the via or barrel does not completely dissolve during the soldering process since the lead-free alloys are high Sn materials and Cu dissolves in this rapidly. Also, the thicker the multilayer board, the greater the stress on the plated holes during the soldering cycle, especially in the z-direction.

Table 3 Comparison of the thermal property values of eight commercially available laminate materials, with the calculated value of their soldering temperature impact index (STII)

Material	T_g°C	T_d °C	% Z-axis Expansion	STII
A	140	320	4.4	186
B	142	350	4.3	203
C	150	345	3.4	211
D	170	345	2.7	231
E	172	310	3.4	208
F	175	350	3.2	231
G	180	350	3.2	226
H	180	350	3.5	222

3.2 Surface finish

There are several laminate surface finishes available for lead-free applications. These include organic solubility preservatives (OSP), immersion silver, electrolytic nickel/gold, electroless nickel/immersion gold (ENIG), and immersion tin. The surface finish chosen should be compatible with the soldering flux.

3.3 Flux chemistry

Soldering [13] is defined as the process of joining metallic surfaces with solder without the melting of the basis metal. In order for this joining to take place, the metal surfaces must be clean of contamination and oxidation. This cleaning action is performed by the flux [2] a chemically active compound which, when heated, removes minor surface oxidation, minimizes oxidation of the basis metal, and promotes the formation of an intermetallic layer between solder and basis metal.

Solder fluxes and pastes have gone through significant evolution since the early 1980s. Before then, soldering fluxes were traditionally rosin-based and they conformed to military specifications and nomenclature: R—rosin, RMA—rosin mildly active, RA—rosin active and RSA—rosin super activated. The activation levels were determined by an extract resistivity test among others. There were also water soluble fluxes used for some applications. In the past, most fluxes contained 25 to 30% solids. Today, new flux formulations use weak organic acids and have much lower solids content (1.5–5 %). These low residue fluxes are often not cleaned—thus the term No Clean Flux. In North America about 70% of the fluxes are not cleaned, 25% are water soluble and 5% are rosin based for military applications [14].

The IPC J-STD-004 [15] for soldering fluxes defines a series of test that are to be used to characterize fluxes. These tests are designed to evaluate the corrosive characteristics of the flux and the flux residues. Fluxes are then defined by their main constituent under one of four categories: R0—Rosin, RE—Resin, OR—Organic, and IN—inorganic. They are further categorized as: L—low flux or flux residue activity, M—moderate flux or flux residue activity and H—high flux or flux residue activity with zero or one being added to identify whether halide has been added to the flux. Thus, an ROL1 flux is a rosin, low-activity flux which contains some halide ($<0.5\%$).

The role of the flux is to remove oxides and other contaminants on the metal surfaces to be soldered. The flux contains several ingredients:

- Activators—react with and remove the metal oxides.
- Vehicle—coats the surface to be soldered, dissolves the metal salts produced when the activator reacts with the oxides, and provides a covering for the cleaned metal surface to prevent further oxidation until soldering takes place.
- Solvent—dissolves the activators and vehicle and deposits them uniformly on the board and component surfaces.
- Special additives—rheological agents and other special ingredients are added to fluxes used in solder pastes, paste flux, and cored wire flux.

The flux becomes active as it is heated. In traditional flux chemistry for Sn/Pb solder, the assembly is preheated to around 100–125°C to remove the solvent and begin to activate the chemicals used to remove the metal oxide. After this plateau, the temperature is increased above the melting point of the solder (183°C) to 240°C for sufficient time to reflow the solder paste, and then the assembly is cooled, solidifying the solder and creating a metallurgical bond between the board metallization and the components. For lead-free soldering the preheat plateau temperature is higher – 150–200°C – and the peak temperature is 245–260°C. This requires solvents that evaporate at a higher temperature, and activators that become chemically active at a higher temperature. In addition, new activators are needed to address the new metallurgy on board surfaces, and new lead-free solders containing Ag, Cu and much higher levels of Sn.

3.4 Cleaning

For some applications, the removal of the solder flux residues is essential, e.g. before conformal coating, or for reasons of reliability. In the 1970s chlorinated solvents such as perchloroethylene, trichloroethylene and methyl chloroform were used to remove flux residues. When they became suspect as potential carcinogens, the chlorofluorocarbon (CFC) based solvents became prominent, and surfactant based water cleaning processes were used. The elimination of CFCs in 1994 let to the prominent use of low solids/no clean fluxes. Water soluble fluxes were cleaned with water, and surfactants and semi-aqueous solvents were used to remove rosin or resin flux residues. The challenge for cleaning in the lead-free era comes from the higher soldering temperatures that create residues that are more difficult to remove. New cleaning agents are being developed to address these issues.

3.5 Components

In manufacturing complex, printed wiring assemblies (PWAs), the thermal process chosen must take into account the thermal mass of the assembly, the component density, the solder flux/paste characteristics, and the maximum temperature limitation of the components. Most of the components assembled to the board in the soldering process, have a maximum temperature of 240°C for traditional Sn/Pb soldering. Some electronic components, such as electrolytic capacitors and plastic-encapsulated components are not rated to experience the high temperatures required to process with lead-free solders. The resulting heat-induced degradation can result in early field failures. Also, the higher temperatures required for lead-free solders are not compatible with many optoelectronic components. The increased heat can cause a variety of conditions with these components, among them: electrical variances, changes in silver-epoxy die attach properties, delamination between plastic and lead-frame parts, deformation of plastic encapsulants and plastic lenses, damage to lens coatings and changes in the light transmission properties.

IPC/JEDEC [16] has developed a recommended reflow profile for nonhermetic packaged semiconductor components. These are based on the temperature taken at the top-side of the packaged device. These recommendations are based on package volume excluding external leads, or solder balls in the case of ball grid arrays (BGAs), and non-integrated heat sinks. Table 4 lists the recommended range for Sn/Pb and Pb-free assemblies.

The maximum recommended temperature for the package depends on the package thickness and volume. Table 5 lists the recommended reflow temperatures for Sn/Pb processing while Table 6 lists the recommendations for Pb-free processing.

Table 4 Reflow profiles recommended for Sn/Pb and Pb-free Assemblies based on temperatures taken on the package body

Profile feature	Sn/Pb assemblies	Pb-free assemblies
Average ramp-up rate	3°C/s max	3°C/s max
Preheat		
- Temperature min	100°C	150°C
- Temperature max	150°C	200°C
- Time	60–120 s	60–180 s
Time maintained above melting temperature	60–150 s	60–150 s
Time within 5°C of peak temperatgure (T_p)	10–30 s	20–40 s
Ramp-down rate	6°C/s max	6°C/s max
Time 25°C to T_p	6 min max	8 min max

Table 5 Recommended maximum package reflow temperatures for Sn/Pb process

Package thickness	Volume <350 mm^3	Volume ≥ 350 mm^3
<2.5 mm	240 + 0/ − 5°C	225 + 0/ − 5°C
≥ 2.5 mm	225 + 0/ − 5°C	225 + 0/ − 5°C

Table 6 Recommended maximum package reflow temperatures for Pb-free process

Package thickness	Volume <350 mm^3	Volume 350–2000 mm^3	Volume >2000 mm^3
<1.6 mm	260 + 0°C	260 + 0°C	260 + 0°C
1.6–2.5 mm	260 + 0°C	250 + 0°C	245 + 0°C
≥ 2.5 mm	250 + 0°C	245 + 0°C	245 + 0°C

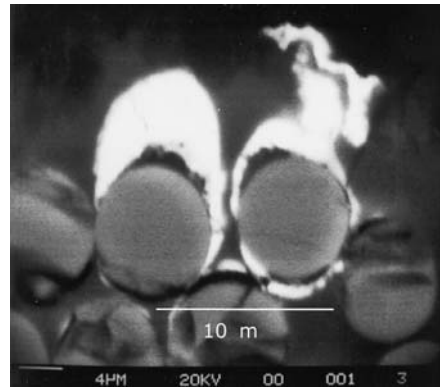

Fig. 1 Cross section of a PWB showing CAF growing along the epoxy/glass interface

4 Conductive anodic filament formation

One failure mode in printed wiring boards that is enhanced by the higher temperatures needed for lead-free soldering is conductive anodic filament (CAF) formation [17]. This failure mode was first reported in 1976 by researchers at Bell Labs [18]. It involves the electrochemical growth of a copper-containing filament subsurface along the polymer-glass interface of a PWB, from anode to cathode. A model developed by the Bell Labs researchers [19] in the late 1970s [20] details the mechanism by which CAF formation and growth occurs. The first step is a physical degradation of the glass/epoxy bond. Moisture absorption then occurs under high humidity conditions. This creates an aqueous medium along the separated glass/epoxy interface that provides an electrochemical pathway and facilitates the transport of corrosion products. A close up of this phenomenon for a real assembly is shown in Fig. 1.

Despite the projected lifetime reduction due to CAF, field failures were not identified in the 1980s. More recently, however, field failures of critical equipment have been reported [21]. Factors that affect this failure mode are substrate choice, conductor configuration, voltage gradient, and storage and use environment. Certain soldering fluxes [22] and HASL fluids, high humidity either in the storage or the use environment, and high voltage gradient enhance this failure mechanism. A recent study indicates that the higher reflow temperatures needed for lead-free soldering will result in significantly higher incidents of CAF in the future [17].

The objective of the study was to evaluate a series of water-soluble fluxes for their propensity to enhance CAF and to determine the effect of reflow temperature on the number of CAF observed. Specifically, it looked at 201°C as the peak temperature experienced by a PWB during wave soldering with Sn/Pb solder versus 241°C peak expected with lead-free wave soldering. The fluxes in this study contained 20 w% of one of the following vehicles: polyethylene glycol [PEG], polypropylene glycol [PPG], polyethylene propylene glycol MW1800 [PEPG 18] and polyethylene propylene glycol MW2600 [PEPG26], glycerine [GLY], octyl phenol ethoxylate [OPE] and a modified linear aliphatic polyether [LAP] dissolved in isopropyl alcohol (IPA). Flux formulations containing 20 w% of the different flux vehicles were also tested with 2 w% HBr or HCl activators, to see what effects the presence of the halide had on CAF formation.

The test boards were IPC-B-24 boards (Fig. 2) containing four comb patterns per board. Two boards for each flux were processed and cleaned. The coupons were placed in a temperature humidity chamber at 85°C and 85% RH, and surface insulation resistance (SIR) measurements were taken for all the boards at 24-hour intervals, over a 28-day period. The SIR testing was done using a bias voltage and a test voltage of 100 V and the same polarity. At the end of 28 days, each board was examined under an optical microscope using back-lighting and the number of CAF counted. Figure 3 shows how the CAF appears as dark shadows originating at the anode when viewed with back lighting.

Table 7 shows the average SIR levels at the end of the 28-day test for boards reflowed at 201°C and at 241°C. Most of the electrical readings were the same for both reflow temperatures. Exceptions to that include PEG/HCl and PEG/HBr which had acceptably high SIR readings (high 10^8) for the 241°C reflow

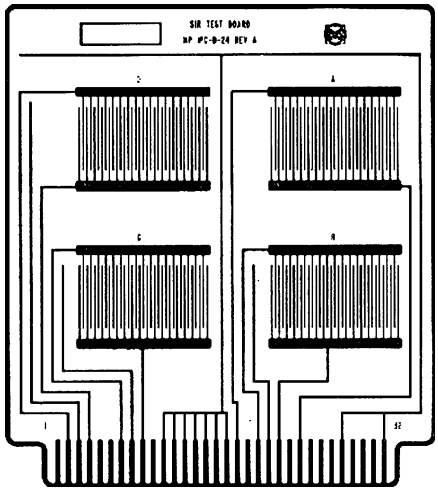

Fig. 2 IPC-B-24 Test Board

conditions but failed electrically ($<10^6$) at the 201°C reflow temperature. Additionally, glycerine (GLY) gave slightly lower SIR readings (high 10^9 vs. $>10^{10}$) under the higher temperature reflow conditions. Table 6 also shows the total number of CAF observed on two boards for each flux chemistry under each of the reflow conditions.

The following observations were made:

- PEG: CAF only forms when no halide activator was present. Also, the numbers of CAF at the *lower* reflow temperature were almost twice as many as at the *higher* reflow temperature. For all PEG fluxes the SIR levels were below the value of the limiting resistor in the circuit, i.e. 10^6 indicating that they have failed the SIR electrical test, except the halide formulations at higher reflow.
- PPG: CAF was almost non-existent at the lower reflow temperature. But many hundreds were observed for all three flux formulations at the higher reflow temperature.
- PEPG 18: There were 13–400 × as many CAF caused by the higher reflow temperature. At the higher reflow temperature the halide-free formulation had the largest number of CAF. At the lower temperature the pattern was: Cl^- activated > Br^- activated. None were observed for the halide free flux.
- PEPG 26: At the higher temperature the number of CAF followed the pattern: Cl^- activated > halide-free > Br^- activated flux. At the lower temperature the number of CAF followed a different pattern: Cl^- activated > Br^- activated. None were observed for the halide-free flux. Also, the total number of CAF observed at both temperatures were significantly less than those noted for the lower molecular weight PEPG 18 flux formulations.
- GLY: CAF is predominantly associated at the higher reflow temperature with Cl^- activated > Br^- activated > halide-free. At the lower reflow temperature, only the Br^- activated gave a few CAF.
- OPE: At the higher reflow temperature, Br^- activated flux >> halide-free > Cl^- activated. At the higher reflow temperature the number of CAF was 4–300 × as many as at the lower reflow temperature. And, at the lower reflow temperature the Cl^- activated flux performed the worst.
- LAP: At the higher reflow temperature Br^- activated > Cl^- activated, whereas at the lower reflow temperature only the Cl^- activated flux showed CAF and this was less than 10 × as many as for the higher temperature.

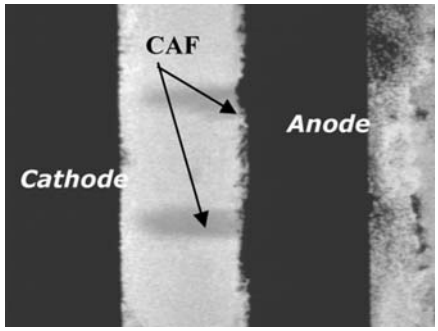

Fig. 3 Using back lighting CAF appears as dark shadows coming from the copper anode to the cathode. The spacing between the anode and cathode is 0.5 mm

It is clear from the above data that the interactions of the flux and processing temperature with the test boards is complex and needs further study. Diffusion of polyglycols into the PWB substrate occurs during soldering. Since the diffusion process follows Arrhenius behavior, the length of time the board is above the glass transition temperature will have an effect on the amount of polyglycol absorbed into the epoxy and that will, in turn, affect its electrical properties. Diffusion will also depend upon the specific chemistry of the flux vehicle and its interaction with the substrate. Brous [23] linked the level of polyglycol in a board to surface insulation resistance (SIR) measurements. Jachim re-

Table 7 Comparison of SIR levels and number of CAF associated with two different reflow temperatures

Flux	SIR (Ω) 201°C reflow	SIR (Ω) 241°Creflow	#CAF at 201°C reflow	#CAF at 241°C reflow
Polyethylene glycol-600(PEG)	$<10^6$	$<10^6$	90	55
PEG/HCl	$<10^6$	High 10^8	None	None
PEG/HBr	$<10^6$	High 10^8	None	None
Polypropylene glycol 1200 (PPG)	$>10^{10}$	$>10^{10}$	None	455
PPG/HCl	$>10^{10}$	$>10^{10}$	None	379
PPG/HBr	$>10^{10}$	$>10^{10}$	1	423
Polyethylene propylene glycol 1800 (PEPG 18)	High 10^9	High 10^9	1	406
PEPG 18/HCl	High 10^9	High 10^9	10	135
PEPG 18/HBr	10^{10}	High 10^9	9	279
Polyethylene propylene glycol 2600 (PEPG 26)	High 10^9	High 10^9	None	91
PEPG 26/HCl	High 10^9	High 10^9	6	218
PEPG 26/HBr	10^{10}	High 10^9	None	51
Glycerine (GLY)	$>10^{10}$	High 10^9	None	56
GLY/HCl	$>10^{10}$	High 10^9	None	583
GLY/HBr	$>10^{10}$	High 10^9	3	104
Ocyl phenol ethoxylate (OPE)	Low 10^9	Low 10^9	None	83
OPE/HCl	Low 10^9	Low 10^9	14	62
OPE/HBr	$>10^{10}$	High 10^9	2	599
Linear aliphatic polyether (LAP)	Low 10^9	Not Tested	None	Not Tested
LAP/HCl	Low 10^9	Low 10^9	15	203
LAP/HBr	Low 10^9	Low 10^9	None	272

ported on water-soluble flux-treated test coupons that were prepared using two different thermal profiles. Those which experienced the higher thermal profile exhibited a SIR level that was an order of magnitude lower than those processed under less aggressive thermal conditions. It is clear that the higher the soldering temperature, the greater the polyglycol absorption. Similarly, for each thermal excursion that occurs, the bonding between the epoxy and glass fibers is weakened due to different coefficient of thermal expansion characteristics of these two materials.

One way of quantifying the effect of the reflow temperature on CAF is to examine the thermal strain (ε) associated with the difference in coefficient of thermal expansion (ΔCTE) between the adjacent materials. Table 8 details that comparison for copper versus FR-4 substrate and e-glass versus epoxy where:

$$\varepsilon = \Delta\text{CTE}\ \Delta T$$

It is clear from this table that the higher reflow temperature creates a severe strain on the epoxy/glass interface, weakening the bond and in general, enhancing the rate of CAF formation. This explains the much higher level of CAF observed for the higher reflow temperature.

Table 8 Thermal strain ($\times 10^{-6}$) assuming an initial temperature of 25 °C

Material	ΔCTE ($\times 10^{-6}$/K)	ε at 201°C reflow	ε at 241°C reflow
Cu/FR-4	2	352	432
e-glass/epoxy	15	2640	3240

Higher board processing temperatures result in increased numbers of CAF for most of the fluxes tested. The 241°C peak temperature represents the wave soldering peak temperature for a typical lead-free solder alloy. Reflow temperatures for solder pastes will be even higher.

5 Summary

The move to lead-free electronics involves a number of material and process issues which are being addressed. These issues are driven by the higher soldering temperatures required for most lead-free solders. Traditional tin–lead solder melts at 183°C, where as the most common lead-free alternatives have a much higher melting temperature—tin–copper (227°C), tin–silver (221°C) and tin–silver–copper (217°C). Other materials are also affected. These include the printed wiring board substrate, the components, the flux and cleaning chemistries, among others.

A failure mode in PWBs that is enhanced by the higher soldering temperatures, conductive anodic filament formation has been described and discussed. This failure is due to electrochemical migration in the use environment. The enhancement related to various flux

chemistries has been described. While the CTE mismatch between epoxy and glass place stress on the board, further work is in progress to understand the complicated flux interactions.

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