Chapter 2
The Charge Sheet Model Revisited

2.1 Why the Charge Sheet Model?

We review in this chapter the main attributes of the 'Charge Sheet Model' (C.S.M.) introduced by J.R. Brews in 1978 (Brews 1978; Van de Wiele 1979). Although its name contains the word 'Model', the C.S.M is not a design tool. It is an invaluable means however for understanding some of the mechanisms governing current in MOS transistors for it scrutenizes phenomena otherwise difficult to apprehend. Unfortunately, the C.S.M. concerns only long channel MOS transistors implemented in a uniformly doped substrate (gradual channel approximation). Trying to predict drain currents of real transistors with the C.S.M. does not work.

Figure 2.1 depicts the structure of the NMOS transistor considered throughout this chapter. The two vertical lines without any other demarcation called respectively S and D symbolize the source and drain junctions. Two-dimensional effects are ignored, obliterating consequently items such as channel length modulation, Drain Induced Barrier Lowering (DIBL), etc. The source, drain and gate voltages are called respectively V_S, V_D and V_G, the surface potential ψ_S and the non-equilibrium voltage V.[1] The latter, called also the channel voltage, varies from V_S at the source to V_D at the drain. Single indices relate to voltages defined with respect to the substrate. Double indices relate to voltages defined with respect to references other than the substrate. For instance, V_{GS} is the voltage difference between the gate and the source.

2.2 The Generic Drain Current Equation

Current in MOS transistors results from mobile carries moving in the channel. It can be represented by the expression below where W is the width of the transistor and Q'_i the mobile charge density along the channel:

$$I_D = W \cdot \left(-Q'_i\right) \cdot velocity \tag{2.1}$$

[1] V is the difference between the "quasi Fermi level" of electrons in the inversion layer and the "quasi Fermi level" of holes in the substrate.

P.G.A. Jespers, *The g_m/I_D Methodology, A Sizing Tool for Low-voltage Analog CMOS Circuits*, Analog Circuits and Signal Processing, DOI 10.1007/978-0-387-47101-3_2,

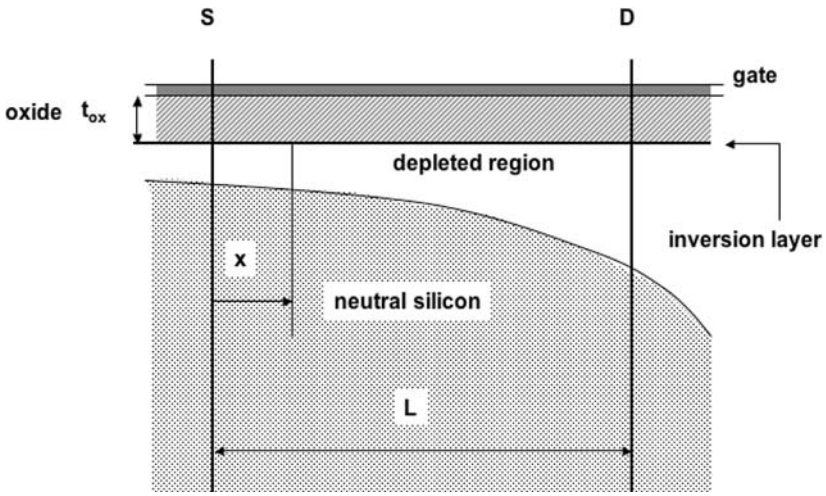

Fig. 2.1 The gradual channel MOS transistor

Two transport mechanisms are taking place currently: *drift* and *diffusion*. The *drift current* velocity is supposed to be proportional to the electrical field E:

$$\textit{drift current velocity} = -\mu \, \mathrm{E} \tag{2.2}$$

The *mobility coefficient* μ is assumed to be constant generally. This is correct as long as electrical fields do not exceed some limit. Modern transistors face very large fields for their gate lengths are ever shorter while supply voltages don't scale down necessarily at the same rate. As electrical fields are getting larger, the velocity of the carriers starts to slow down so that mobility declines. The effect can be taken into account by making μ a function of the electrical field.

The *diffusion current* is governed by the non-uniform concentration of carriers (like gas scattering in a closed vessel to homogenize the pressure). The diffusion current velocity is supposed to be proportional to the carrier's concentration:

$$\textit{diffusion current velocity} = -D \frac{1}{n} \frac{\partial n}{\partial x} = -D \frac{1}{Q_i'} \frac{\partial Q_i'}{\partial x} \tag{2.3}$$

The *diffusion constant D* is related to the mobility μ by the Einstein relation:

$$D = \mu U_T \tag{2.4}$$

As the electrical field along the channel is replaced by the derivative of the surface potential ψ_S:

$$\mathrm{E} = -\frac{d\psi_S}{dx} \tag{2.5}$$

Equation 2.1 can be rewritten as follows:

$$I_D = \mu W \left[-Q_i' \frac{d\psi_S}{dx} + U_T \frac{dQ_i'}{dx} \right] \tag{2.6}$$

or:

$$I_D \, dx = \mu W \left[-Q_i' \, d\psi_S + U_T \, dQ_i' \right] \tag{2.7}$$

While the left side of the above equation lends itself to integration (current is constant along the channel), the right part doesn't. One of the two integration variables should be expressed as a function of the other. Two strategies are possible. In the Charge Sheet Model, the charge density is expressed as a function of the surface potential. In the compact model, discussed in Chapter 4, the surface potential is expressed as a function of the charge density. The first representation follows a rigorous treatment while the second implies an approximation. The first does not lend itself to circuit design, the second does.

2.3 The Charge Sheet Model *Drain Current Equation*

In this chapter, we lay down the grounds of the Charge Sheet Model. We take the surface potential as integration variable rewriting the right part of Eq. 2.7 as shown below after introducing the gate oxide capacitance per unit-area C'_{ox}:

$$I_D \, dx = \mu C_{ox}' W \left[-\frac{Q_i'}{C_{ox}'} + U_T \frac{d}{d\psi_S} \left(\frac{Q_i'}{C_{ox}'} \right) \right] d\psi_S \tag{2.8}$$

To perform the integration, an expression of Q'_i/C'_{ox} versus the surface potential is required. The equation is derived currently from the total charge density Q_t/C'_{ox} expression obtained after combining the Gauss law, the Poisson equation and Boltzmann statistics (detailed computations can be found in textbooks):

$$-\frac{Q_t'}{C_{ox}'} = \gamma \cdot \left[U_T \exp\left(\frac{\psi_S - 2\phi_B - V}{U_T} \right) + \psi_S \right]^{1/2} \tag{2.9}$$

where:

V represents the non-equilibrium voltage along the channel
Φ_B is the bulk potential, depending on the ratio of the substrate doping concentration N over the intrinsic carrier density of silicon n_i

$$\phi_B = U_T \log\left(\frac{N}{n_i} \right) \tag{2.10}$$

γ is the Gamma commonly used in SPICE, which depends on N and the oxide thickness via the oxide capacitance C'_{ox}:

$$\gamma = \frac{1}{C'_{ox}}\sqrt{2\,q\,\varepsilon_S N} \tag{2.11}$$

where q is the electron charge,
ε_S the silicon permittivity
N the substrate impurity concentration

The two terms under the square root of Eq. 2.9 relate respectively to the inversion charge density (left term) and the depleted charge density (right term). If we ignore the first term, in other words if the mobile charge density Q'_i vanishes, the total charge density Q'_t resumes to the fixed charge density Q'_b so that what remains of Eq. 2.9 boils down to:

$$-\frac{Q'_b}{C'_{ox}} = \gamma\sqrt{\psi_S} \tag{2.12}$$

An expression of the mobile carrier's density lies now for the hand. We start from the Gauss law[2]:

$$V_G = -\frac{Q'_t}{C'_{ox}} + \psi_S \tag{2.13}$$

Since Q'_t is the sum of mobile and fixed charge densities, we may write owing to Eq. 2.12:

$$V_G = -\frac{Q'_i}{C'_{ox}} + \gamma\sqrt{\psi_S} + \psi_S \tag{2.14}$$

which leads to the expression of Q'_i/C'_{ox} versus the surface potential that we are looking for:

$$-\frac{Q'_i}{C'_{ox}} = V_G - \gamma\sqrt{\psi_S} - \psi_S \tag{2.15}$$

We can evaluate now the derivative with respect to the surface potential of Q'_i/C'_{ox}:

$$d\left(-\frac{Q'_i}{C'_{oc}}\right) = -\left(1 + \frac{\gamma}{2\sqrt{\psi_S}}\right)d\psi_S \tag{2.16}$$

and combine Eqs. 2.8, 2.15 and 2.16 to get the differential equation below ready for integration:

$$I_D\,dx = \mu C'_{ox} W \cdot \left[V_G - \gamma\sqrt{\psi_S} - \psi_S + U_T\left(1 + \frac{\gamma}{2\sqrt{\psi_S}}\right)\right]d\psi_S \tag{2.17}$$

[2] The contact potentials between the gate material, the substrate material and the metal connections as well as the fixed charges trapped in the oxide produce a shift of the gate voltage that can be taken into account by adding to the gate voltage a constant voltage, called the Flat Band Voltage V_{FB}.

After integration, the expression of the drain current below is found where ψ_{SD} and ψ_{SS} represent respectively the surface potential at the drain and the source and β as usual $\mu C'_{ox} W/L$:

$$I_D = \beta \left[F(\psi_{SD}) - F(\psi_{SS}) \right] \tag{2.18}$$

with the function $F(\psi_S)$ given by:

$$F(\psi_S) = -\frac{1}{2}\psi_S^2 - \frac{2}{3}\gamma\, \psi_S^{1.5} + (V_G + U_T)\, \psi_S + \gamma\, U_T \psi_S^{0.5} \tag{2.19}$$

Equations 2.18 and 2.19 are interesting and frustrating results in the same time. The good news is that the drain current can be expressed as a polynomial of the square root of the surface potential. The bad news is that we must find a way to connect the source and drain surface potentials ψ_{SS} and ψ_{SD} to V_S and V_D. No analytical expression is available. The only way out is to extract the surface potential from the expression below resulting from the combination of Eqs. 2.13 and 2.9.

$$V_G = \gamma \cdot \left[U_T \exp\left(\frac{\psi_S - 2\phi_B - V}{U_T} \right) + \psi_S \right]^{1/2} + \psi_S \tag{2.20}$$

Since Eq. 2.20 is an implicit non-linear equation of ψ_S, the evaluation must be done numerically. The MATLAB function *surfpot* residing in the Matlab toolbox under 'extras.springer.com' takes care of this. For more details, please consult Annex 2.

2.4 Common Source Characteristics

The analytical expression of the drain current given by Eqs. 2.18 and 2.19 together with the *surfpot* function solving Eq. 2.20 pave the road towards experiments that help understanding the behavior of MOS transistors under low-power low-voltage conditions. Some examples are reviewed in the next sections considering an N-channel transistor implemented in a substrate having an impurity concentration equal to 10^{17} atoms cm^{-3} and an oxide thickness equal to 5 nm. The flat-band voltage V_{FB} is supposed to be equal to 0.6 V and the temperature equal to be 300 K. The reader can make use of the toolbox to run additional 'experiments', like those of Annex 3, which examine the impact of technology and temperature on transistor's performances.

2.4.1 The $I_D(V_D)$ Characteristics

The curves displayed in Fig. 2.2 show drain currents versus the drain voltage characteristics obtained by means of the program below making use of two additional MATLAB function, pMat and IDsh, reported in the toolbox. The unusual semilog

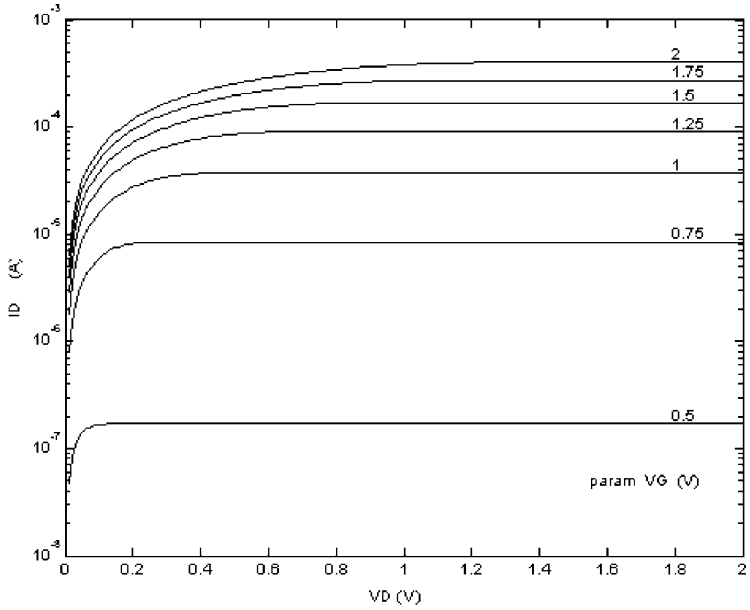

Fig. 2.2 Drain current versus drain voltage obtained by means of the *IDsh* file (MATLAB fig022.m)

vertical scale used for the display is chosen in order to plot drain currents from weak to strong inversion in a single diagram encompassing five orders of magnitude.

```
clear
clf
% data techno
T = 300;
N = 1e17;
tox = 5;
VFB = .6;

% compute pMat(technology vector)
p = pMat(T,N,tox);

% compute ID(VD)
VS = 0;
M = 201; VD = linspace(.01,2,M).';
UG = linspace (2,.5,7);
for k = 1: length(UG),
     ID(:,k) = IDsh(p,VS,VD,UG(1,k) + VFB);
end
% plot
semilogy(VD,ID,'k'); axis([0 2 1e-8 1e-3]);
```

A series of well-known facts are clearly visible:

1. The Charge Sheet Model represents drain currents in a smooth way all over the so-called linear (resistive) and saturated modes of operation. The model is 'continuous'. In other words it does not require several equations to describe distinct modes of operation.
2. The passage from strong to weak inversion and vice – versa is gradual and continuous too.
3. The distances between adjacent $I_D(V_D)$ characteristics gets larger as one goes from strong to weak inversion. Since all gate voltage increments are identical, the transconductance over drain current ratio is larger in weak than in strong inversion (remind weak and moderate inversion conditions achieve better gains).
4. The pinch-off voltage is very small in weak inversion and remains quasi-constant throughout the weak inversion regime. It is of the order of 100 mV, similar to the saturation voltage of bipolar transistors.
5. Drain currents in saturation are quasi-constant for the C.S.M. ignores effects like channel length modulation and DIBL. The transistor behaves like a perfect current source.

2.4.2 The $I_D(V_G)$ Characteristic of the Saturated Transistor

Figure 2.3 shows the drain current versus the gate voltage of the same transistor as above when saturated (the drain voltage V_D has no influence on the drain current). The almost linear section left attests clearly that below 0.5 V (weak inversion) the

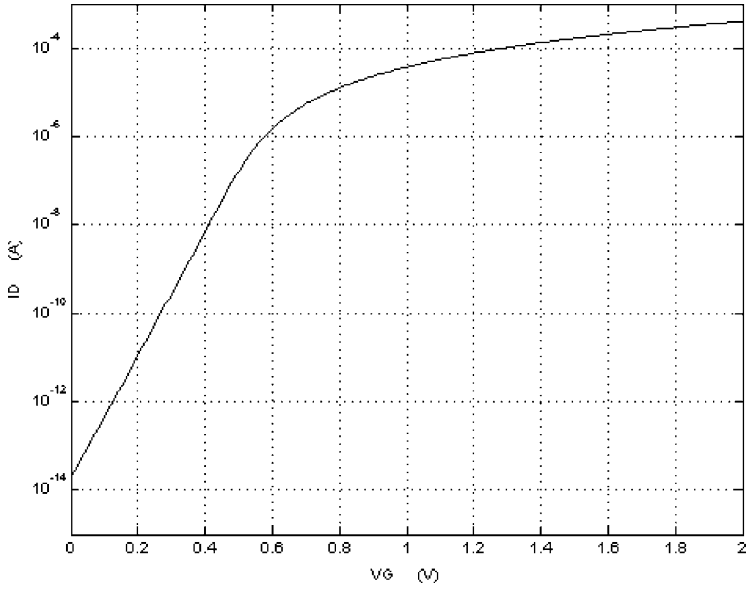

Fig. 2.3 Drain current of the saturated common source transistor (MATLAB fig023.m)

drain current increases quasi-exponentially. In this region, the '*subthreshold*' slope S determines the so-called slope factor n:

$$n = \frac{S}{U_T \log(10)} \tag{2.21}$$

Beyond the exponential, the drain current levels off gradually while the transistor is entering moderate and strong inversion. The trend in the strong inversion region is quadratic.

2.4.3 Drift and Diffusion Contributions to the Drain Current

The C.S.M. offers the possibility to compare the contributions of drift and diffusion currents to the drain current. All what is needed therefore is to break the polynomial representation of I_D of Eq. 2.19 into two parts. For the diffusion current, the two last terms of Eq. 2.17 are considered and for the drift current what remains. The polynomials are respectively:

$$P_{diffusion} = [0 \quad 0 \quad U_T \quad \gamma\, U_T \quad 0] \tag{2.22}$$

and

$$P_{drift} = \left[-\frac{1}{2} - \frac{2}{3}\gamma \quad V_G \quad 0 \quad 0\right] \tag{2.23}$$

The drift and diffusion currents displayed in Fig. 2.4 show clearly the dominance of one current over the other depending on which mode of operation is taking the lead. Diffusion dominates in weak inversion while drift takes over in strong inversion. In the middle, around 0.6 V, drift and diffusion currents have almost the same magnitudes. In strong inversion, the total current coincides practically with the quadratic approximation of I_D. The same holds true for the exponential current in weak inversion. Many analog circuits, especially low-power low-voltage circuits, operate nowadays in the so-called moderate inversion region.

2.5 Weak Inversion Approximation of the Charge Sheet Model

The fact that diffusion current overwhelms drift current in weak inversion leads to a number of useful approximate expressions. Because the first of the two right terms of Eq. 2.6 can be ignored, one has:

$$I_D\, dx \approx -\mu\, C'_{ox} W\, U_T\, d\left(-\frac{Q'_i}{C'_i}\right) \tag{2.24}$$

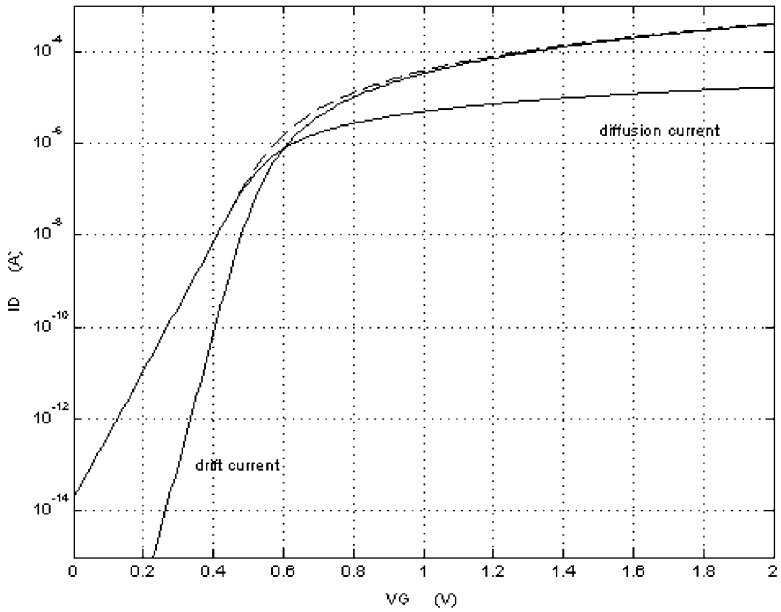

Fig. 2.4 Same as Fig. 2.3 with explicit representations of the drift and diffusion currents (MATLAB fig024.m)

Consequently, the drain current in weak inversion is given by:

$$I_D \approx -\mu\, C'_{ox} \frac{W}{L}\, U_T \left[\left(-\frac{Q'_{iD}}{C'_{ox}} \right) - \left(-\frac{Q'_{iS}}{C'_{ox}} \right) \right] \tag{2.25}$$

Let us find now an approximate expression of Q'_i/C'_{ox} in weak inversion. The inversion layer charge density is extracted from the equality:

$$-\frac{Q'_i}{C'_{ox}} = -\frac{Q'_t}{C'_{ox}} + \frac{Q'_b}{C'_{ox}} \tag{2.26}$$

where Q'_t/C'_{ox} and Q'_b/C'_{ox} are replaced by Eqs. 2.9 and 2.12. This leads to:

$$-\frac{Q'_i}{C'_{ox}} = \gamma \cdot \left[U_T \exp\left(\frac{\psi_S - 2\phi_B - V}{U_T} \right) + \psi_S \right]^{1/2} - \gamma \sqrt{\psi_S} \tag{2.27}$$

Since the contribution of the first of the two terms under the square root (drift current) is small compared to that of the second (diffusion current), the equation above can be approximated as follows:

$$-\frac{Q'_i}{C'_{ox}} = \gamma \sqrt{small + \psi_S} - \gamma \sqrt{\psi_S} \approx \gamma \frac{small}{2\sqrt{\psi_S}} \tag{2.28}$$

This leads to:

$$-\frac{Q'_i}{C'_{ox}} \approx \gamma \frac{U_T}{2\sqrt{\psi_S}} \exp\left(\frac{\psi_S - 2\phi_B}{U_T}\right) \cdot \exp\left(-\frac{V}{U_T}\right) \tag{2.29}$$

The surface potential ψ_S depends practically only on the gate voltage. In weak inversion, Eq. 2.14 boils down indeed to a second order equation relating the gate voltage V_G to ψ_S for Q'_i/C'_{ox} is small in comparison to the contribution of the depletion layer represented by the two last terms. An expression of the weak inversion surface potential ψ_{Swi} can be extracted then from the latter:

$$\psi_{Swi} = \left[-\frac{\gamma}{2} + \sqrt{\left(\frac{\gamma}{2}\right)^2 + V_G}\right]^2 \tag{2.30}$$

When ψ_{Swi} is put in Eq. 2.29 and the latter combined with Eq. 2.25, the next expression of the drain current in weak inversion is obtained:

$$I_D \approx \underbrace{\frac{1}{2}\beta\gamma\, U_T^2 \frac{1}{\sqrt{\psi_{Swi}}} \exp\left(\frac{\psi_{Swi} - 2\phi_B}{U_T}\right)}_{A} \cdot \left[\exp\left(-\frac{V_S}{U_T}\right) - \exp\left(-\frac{V_D}{U_T}\right)\right] \tag{2.31}$$

This is an interesting result for it shows that the drain current in weak inversion is controlled exponentially by the source and drain voltages owing to the fact that the factor A depends only on the gate voltage. Another interesting observation concerns the drain voltage when the transistor enters saturation. Rewriting Eq. 2.31 in terms of the drain-to-source voltage difference V_{DS} turns the above expression into:

$$I_D \approx A \cdot \exp\left(-\frac{V_S}{U_T}\right) \cdot \left[1 - \exp\left(-\frac{V_{DS}}{U_T}\right)\right] \tag{2.32}$$

The drain current saturates as soon as the drain-to-source voltage attains 100 mV (nearly four times U_T). The impact of the gate voltage is more difficult to apprehend for it is hidden in the A factor, which depends on the geometry via β, and γ, ϕ_B and the surface potential. The point is discussed more in detail further.

2.6 The g_m/I_D Ratio in the Common Source Configuration

An analytic expression of the transconductance over drain current ratio cannot be derived from the Charge Sheet Model. The ratio must be evaluated numerically by taking the derivative with respect to the gate voltage of the log of the drain current:

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{\partial \log(I_D)}{\partial V_G} \tag{2.33}$$

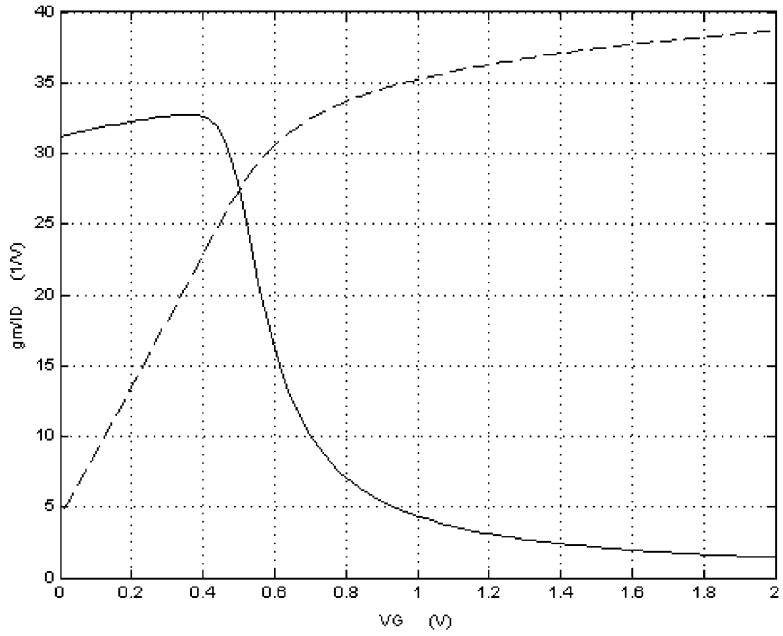

Fig. 2.5 The g_m/I_D ratio derived from the $I_D(V_G)$ plot of Fig. 2.4, which is reproduced in the background (MATLAB fig025.m)

The g_m/I_D ratio is shown in Fig. 2.5. It is larger in weak than in strong inversion but displays a slightly decaying trend under very small currents. The phenomenon can be explained as follows. Consider the derivative versus the gate voltage of the expression hereafter extracted from Eq. 2.31:

$$\left(\frac{g_m}{I_D}\right)_{W.I.} \approx \frac{\partial}{\partial V_G} \log\left[\frac{1}{\sqrt{\psi_{Swi}}} \exp\left(\frac{\psi_{Swi} - 2\phi_B}{U_T}\right)\right] \tag{2.34}$$

The derivative is done into two steps, first with respect to V_G, second to ψ_{Swi}:

$$\left(\frac{g_m}{I_D}\right)_{W.I.} \approx \left(-\frac{1}{2\,\psi_{Swi}} + \frac{1}{U_T}\right) \frac{\partial \psi_{Swi}}{\partial V_G} \tag{2.35}$$

When the derivative of the weak inversion surface potential with respect to the gate voltage is extracted from Eq. 2.30, one has:

$$\left(\frac{g_m}{I_D}\right)_{W.I.} = \frac{1}{UT} \cdot \frac{1 - \frac{U_T}{2\psi_{Swi}}}{1 + \frac{\gamma}{2\sqrt{\psi_{Swi}}}} \tag{2.36}$$

Notice the similarity with the approximate g_m/I_D ratio of Eq. 1.13 in the first chapter, stating that:

$$\left(\frac{g_m}{I_D}\right)_{W.I.} = \frac{1}{n\,U_T} \tag{2.37}$$

The comparison of Eq. 2.36 with 2.37 brings about an interesting analytical expression of the weak inversion subthreshold slope factor, called n_{wi}:

$$n_{wi} = \frac{1 + \frac{\gamma}{2\sqrt{\psi_{Swi}}}}{1 - \frac{U_T}{2\psi_{Swi}}} \tag{2.38}$$

The signification of n_{wi} gets clear when several g_m/I_D plots are merged as their source voltages changes. Figure 2.6 shows clearly that when the transistor enters weak inversion, all g_m/I_D ratios come together forming a single consolidated envelope, which coincides with Eq. 2.36.

Near the origin, the envelope bends down more rapidly for the width of the depleted region under the gate is getting smaller as the source voltage decreases. The ratio of the capacitive divider formed by the gate oxide and the depleted region increases, modifying consequently the slope factor n_{wi}.

One may substitute a more compact and more familiar expression to Eq. 2.31:

$$I_D \approx \underbrace{I_o \exp\left(\frac{V_G}{n_{wi}U_T}\right)}_{A} \cdot \left[\exp\left(-\frac{V_S}{U_T}\right) - \exp\left(-\frac{V_D}{U_T}\right)\right] \tag{2.39}$$

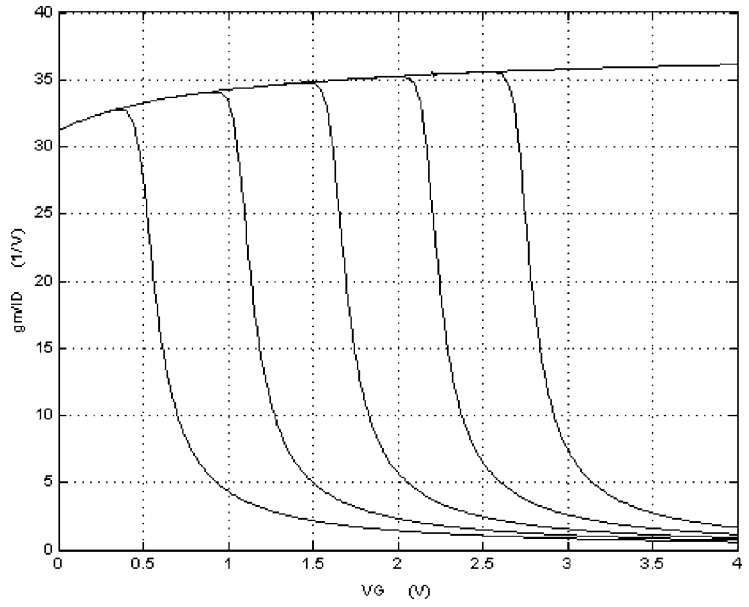

Fig. 2.6 Plot of g_m/I_D ratios when the source voltage changes from 0 V (*left*) to 2 V (*right*) in steps 0.5 V wide. The distance separating g_m/I_D's is a little more than 0.5 V owing to the body-effect discussed more in detail in the next chapter (MATLAB fig026.m)

2.7 Common Gate Characteristics of the Saturated Transistor

Let us consider now the common-gate configuration. The gate voltage is fixed while the source V_S is the input now. Figure 2.7 shows the $I_D(V_S)$ curve obtained after running the same file as above when the gate voltage is equal to 2 V and the source voltage V_S varies from 0 to 2 V. The drain voltage is supposed to be large enough in order to keep the transistor saturated under any circumstance. As V_S increases, the gate-to-source voltage V_{GS} decreases abating the drain current. First, the drain current slows down gradually for the transistor is still in strong inversion. Once the transistor is in weak inversion, the current decreases exponentially. In this region, the slope of the drain current follows the $\exp(V_S/U_T)$ law predicted by Eq. 2.31. Put differently, the slope factor is equal to one in strong contrast with the slope factor of the common source slope factor.

The same plot shows also the g_{ms}/I_D ratio inferred from the drain current characteristic. Like in the common-source configuration, the ratio is given by the slope of the semilog-scaled drain current. The 'transconductance' is now g_{ms} instead of g_m. The sequence is being reversed with respect to the common-source configuration for the g_{ms}/I_D is flipped horizontally with respect to g_m/I_D.

In weak inversion, the g_{ms}/I_D ratio is equal to $1/U_T$ in accordance with the unity slope factor mentioned above. This once again underlines the similarity MOS

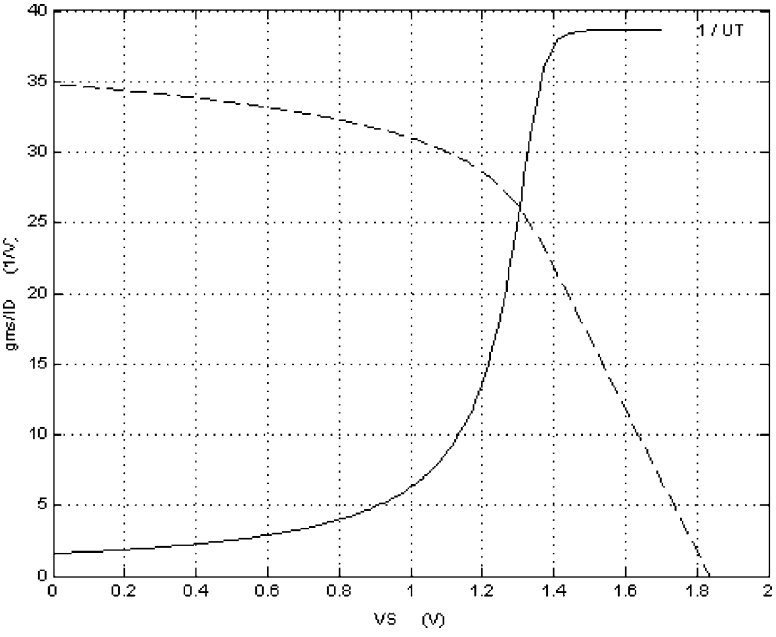

Fig. 2.7 The g_{ms}/I_D ratio (*plain lines*) versus the source voltage is obtained by taking the derivative of the log scaled drain current plotted in *dashed lines* (V_G is equal to 2 V) (MATLAB fig027.m)

transistors share with bipolar transistors when operating in weak inversion. Two reasons explain this. First, the drain current is dominated by diffusion current as in the neutral base of the bipolar transistor. Second, the front and back gates co-operate whereas the back-gate remains idle in the common source configuration. The common-gate configuration ignores consequently the partitioning inherent to the common-source configuration.

We will show in later chapters that real transistors do not conform to the unity slope factor in weak inversion in the common-gate configuration. The slope factor is generally slightly larger than one. This is due to the drain-to-source voltage variation going along with the gate-to-source voltage modifications. In the C.S.M. the drain voltage has no effect on the current as long as the transistor is saturated, but with real transistors, changes of the drain voltage modify the space charge near the drain and below the inversion layer. The drain influences thus the current even though the transistor is saturated. The g_{ms}/I_D ratio of real transistors in weak inversion is smaller thus than the predicted $1/U_T$.

2.8 A Few Concluding Remarks Concerning the C.S.M.

The Charge Sheet Model is a physical model that predicts drain currents whatsoever mode of operation, weak or strong inversion, saturation or not. It is relevant and particularly instrumental for understanding the basic mechanisms controlling low-power operation. In addition, the model bridges drain currents to physical quantities such as the substrate impurity concentration, oxide thickness and temperature. It offers therefore the possibility to scrutinize sensitivity aspects. The validity of the C.S.M. is restricted however to ideal transistors implemented in a uniformly doped substrate with gate lengths sufficiently large to obliterate short channel effects.

An interesting observation can be made as far as the *threshold voltage*. So far, the concept has not been mentioned except occasionally, for instance when the quadratic model was considered. The Charge Sheet Model ignores actually the concept. The reason is that the threshold voltage is not a physical quantity but a parameter embodied on measurements. Its interpretation varies according to the evaluation techniques. This does not mean that the threshold voltage is a useless concept. On the contrary, it is a landmark, like the voltage drop across forward biased junctions. It is an essential parameter exploited in every circuit oriented model. In the next chapter, we are going to clarify the concept.