Chapter 4
Coplanar Waveguide Transmission Line

The objective of this chapter is to investigate silicon-core (Si-core) metal-coated coplanar waveguide transmission (CPW) line [1]. The Si-core CPW is designed, fabricated, and experimented. Then, attenuation related to different substrate materials, core materials, and fabrication processes are analyzed. The experimental results show that the Si-core CPW supports quasi-TEM mode propagation up to 25 GHz with attenuation less than 4 dB/cm.

4.1 Design of the Si-Core CPW

The geometry of the Si-core CPW is similar to the conventional thin film CPW as shown in Fig. 4.1. It consists of three parallel plate waveguides. In this structure, each waveguide of the Si-core CPW is formed from a single-crystal silicon plate with thickness of 35–75 μm which is coated with a thin layer of metal on the top and sidewalls. RF signal can then propagate along the metal on the top surface and also along sidewalls of the transmission line. The core material can either be low-resistivity silicon ($\rho \leq 10\ \Omega$ cm) or high-resistivity silicon ($\rho \geq 1000\ \Omega$ cm). The substrate can be either Si on glass (SiOG) or high-resistivity silicon in silicon on insulator (SOI). The recesses formed in the substrate under waveguides serve three purposes: (1) to help the release of movable structures in the RF MEMS circuits; (2) to avoid metal connection to short circuit after metal coating; and (3) to reduce the dielectric loss of the transmission line.

The characteristic impedance of CPW depends significantly on its geometrical parameters, including the center conductor width, S, the ground width, G, and the conductor separation, W, and the substrate material properties, such as the substrate thickness, H, and the relative permittivity, ε_r. In the Si-core CPW, other process parameters also affect the characteristic impedance. These include the thickness, T, and the resistivity, ρ, of the core material, the depth of the recesses, h_r, the undercut width, w_r, the thickness of the metal on the top, t_t, and at sidewalls, t_s.

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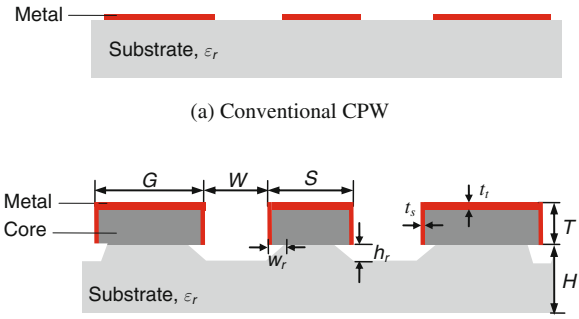


(a) Conventional CPW

(b) Si-core CPW

Fig. 4.1 Schematic cross-sectional view of the CPW. Copyright/used with permission of/courtesy of Institute of Physics and IOP Publishing Limited

The design of the Si-core CPW involves three steps. First, based on the process requirements, some parameter values are determined such that the thickness of the glass substrate $H = 500$ μm, the permittivity of the glass substrate $\varepsilon_r = 4.6$, the thickness of the silicon core $T = 50$–80 μm, and the recess parameters $w_r = 1.6h_r$ to $1.8h_r$. To accommodate 150-μm-pitch ground–signal–ground coplanar probes, the distance between the two ground lines ($S + 2W$) is 200 μm and the ground line width, G, falls within the range of 100–400 μm. Second, the characteristic impedance, Z_0, for the normal finite CPW [2] can be expressed as

$$Z_0 = \frac{40\pi}{\sqrt{\varepsilon_{\text{eff}}}} \frac{K(k_1)}{K(k_1')} \tag{4.1a}$$

where

$$\varepsilon_{\text{eff}} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k_2')K(k_1)}{K(k_2)K(k_1')} \left[1 + \frac{T}{2W} \frac{K(k_1)}{K(k_1')}\right] + \frac{T}{2W} \frac{K(k_1)}{K(k_1')} \left[2 + \frac{T}{2W} \frac{K(k_1)}{K(k_1')}\right] \tag{4.1b}$$

$$k_1 = \frac{S + 2W + 2G}{S + 2W} \sqrt{\frac{(S + 2W)^2 - S^2}{(S + 2W + 2G)^2 - S^2}} \tag{4.1c}$$

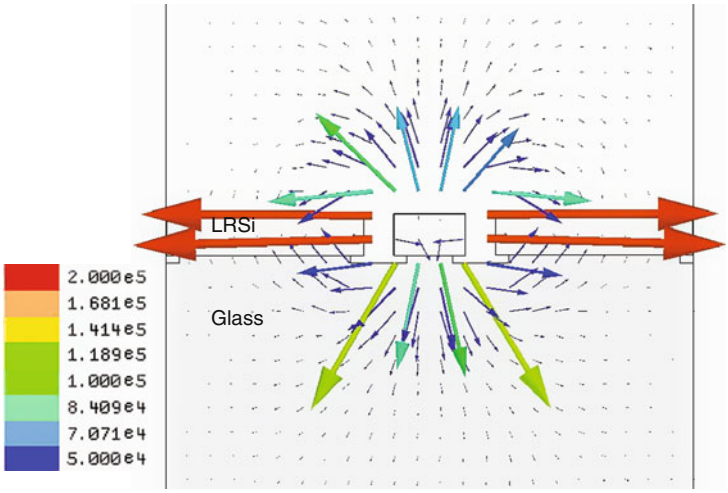
$$k_2 = \frac{\sinh\left[\frac{\pi(S+2W+2G)}{4H}\right]}{\sinh\left[\frac{\pi(S+2W)}{4H}\right]} \sqrt{\frac{\sinh\left[\frac{\pi(S+2W)}{4H}\right] - \sinh\left(\frac{\pi S}{4H}\right)}{\sinh\left[\frac{\pi(S+2W+2G)}{4H}\right] - \sinh\left(\frac{\pi S}{4H}\right)}} \tag{4.1d}$$

$$k_n' = \sqrt{1 - k_n^2}, \quad n = 1, 2 \tag{4.1e}$$

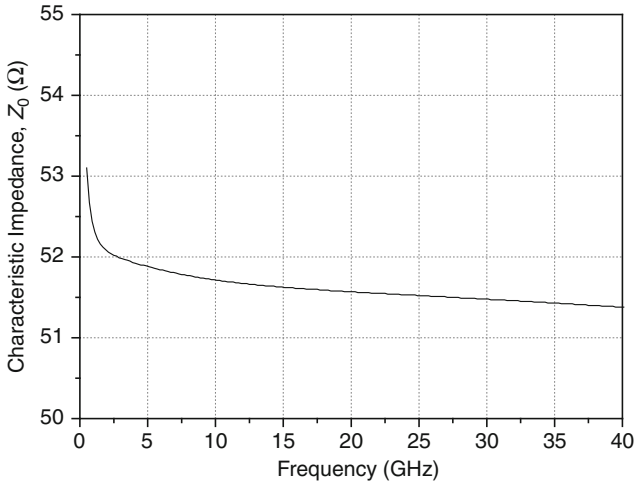
where K is the complete elliptic integrals of the first kind and ε_{eff} is the effective relative permittivity. The center conductor width, S, and the conductor separation, W, can be used to determine the required characteristic impedance. The dimension

values of the center conductor width, S, the ground width, G, and the conductor separation, W, can be determined using three-dimensional (3D) finite-element method (FEM) simulation.

Figure 4.2a shows the electric field (E-field) distribution of the Si-core CPW at 20 GHz. The electric field radiates from the center signal conductor to the two ground conductors. The dominant mode of the transmission line is quasi-transverse



(a)



(b)

Fig. 4.2 (**a**) Vector E-field distribution and (**b**) characteristic impedance of the Si-core CPW ($S/W/G = 110/45/300$ μm, $h_r = 12$ μm, $w_r = 20$ μm). Copyright/used with permission of/courtesy of Institute of Physics and IOP Publishing Limited

electromagnetic (TEM) mode, which is similar to the conventional thin film CPW transmission line. It is found that there is strong penetration of the E-field into the substrate and the silicon core. Therefore, the material properties of the substrate and the core have significant effects on the performance of the Si-core CPW. The simulated characteristic impedance versus frequency of a Si-core CPW is shown in Fig. 4.2b. The characteristic impedance of this Si-core CPW is 51.3–52 Ω when the dimension values of CPW *S*/*W*/*G* are equal to 110/45/300 μm, $h_r = 12$ μm, $w_r = 20$ μm, $T = 50$ μm, $H = 500$ μm, $\varepsilon_r = 4.6$, $t_t = 1$ μm, and $t_s = 0.5$ μm, respectively. The characteristic impedance decreases with frequency slowly.

4.2 Losses of the Si-Core CPW

The attenuation, α, is an important characteristic indicating the efficiency of the coplanar lines' transmit power. The attenuation of the Si-core CPW consists of three losses, namely conductor loss, α_c, dielectric loss, α_d, and radiation loss, α_r.

4.2.1 Conductor Loss

The conductor loss, α_c, resulting from the finite conductivity of the metal, in Np/cm is given by

$$\alpha_c = \frac{R}{2Z_0} \tag{4.2}$$

where R is the unit resistance of the transmission line. Therefore, the conductor loss is determined by the line unit resistance and the characteristic impedance. Decreasing the line unit resistance or increasing the line characteristic impedance can reduce the conductor loss. Figure 4.3 shows the conductor loss, α_c, as a function of the transmission line unit resistance, R, under different characteristic impedances, Z_0. When $Z_0 = 50$ Ω and $R = 40$ Ω/cm, the conductor loss is 3.5 dB/cm. When Z_0 decreases to 42 Ω, the conductor loss increases to 4.1 dB/cm.

In the Si-core CPW, the transmission line unit resistance, R, is determined by the metal resistance of the signal line, $R_{s,m}$, and ground lines, $R_{g,m}$. They are expressed as

$$R_{s,m} = \begin{cases} R_{s,dc} = \frac{1}{\sigma(2t_sT + t_tS)} & \left(\text{if } R_s(f) \le R_{s,dc}\right) \\ R_s(f) = \frac{1}{\sigma\delta_s\left[2T\left(1-e^{-t_s/\delta_s}\right)+S\left(1-e^{-t_t/\delta_s}\right]\right.} & \left(\text{if } R_s(f) > R_{s,\,dc}\right) \end{cases} \tag{4.3a}$$

$$R_{g,m} = \begin{cases} R_{g,dc} = \frac{1}{\sigma(2t_sT + t_tG)} & \left(\text{if } R_g(f) \le R_{g,dc}\right) \\ R_g(f) = \frac{1}{\sigma\delta_s\left[2T\left(1-e^{-t_s/\delta_s}\right)+G\left(1-e^{-t_t/\delta_s}\right]\right.} & \left(\text{if } R_g(f) > R_{g,dc}\right) \end{cases} \tag{4.3b}$$

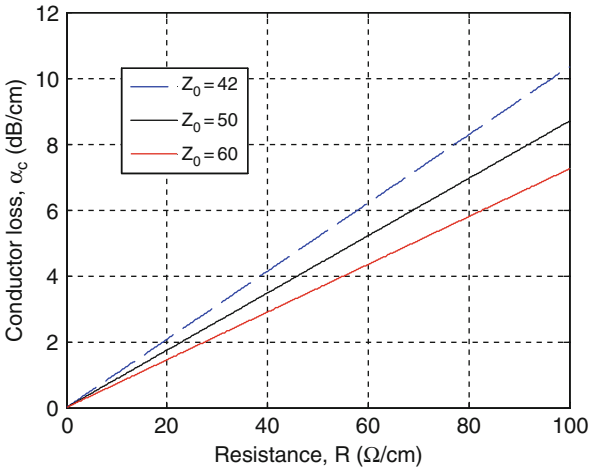


Fig. 4.3 Conductor loss with respect to different line unit series resistances and characteristic impedances

where T and S are the thickness and the width of the signal line; t_s and t_t are the metal thickness on the top and sidewalls of the transmission line, as shown in Fig. 4.1b; σ is the conductivity of the metal and δ_s is the skin depth, which is determined by Eq. (2.5). At low-frequency range, the resistance is determined by the DC resistance, $R_{s,dc}$ and $R_{g,dc}$. However, when the frequency increases, the current is crowded outside the surface of the conductor. The line resistance is determined by the $R_s(f)$ and $R_g(f)$ at high-frequency range.

4.2.2 Dielectric Loss

The dielectric loss, α_d, is due to the displacement current in the guiding medium of the transmission line. The dielectric loss, α_d, in Np/cm is given by [3]

$$\alpha_d = \frac{1}{2} G Z_0 = \frac{\omega\sqrt{\mu_0 \varepsilon_0 \varepsilon_r}\tan\delta}{2} \times \frac{1}{100} \tag{4.4a}$$

where $\tan\delta$ is the loss tangent of the guiding medium. The loss tangent specifies the lossy nature of the dielectric material and is defined as

$$\tan\delta = \frac{\sigma_d}{\omega \varepsilon_0 \varepsilon_r} \tag{4.4b}$$

where σ_d is the electrical conductivity of the dielectric material. Table 4.1 provides the material properties of four dielectric materials used in this study and their dielectric loss at 20 GHz. The dielectric loss is air, glass, high-resistivity silicon (HRSi), and low-resistivity silicon (LRSi).

Table 4.1 Dielectric properties of the fabrication materials

Material	ε_r	tan δ	σ_d (S/m)	α_d (dB/cm)
Glass	4.6	0.003	–	0.12
HRSi	11.9	–	0.05	0.24
LRSi	11.9	–	100	474.30
Air	1.0	0	–	0

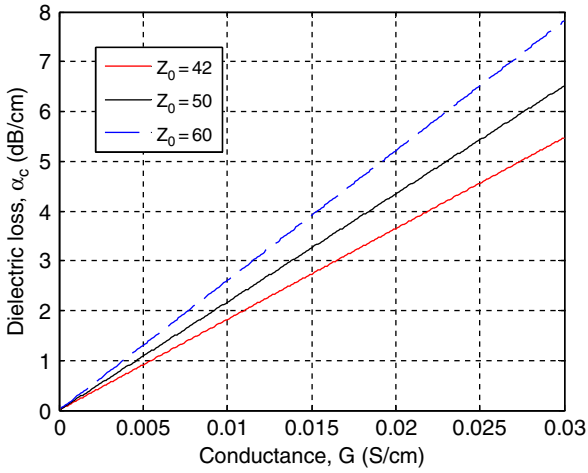


Fig. 4.4 Conductor loss with respect to different line unit shunt conductances and characteristic impedances

Figure 4.4 shows the dielectric loss, α_d, as a function of the unit shunt conductance, G, with the characteristic impedance, Z_0, as a parameter. The dielectric loss increases with the unit conductance and the characteristic impedance. When $Z_0 = 50\ \Omega$ and $G = 0.005$ S/cm, the dielectric loss is 1.08 dB/cm. When G increases to 0.02 S/cm, the dielectric loss increases to 4.34 dB/cm.

4.2.3 Radiation Loss

In addition to the conductor loss and the dielectric loss, radiation from unwanted parasitic modes and coupling of power to surface waves contribute to radiation loss, α_r. The parasitic mode in the CPW is the odd mode with anti-phase voltages in the two slots, which is excited at the discontinuities. Radiation from this mode can be minimized by maintaining the symmetrical structure of the circuits and avoiding its excitation by using air bridges or bond wires at periodic intervals. For the CPW with a finite substrate thickness, the surface wave modes of the substrate are also responsible for the leakage. Surface waves are the guided modes of a dielectric slab

with finite thickness. Excitation of surface modes depends on the polarizations and symmetries of the transmission line.

Figure 4.5 shows the radiation loss, α_r, as a function of frequency, f, with the substrate permittivity, ε_r, as a parameter. In this scenario, $H = 500$ μm, $S = 110$ μm, $W = 45$ μm, and $G = 300$ μm. It shows that the radiation loss is substantially affected by the permittivity of the substrate at high-frequency range. The higher the permittivity, the faster the increase of radiation loss with frequency. For instance, when $\varepsilon_r = 4.6$ (glass) at 40 GHz, the radiation loss of the substrate is 0.006 dB/cm. When $\varepsilon_r = 11.9$, the radiation loss of the substrate increases to 0.046 dB/cm. However, compared with the conductor loss and the dielectric loss, the radiation loss is negligible when frequency is below 40 GHz. The radiation losses dominate for frequencies over 200 GHz for coplanar lines with dimensions of the order of a few tens of microns, as demonstrated in the experiments [4].

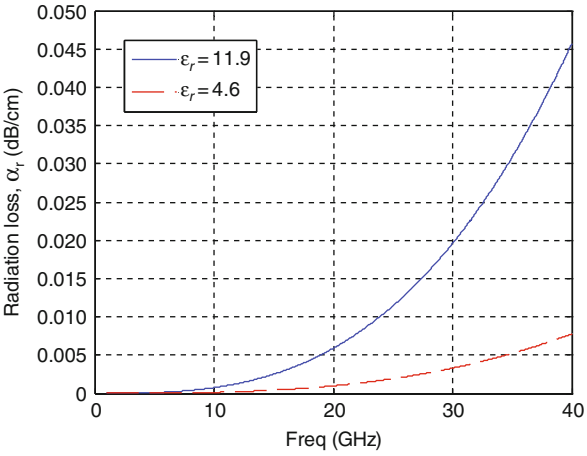


Fig. 4.5 Radiation loss curves with respect to different frequencies and substrate permittivities

4.3 Effect of Material Properties and Fabrication Processes

Factors affecting the RF properties of the Si-core CPW are studied in this section. These factors include the substrate material, the core material, and the fabrication process.

4.3.1 Effect of Different Substrate Materials

Figure 4.6 shows the simulation results of the Si-core CPW on glass and on high-resistivity silicon substrate. The core material is the low-resistivity silicon with

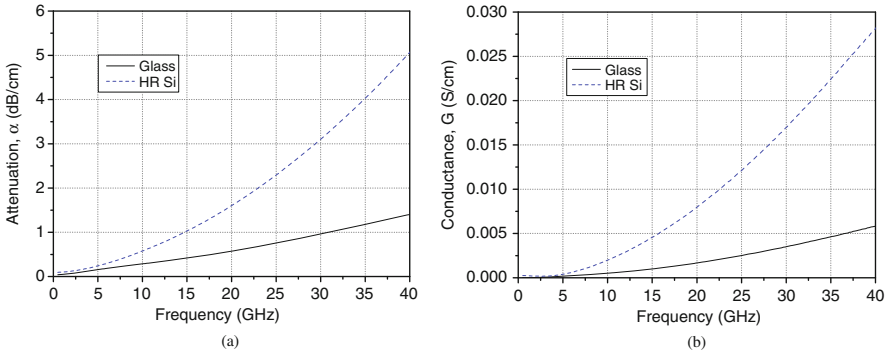


Fig. 4.6 Comparison of simulation results between the Si-core CPW on glass and HRSi substrate ($S/W/G = 110/45/300$ μm, $h_r = 12$ μm, and $w_r = 20$ μm, LRSi core): (**a**) attenuation and (**b**) shunt conductance G

$\rho = 1\ \Omega$cm . The attenuation, α, and the shunt conductance, G, are determined by S-parameters, since the substrate is the main contributory factor to the dielectric loss through the shunt conductance, G. Figure 4.6a shows that a 50-Ω Si-core CPW on the glass substrate has lower attenuation. According to the analysis in Section 4.2.2, the conductance, G, of the high-resistivity silicon is larger than the glass. When the frequency increases, the shunt conductance, G, on the HRSi substrate increases faster than the glass substrate as shown in Fig. 4.6b.

4.3.2 Effect of Different Core Materials

The effect of the core material is shown in Fig. 4.7. In the simulation models, the substrate is 500-μm-thick glass. $S/W/G$ are 110/45/300 μm. h_r, w_r, and T are 12, 20, and 50 μm, respectively. The characteristic impedance, Z_0, increases slightly from 48 to 50 Ω when the core material changes from the low-resistivity silicon to the high-resistivity silicon. The LRSi-core CPW has higher attenuation than the HRSi-core CPW. This difference becomes larger when the frequency increases.

The *RLGC* parameters of the Si-core CPW transmission lines have been extracted and compared in Fig. 4.8. Figure 4.8a shows that when the core resistivity of the Si-core CPW increases, the unit inductance, L, increases by only a small amount and the unit capacitance, C, decreases by only a small amount. Therefore, the characteristic impedance which is determined by $\sqrt{L/C}$ at high frequencies (>5 GHz) increases. The unit resistance, R, of the LRSi-core CPW is slightly lower than the HRSi-core CPW when the frequency is below 3 GHz as shown in Fig. 4.8b. The shunt conductance, G, of the LRSi-core CPW is significantly larger than that of the HRSi-core CPW, especially at high frequencies. This results in higher dielectric loss

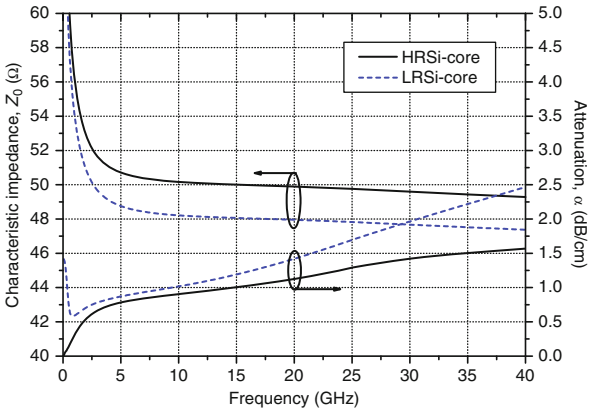


Fig. 4.7 Comparison of the RF properties of Si-core CPW with different core resistivities ($S/W/G = 110/45/300$ μm, $h_r = 12$ μm, and $w_r = 20$ μm). Copyright/used with permission of/courtesy of Institute of Physics and IOP Publishing Limited

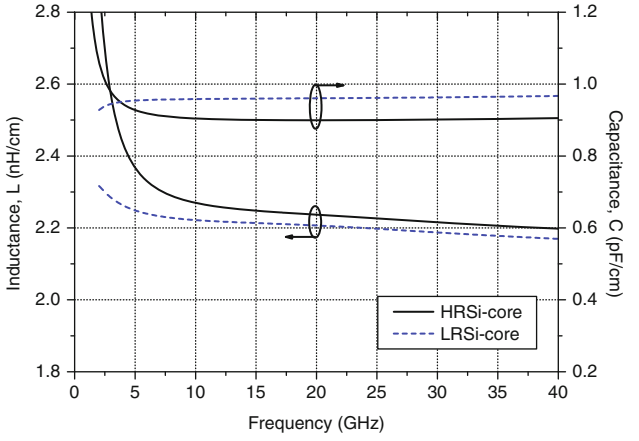
for LRSi-core CPW than HRSi-core CPW. Therefore, the attenuation of LRSi-core CPW is larger than the HRSi-core CPW.

4.3.3 Effect of Different Fabrication Processes

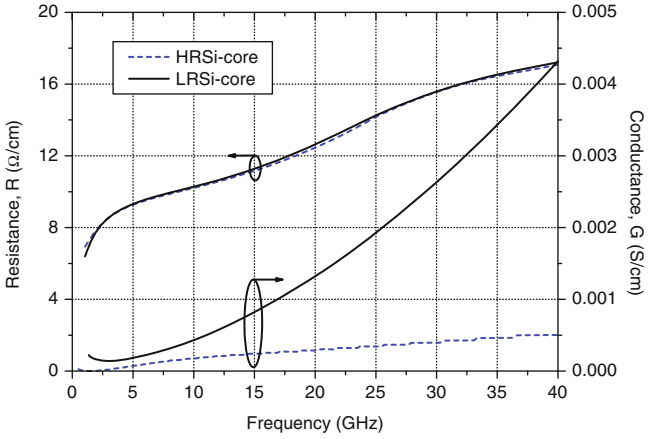
Besides the geometrical dimensions, the types of the substrate material, and the core material, the RF properties of the Si-core CPW are also affected by the variation in fabrication process. These include the thickness of the transmission line, T, the etching depth of the glass recesses, h_r, and the undercut width, w_r, as shown in Fig. 4.9.

The characteristic impedance, Z_0, of the Si-core CPW is reduced from 55 to 44 Ω when the transmission line thickness, T, increases from 50 to 80 μm, as shown in Fig. 4.10a. This is because when the line unit capacitance, C, increases the characteristic impedance reduces. Figure 4.10b shows that the attenuation slightly decreases with an increase in the conductor thickness. This is because the surface current is distributed in the larger area, which leads to the lower conductor loss.

Figure 4.11a, b shows that when the substrate is etched more, with larger w_r and h_r, the characteristic impedance of the Si-core CPW increases from 47.6 to 51.4 Ω, and the attenuation decreases slightly. This is because when the connection of the conductor to the substrate is smaller, there is smaller wave penetration into the substrate, which leads to smaller unit capacitance and smaller dielectric loss.



(a)



(b)

Fig. 4.8 Comparison of the distributed *RLGC* parameters of the Si-core CPW on glass substrate: (**a**) capacitance and inductance and (**b**) conductance and resistance

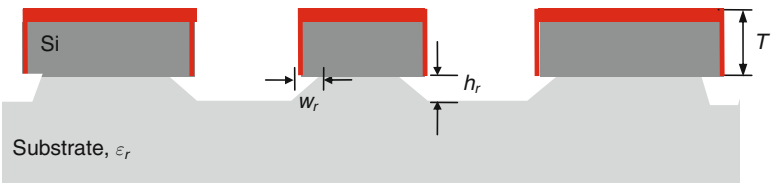
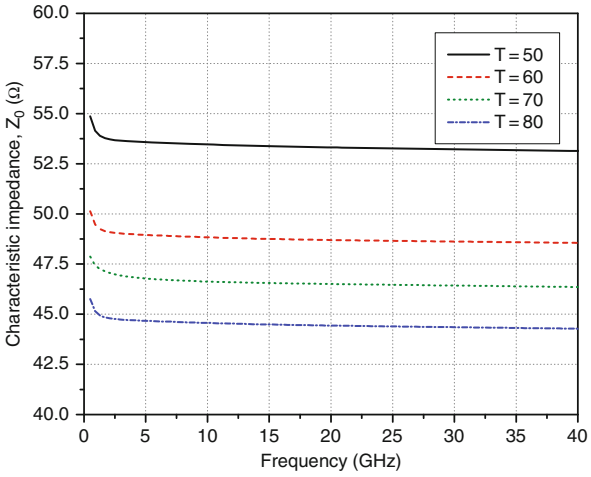
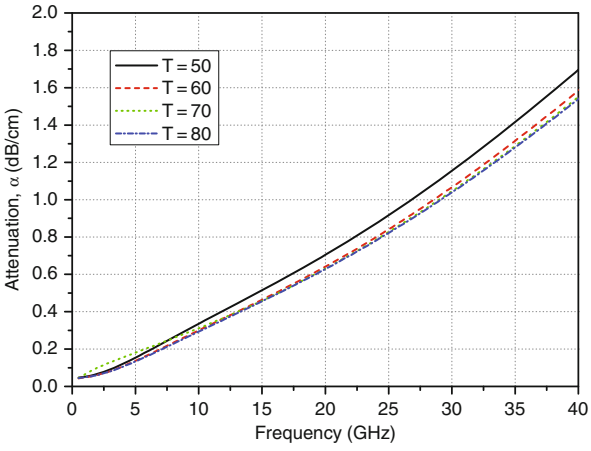


Fig. 4.9 Schematic of cross-sectional view of the Si-core CPW transmission line



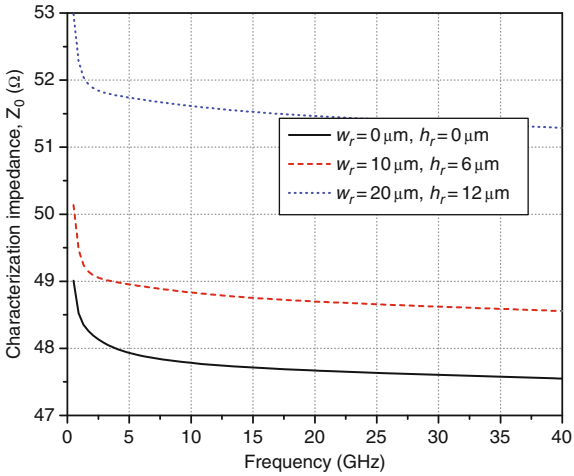
(a) Characteristic impedance



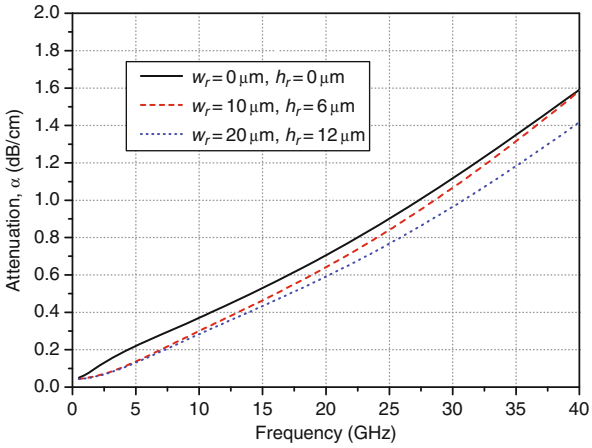
(b) Attenuation

Fig. 4.10 Simulation results of HRSi-core CPWs with various conductor thicknesses, T ($S/W/G$ = 110/45/300 μm)

The characteristic impedance of the Si-core CPW is significantly affected by the variation in the fabrication process. Therefore, the process control is important for the RF properties of the Si-core CPW, in particular the characteristic impedance, which determines the impedance matching of the RF circuits.



(a) Characteristic impedance Z_0



(b) Attenuation

Fig. 4.11 Simulation results of HRSi-core CPWs with various undercut dimensions ($S/W/G$ = 110/45/300 μm). Copyright/used with permission of/courtesy of Institute of Physics and IOP Publishing Limited

4.4 Experimental Results and Discussions

The RF responses of the Si-core CPW are measured using the HP 8510C Vector Network Analyzer with tungsten-tip 150-μm-pitch Cascade Microtech ground–signal–ground coplanar probes. The system is calibrated using the standard short-open-load-through (SOLT) on-wafer calibration technique. A 5-mm plastic plate is placed between the probe chuck and the sample to remove higher order modes of propagation. All experiments are performed in the room environment without any

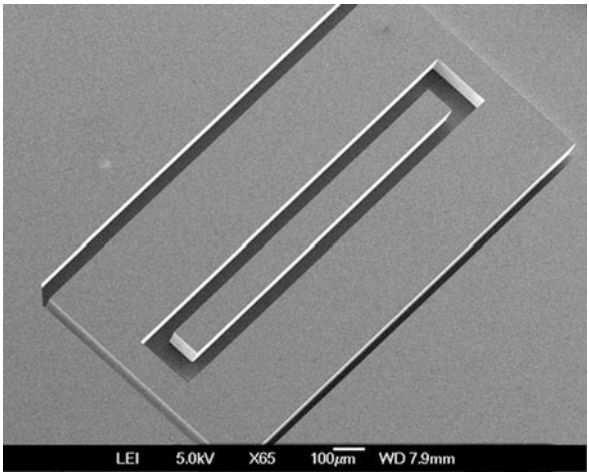


Fig. 4.12 SEM image of a 1-mm-long Si-core CPW transmission line

packaging. A SEM image of a Si-core CPW coated with 1-μm-thick gold (Au) is shown in Fig. 4.12. The thickness of the transmission line, T, is 62 μm and the length, L, is 1 mm.

4.4.1 Comparison Between Simulation Results and Measurement Results

Figure 4.13 shows the measurement results with the post-simulation results of a 1-mm-long HRSi-core CPW on glass. The *S*/*W*/*G* are 110/45/400 μm, respectively. The thickness of the transmission line is 62 μm. The glass cavity parameters, h_r and w_r, are about 6 and 10 μm, respectively. In the post-simulation model of HFSS, all geometrical parameters are set based on the experimental values. For example, the metal layer spread on glass has a thickness of 1 μm on the top and 0.3 μm on the sidewalls. Figure 4.13 shows that the simulation results are in good agreement with the measurement results. The characteristic impedance of the glass substrate, HRSi-core CPW is about 47 Ω when the frequency is above 10 GHz. The attenuation increases with frequency, which is 4 dB/cm at 25 GHz.

The unit *RLGC* parameters of simulation results and measurement results are compared in Fig. 4.14. The measured unit *RLGC* values match well with the simulated results. The unit inductance, L, and the unit capacitance, C, are kept constant from 10 to 25 GHz, which are 2.85 nH/cm and 1.3 pF/cm, respectively, as shown in Fig. 4.14a. The resistance, R, and shunt conductance, G, increase with the frequency, as shown in Fig. 4.14b. Table 4.2 compares simulated and measured attenuation due to the unit resistance, R, and the shunt conductance, G, of the HRSi-core CPW on glass at 20 GHz. The measured conductance, G, is 0.0017 S/cm, resulting in the

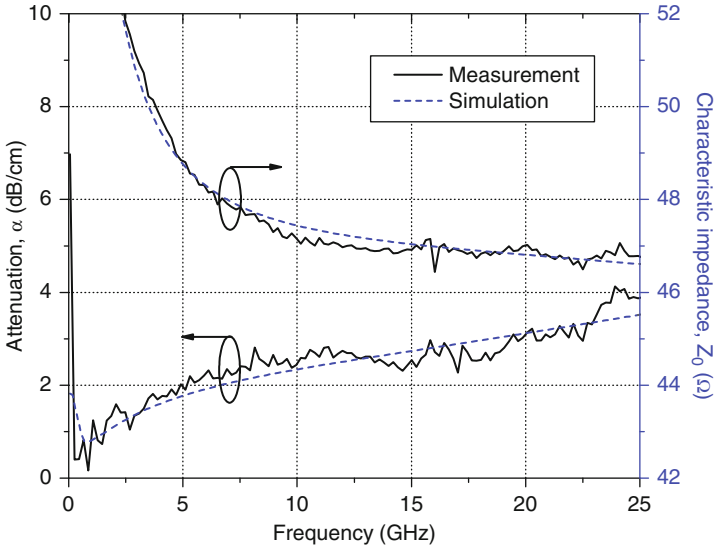


Fig. 4.13 Comparison of the measurement and the simulation results of an HRSi-core CPW on the glass substrate ($T = 62\ \mu$m, $h_r \approx 6\ \mu$m, $w_r \approx 10\ \mu$m, and 1-μm-thick Au coating). Copyright/used with permission of/courtesy of Institute of Physics and IOP Publishing Limited

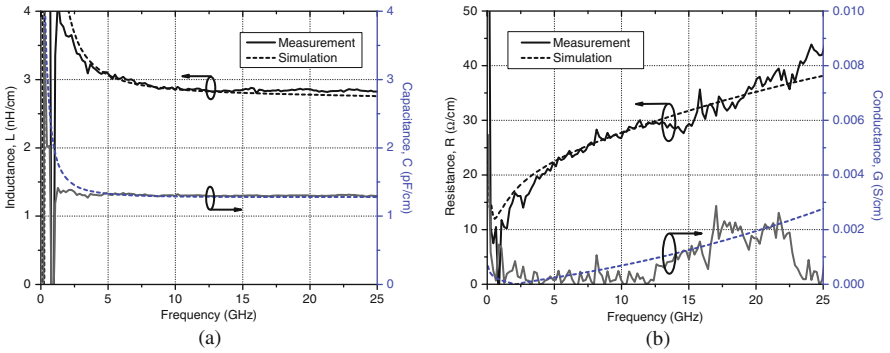


Fig. 4.14 Comparison of the measured and the simulated *RLGC* parameters of an HRSi-core CPW on a glass substrate: **(a)** *L* and *C*, and **(b)** *R* and *G*. Copyright/used with permission of/courtesy of Institute of Physics and IOP Publishing Limited

dielectric loss, α_d, of 0.34 dB/cm. The measured resistance, *R*, of 37.6 Ω/cm contributes to the conductor loss, α_c, of 3.48 dB/cm. The conductor loss is nine times higher than the dielectric loss. Therefore, the large unit resistance, *R*, is the dominant factor of the attenuation of the Si-core CPW.

By investigating the fabrication process in Chapter 5, the large unit resistance is due to low-quality metal deposition. The metal is deposited using E-beam evaporation. Generally, the E-beam evaporation has poor step coverage. The metal

Table 4.2 Comparison of the simulated and measured attenuation contributed by the unit resistance and the conductance of the glass-based HRSi-core CPW at 20 GHz

	Z_0 (Ω)	R (Ω/cm)	G (S/cm)	α_c (dB/cm)	α_d (dB/cm)	α (dB/cm)
Measurement	47.0	37.6	0.0017	3.48	0.34	3.82
Simulation	46.8	35.2	0.002	3.27	0.4	3.67

coated on sidewalls is found to be only 1/3 of the metal coated on the top surface. Therefore, only 3000–4000 Å gold can be coated on sidewalls when 1-μm-thick gold is deposited on the top of silicon structures. On the other hand, the surface current of the proposed Si-core CPW is mainly concentrated on sidewalls of the apertures, as shown in Fig. 4.2a. Therefore, more loss is caused by the thin metal coating of sidewalls. The increase of the shunt conductance, G, caused by the metal spreading on the substrate during E-beam evaporation is very small. Compared to the conductor loss, the dielectric loss is negligible.

4.4.2 Effect of Geometrical Parameters

The performance of the Si-core CPW depends on the geometrical parameters significantly, including the signal width, S, the ground width, G, and the conductor separation, W. Four 1-mm-long LRSi-core CPW with various $S/W/G$ are fabricated on glass and measured. Their $S/W/G$ parameters are summarized in Table 4.3. Note that $S+2W$ and G are the same for designs A, B, and C. Design D is optimized using Ansoft HFSS, whose simulated characteristic impedance is 50 Ω. The other parameters are $T \approx 50$ μm, $h_r \approx 6$ μm, and $w_r \approx 10$ μm.

Table 4.3 Geometrical parameters of four 1-mm-long Si-core CPWs

Design no.	Signal, S (μm)	Space, W (μm)	Ground, G (μm)	Sum, $S + 2W$ (μm)
A	680	10	150	700
B	300	200	150	700
C	60	320	150	700
D	110	45	400	200

The characteristic impedance, Z_0, and the attenuation, α, extracted from measured S-parameters are shown in Fig. 4.15a, b. The variation of the characteristic impedance of the Si-core CPW is larger when the frequency is below 5 GHz, indicating slow-wave mode propagation. However, when the frequency rises above 5 GHz, the characteristic impedance, Z_0, reduces gradually for all structures, indicating that the quasi-TEM mode propagation is supported above 5 GHz. In the quasi-TEM mode propagation, the characteristic impedance of the transmission line is inversely

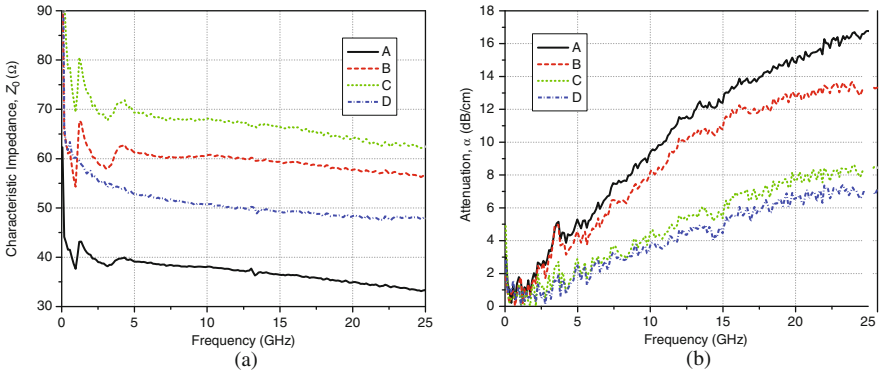


Fig. 4.15 Measured results of 1-mm-long LRSi-core CPWs on glass with different dimensions: (**a**) characteristic impedance and (**b**) attenuation

proportional to the square root of the line capacitance. When the space between the signal line and the ground line, *W*, is smaller, the unit inductance, *L*, is less and the unit capacitance, *C*, is larger, which lead to smaller characteristic impedance. This tendency can be observed in designs A, B, and C. At high frequency, impedance matching is important to minimize signal oscillations that are caused by the reflection of the electromagnetic wave at the impedance discontinuity. Therefore, it is most desirable to design the transmission line with the characteristic impedance of 50 Ω. The characteristic impedance of design D is about 50 Ω at 5–25 GHz. Figure 4.15b shows that the attenuation of the Si-core CPW increases with the signal line width, *S*. When (*S*+2*W*) is a constant, the Si-core CPW with wider signal line shows larger attenuation. That is because more electromagnetic field leaks into the substrate, e.g., dielectric loss is larger. However, design D (*S*/*W*/*G* = 110/45/400 μm) has lower attenuation than design C (*S*/*W*/*G* = 60/320/150 μm). That is because the sum (*S*+2*W*) of design C is larger than the glass substrate thickness of 500 μm, whereas the sum (*S*+2*W*) of design D is less than 500 μm. This leads to larger frequency dispersion and radiation loss in design C as compared to design D. Therefore, geometrical parameters of the Si-core CPW can be optimized to obtain the desired characteristic impedance and, simultaneously, suppress the unwanted radiation loss and the frequency dispersion when designing the Si-core CPW.

4.4.3 Effect of Material Properties

Both the substrate material and the core material affect the RF performance of the Si-core CPW. The effect of the substrate material is illustrated in Figs. 4.16 and 4.17. For the SOI-based LRSi-core CPW, the parameters of the CPW transmission line

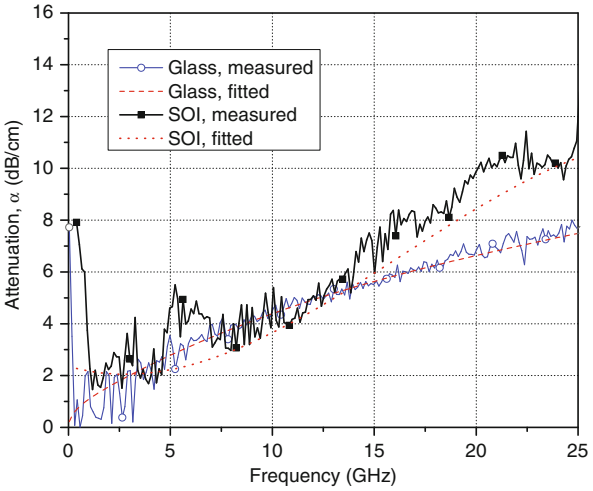


Fig. 4.16 Comparison of attenuation of LRSi-core CPW on SOI and glass substrate

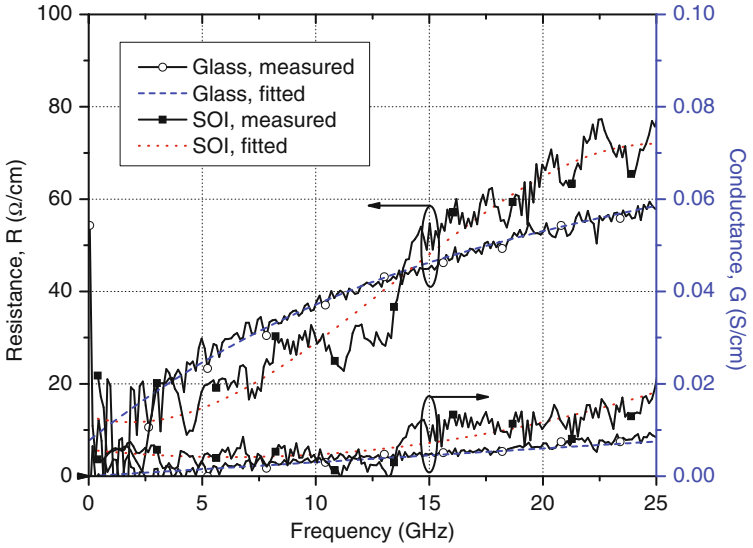


Fig. 4.17 Comparison of resistance and conductance of LRSi-core CPW on SOI and glass substrate

S/*W*/*G* are 66/67/100 μm. The substrate is high-resistivity silicon with the thickness of 500 μm. The core material is low-resistivity silicon with the thickness of 35 μm. Between the substrate and the device, silicon layer is a 2-μm-thick thermal oxide; 1.2-μm-thick Al is coated. For the glass-based LRSi-core CPW, *S*/*W*/*G* are

110/45/400 μm, respectively. The substrate is 500-μm-thick glass. The core material is 60-μm-thick low-resistivity silicon. $h_r \approx 6$ μm, $w_r \approx 10$ μm; 1-μm-thick gold is coated. The measured unit *RLGC* parameters, the characteristic impedance, and the attenuation are extracted from measured *S*-parameters. The fitted unit *RLGC* parameters are fitted from the measured *RLGC* parameters. The fitted attenuation and the fitted characteristic impedance are calculated from the fitted *RLGC* parameters, which agree well with the measured results. As in Section 4.3.1, the SOI-based CPW has larger shunt conductance than the glass-based CPW, especially at high-frequency range. Therefore, the SOI-based CPW has higher dielectric loss than the glass-based CPW, as shown in Fig. 4.17. For any frequency below 13 GHz, the resistance of the SOI-based CPW is less than the glass-based CPW due to thicker metal coating. However, when the frequency is above 13 GHz, both the resistance and the conductance of the SOI-based CPW arise abruptly, resulting in larger attenuation than the glass-based CPW, as shown in Fig. 4.16.

The effect of the core material of the Si-core CPW is illustrated in Figs. 4.18 and 4.19. The parameters of the transmission line *S*/*W*/*G* are 110/45/400 μm. The substrate is 500-μm-thick glass. $h_r \approx 6$ μm, $w_r \approx 10$ μm, and 1-μm-thick Au is deposited. The thickness of waveguides of Si-core CPWs is about 60 μm. The unit capacitance of the LRSi-core CPW is 1.33 pF/cm, which is slightly larger than the HRSi-core CPW of 1.30 pF/cm. However, as in Section 4.3.2, the inductance of the HRSi-core CPW is larger than the LRSi-core CPW. They are 2.85 and 2.26 nH/cm, respectively. As a result, the characteristic impedance of the HRSi-core CPW of 47 Ω is larger than that of the LRSi-core CPW of 41.2 Ω, as shown in Fig. 4.18.

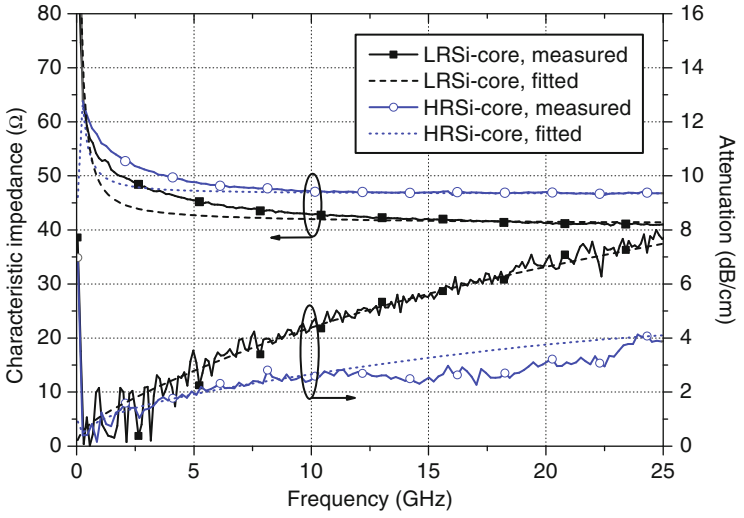


Fig. 4.18 Comparison of characteristic impedance and attenuation between the HRSi-core CPW and the LRSi-core CPW on glass. Copyright/used with permission of/courtesy of Institute of Physics and IOP Publishing Limited

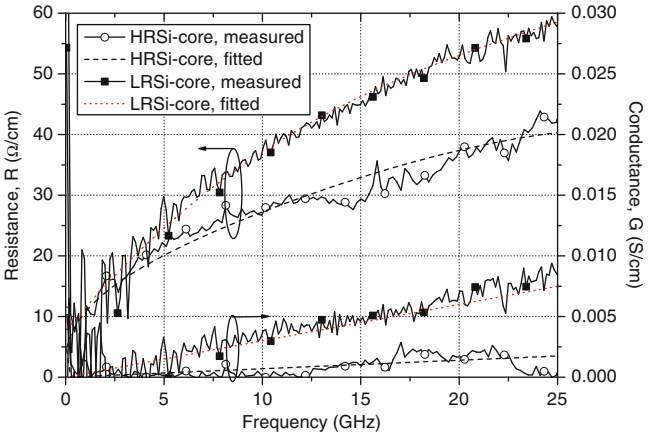


Fig. 4.19 Comparison of resistance and conductance between the HRSi-core CPW and the LRSi-core CPW on glass

The HRSi-core CPW has lower attenuation than the LRSi-core CPW, as shown in Fig. 4.19. That is because the unit shunt conductance, G, of the HRSi-core CPW is less than the LRSi-core CPW, resulting in lower dielectric loss. The unit resistance, R, of the HRSi-core CPW is significantly lower than the LRSi-core CPW, resulting in lower conductor loss.

Table 4.4 shows the comparison between the measured and fitted *RLGC* parameters, the characteristic impedance, the attenuation between the SOI-based LRSi-core CPW, the glass-based LRSi-core CPW, and the glass-based HRSi-core CPW at 20 GHz. The glass-based HRSi-core CPW has the lowest resistance, conductance, and attenuation. The conductor loss is the dominant factor of the attenuation. Thicker metal should be coated to reduce the attenuation of the Si-core CPW.

Table 4.4 Comparison of measured and fitted *RLGC* values and attenuations of Si-core CPW with different substrates and core materials at 20 GHz

	SOI-based LRSi core		Glass-based LRSi core		Glass-based HRSi core	
CPW parameters	Measured	Fitted	Measured	Fitted	Measured	Fitted
R (Ω/cm)	69.7	65.1	53	53	37.6	37.4
L (nH/cm)	4.1	4.1	2.26	2.29	2.85	2.83
G (S/cm)	0.012	0.011	0.007	0.006	0.0017	0.0014
C (pF/cm)	1.95	1.95	1.33	1.33	1.30	1.30
Z_0 (Ω)	45.9	46.2	41.2	41.5	47	46.7
α_c (dB/cm)	6.59	6.11	5.58	5.55	3.48	3.48
α_d (dB/cm)	2.39	2.37	1.25	1.08	0.34	0.28
α (dB/cm)	10.04	8.48	6.88	6.63	3.82	3.76

Based on this study, the following guidelines are recommended to achieve low-loss Si-core CPW: (i) depositing sufficiently thick metal and improving the step coverage of the metal deposition; (ii) using low-loss substrate, such as glass; and (iii) using high-resistivity silicon as the core material.

4.5 Surface-Micromachined CPW Transmission Line

A coplanar waveguide (CPW) consists of a center strip conductor with semi-infinite ground planes on either side as shown in Fig. 4.20. The dimensions of the center strip, the gap, the thickness, and permittivity of the dielectric substrate are determined by the effective dielectric constant ε_{eff}, the characteristic impedance Z_0, and the attenuation, α, of the transmission line. This CPW structure supports a quasi-TEM mode of propagation. The CPW offers several advantages over the conventional microstrip line [5–12] as (1) it simplifies fabrication, (2) easy shunt as well as series surface mounting of active and passive devices, (3) it eliminates the need for wraparound and via holes, and (4) it reduces radiation loss.

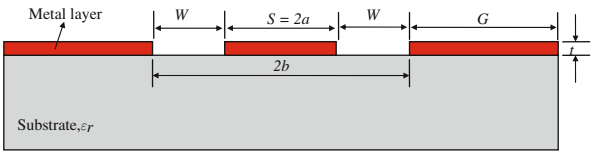


Fig. 4.20 Schematic of the coplanar waveguide (CPW) structure

4.5.1 Characteristic Impedance and Effective Dielectric Constant

The cross-sectional view of CPW is shown in Fig. 4.20. The CPW center strip conductor width S is equal to $2a$ and the distance of separation between the two ground planes is $2b$. Consequently, the slot width W is equal to $b - a$. The CPW conductors and the dielectric substrates are assumed to have perfect conductivity and relative permittivity, respectively. Hence, the structure is considered to be low loss and the dielectric substrate materials are considered to be isotropic.

In this section, the mathematical derivations of ε_{eff} and Z_0 using the conformal mapping techniques are presented. Two assumptions are made. First, the conductor thickness t is zero and, second, the magnetic walls are present along all the dielectric boundaries including the CPW slots. The CPW is then divided into several partial regions and the electric field is considered to exist successively only in the partial region. In this manner, the capacitance of each partial region is determined separately. The total capacitance is the sum of the partial capacitances [13]. The total capacitance C_{CPW} can be expressed as [14]

$$C_{\text{CPW}} = C_1 + C_{\text{air}} \tag{4.5}$$

where

$$C_1 = 2\varepsilon_0 \left(\varepsilon_{r1} - 1\right) \frac{K\left(k_1\right)}{K\left(k_1'\right)} \tag{4.6a}$$

where K is complete elliptic integral of first kind and the modulus of the elliptic integrals $K\left(k_1\right)$ and $K\left(k_1'\right)$ are given by

$$k_1 = \frac{\sinh\left(\pi S/4h_1\right)}{\sinh\left\{\left[\pi\left(S + 2W\right)\right]/4h_1\right\}} \tag{4.6b}$$

and

$$k_1' = \sqrt{1 - {k_1}^2} \tag{4.6c}$$

where h_1 is the height of the substrate, S is the CPW central strip conductor width, and W is the slot width.

The capacitance C_{air} is given by

$$C_{\text{air}} = 2\varepsilon_0 \frac{K(k_3)}{K(k_3')} + 2\varepsilon_0 \frac{K(k_4)}{K(k_4')} \tag{4.7a}$$

where

$$k_3 = \frac{\sinh\left(\pi S/4h_3\right)}{\sinh\left\{\left[\pi\left(S + 2W\right)\right]/4h_3\right\}} \tag{4.7b}$$

$$k_4 = \frac{\sinh\left(\pi S/4h_4\right)}{\sinh\left\{\left[\pi\left(S + 2W\right)\right]/4h_4\right\}} \tag{4.7c}$$

$$k_3' = \sqrt{1 - {k_3}^2} \tag{4.7d}$$

$$k_4' = \sqrt{1 - {k_4}^2} \tag{4.7e}$$

Substituting $h_3 = h_4 = \infty$ into Eqs. (4.7a), (4.7b), and (4.7c), we have

$$C_{\text{air}} = 4\varepsilon_0 \frac{K(k_0)}{K(k_0')} \tag{4.8a}$$

and

$$k_3 = k_4 = k_0 = \frac{S}{S + 2W} \tag{4.8b}$$

Substituting Eqs. (4.6a) and (4.8a) into Eq. (4.5), C_{CPW} is expressed as

$$C_{\mathrm{CPW}} = 2\varepsilon_0 \left(\varepsilon_{\mathrm{r1}} - 1\right) \frac{K\left(k_1\right)}{K\left(k_1'\right)} + 4\varepsilon_0 \frac{K\left(k_0\right)}{K\left(k_0'\right)} \tag{4.9}$$

Under the quasi-static approximation, $\varepsilon_{\mathrm{eff}}$ is defined as [14]

$$\varepsilon_{\mathrm{eff}} = \frac{C_{\mathrm{CPW}}}{C_{\mathrm{air}}} \tag{4.10}$$

Substituting Eqs. (4.8a) and (4.9) into Eq. (4.10) is expressed as

$$\varepsilon_{\mathrm{eff}} = 1 + \frac{\varepsilon_{\mathrm{r1}} - 1}{2} \frac{K(k_1)}{K(k_1')} \frac{K(k_0')}{K(k_0)} \tag{4.11}$$

The characteristics impedance Z_0 is defined as [14]

$$Z_0 = \frac{1}{cC_{\mathrm{air}}\sqrt{\varepsilon_{\mathrm{eff}}}} \tag{4.12}$$

Substituting Eq. (4.8a) into Eq. (4.12) gives

$$Z_0 = \frac{1}{4c\varepsilon_0\sqrt{\varepsilon_{\mathrm{eff}}}} \frac{K\left(k_0'\right)}{K\left(k_0\right)} \tag{4.13a}$$

where $c = 3 \times 10^8$ m/s and $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m, then Eq. (4.13a) is simplified as

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{\mathrm{eff}}}} \frac{K\left(k_0'\right)}{K\left(k_0\right)} \tag{4.13b}$$

In Fig. 4.21, the characteristics impedance curve is plotted with different slot and conductor width values. The characteristic impedances for different dielectric substrates are also included. For the same ratio, $S/(S+W)$ of the slot conductor, the substrate with a lower dielectric constant has a higher characteristic impedance.

The vector current distribution of the coplanar waveguide is calculated using the method of moment software IE-3D as shown in Fig. 4.22. In CPW transmission line, the electric field radiates from the center signal conductor to the two ground conductors and into the substrate where the dominant mode for this kind of transmission line is quasi-transverse electromagnetic (TEM) mode, while the magnetic field lines enclose around only the center signal conductor. The electric current calculated from IE-3D is 250.3 amp/m which is dominant compared to magnetic current of 1×10^{-5} V/m. This is the reason for the strong penetration of the E-field from the signal line to ground plane and into the substrate. In Fig. 4.22, the bar indicates the different color representations in decibels for different attenuation levels. It is noticed that the signal passes with minimum attenuation of 0.1–0.3 dB from input to the output port.

The material property of the substrate has significant effects on the performance of the CPW transmission line.

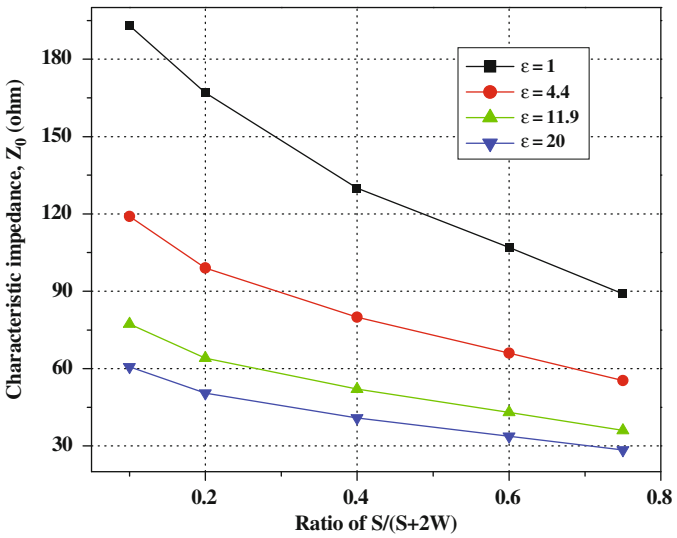


Fig. 4.21 Characteristic impedance of coplanar waveguide versus different dielectric constant of the substrate material

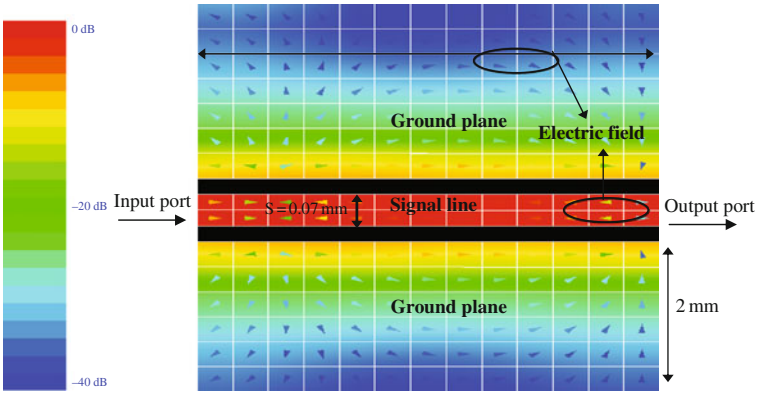


Fig. 4.22 Simulation result of the current distribution in the coplanar waveguide. Copyright/used with permission of/courtesy of IEEE

Figure 4.23 shows that for fixed (S+2W) and aspect ratio S/(S+2W) the Z_0 decreases as the thickness of the metal t increases for silicon substrate. For the fixed aspect ratio S/(S+2W) of 0.1 and the metal thickness 0.5 μm, the characteristic impedance is 78.37 Ω. On the other hand, when the metal thickness is 10 μm the characteristic impedance is 72.54 Ω; for the fixed aspect ratio of 0.75, the characteristic impedance is 37.5 Ω for 10 μm and 38.4 Ω for 2-μm metal thickness.

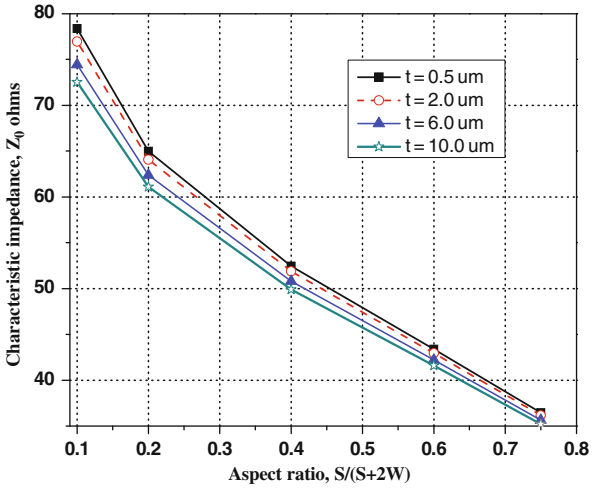


Fig. 4.23 Simulation result of characteristic impedance of CPW with different metal thicknesses

4.5.2 Losses of CPW Structure

For the CPW structure, two major factors are considered for the transmission line losses. The total CPW attenuation is expressed as the sum of the attenuation due to the dielectric losses in the substrate and that due to the conductor losses in the strip and the ground planes.

The dielectric loss, α_d is due to the displacement current in the guiding medium of the CPW transmission line. The attenuation constant due to the dielectric loss is expressed as [15]

$$\alpha_d = \frac{\pi}{\lambda_0} \frac{\varepsilon_r}{\sqrt{\varepsilon_{eff}}} q \tan \delta_e (\mathrm{N/m}) \tag{4.14}$$

where λ_0 is the free space wavelength in meters, ε_r is the relative permittivity of the substrate,tan δ_e is the dielectric loss tangent, ε_{eff} is the effective dielectric constant. The loss tangent tan δ_e remains constant with respect to the frequency for different dielectric materials. However, the dielectric loss α_d increases linearly with the frequency. The loss tangent is an important factor to be taken into consideration as there are material losses due to bulk conductivityσ. The loss tangent is defined as

$$\tan \delta_e = \frac{\sigma}{\omega \varepsilon_0 \varepsilon_{eff}} \tag{4.15}$$

The material with high loss tangent results in a higher dielectric loss. The material or substrate properties are listed in Table 4.5.

The attenuation constant due to the conductor loss α_c in the central strip conductor and the ground planes of the CPW is given below. In deriving this expression,

Table 4.5 Properties of the dielectric materials

Materials	ε_r	$\tan \delta_e$
High-resistivity (HR) silicon	11.9	0.025 S × m
Low-resistivity (LR) silicon	11.9	100 S × m
Air	1.0	0.0 S × m

the thickness t of the CPW conductors is assumed to be greater than the skin depth δ in the metal. The conductor loss α_c is defined as [15]

$$\alpha_c = \frac{R_c + R_g}{2Z_0} \tag{4.16}$$

where R_c is the series resistance in ohms per unit length of the center conductor given by

$$R_c = \frac{R_s}{4S\left(1 - k_0^2\right) K^2(k_0)} \left[\pi + \ln\left(\frac{4\pi S}{t}\right) - k_0 \ln\left(\frac{1 + k_0}{1 - k_0}\right)\right] \tag{4.17}$$

R_g is the distributed series resistance in ohms per unit length of the ground planes and is given by

$$R_g = \frac{k_0 R_s}{4S\left(1 - k_0^2\right) K^2(k_0)} \left[\pi + \ln\left(\frac{4\pi(S + 2W)}{t}\right) - \frac{1}{k_0} \ln\left(\frac{1 + k_0}{1 - k_0}\right)\right] \tag{4.18}$$

R_s is the skin effect surface resistance and is given by

$$R_s = \sqrt{\frac{2}{\omega \delta \sigma}} \tag{4.19}$$

where σ is the conductivity and δ is the skin depth. Therefore, the total attenuation α can be expressed as

$$\alpha = \alpha_c + \alpha_d \tag{4.20}$$

Based on Eq. (4.14), the dielectric loss is linearly proportional to frequency. Figure 4.24 shows the relationship between the frequency and the attenuation. The attenuation at the frequency of 20 GHz is 0.37 dB/cm.

Figure 4.25 shows the simulation results of the attenuation constant α and the characteristic impedance Z_0 when the ground plane separation (S+2W) is constant. It is noted that the attenuation decreases slowly with the increase in characteristic impedance. Minimum attenuation occurs at the characteristic impedance which is close to 50 Ω. When the characteristic impedance is raised above 50 Ω, the attenuation increases gradually.

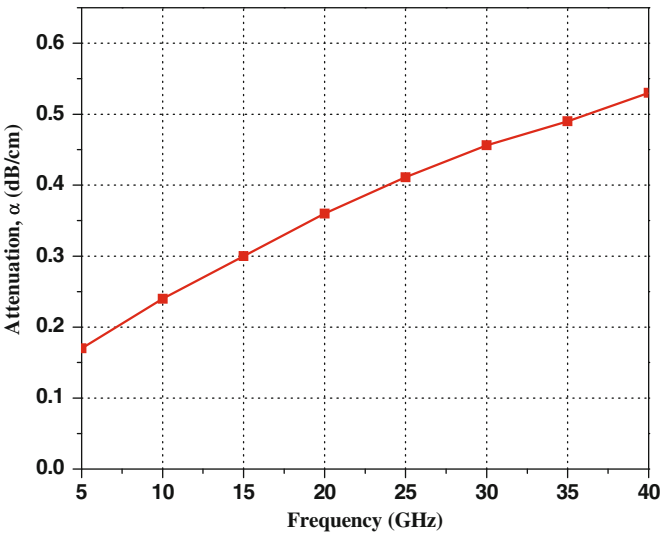


Fig. 4.24 Simulation results of attenuation constant due to conductor loss as a function of frequency of the CPW structure. Copyright/used with permission of/courtesy of IEEE

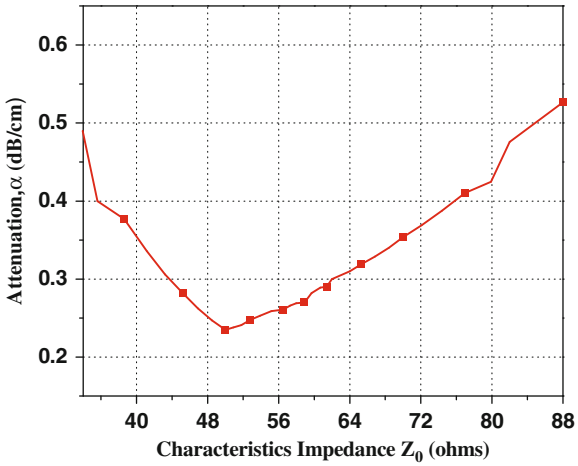


Fig. 4.25 Simulation results of coplanar waveguide attenuation constant versus characteristic impedance for an aspect ratio, $S/(S+2W)$. Copyright/used with permission of/courtesy of IEEE

4.5.3 Effects of Material Properties

The material properties have a significant effect on the performance of the CPW structure. They affect both the insertion loss and the RF transmission properties of the structure. Usually the insertion loss of the CPW structure should be made as

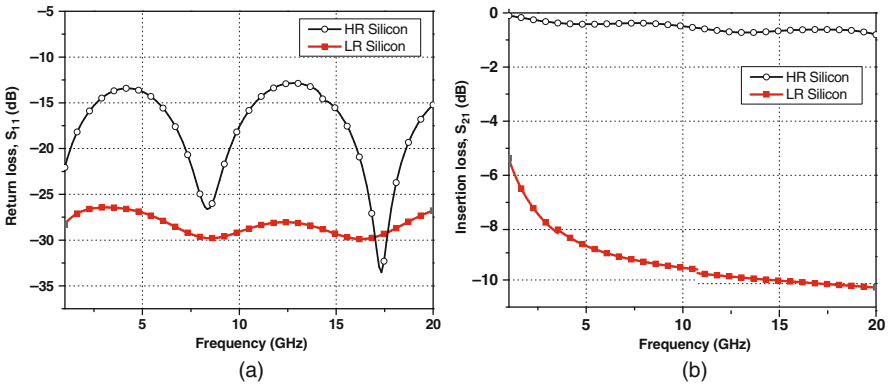


Fig. 4.26 Comparison of the simulated results of the HR silicon and LR silicon: **(a)** return loss S_{11} and **(b)** insertion loss S_{21}. Copyright/used with permission of/courtesy of IEEE

low as possible so that its influence on the performance of any microwave devices, such as filters, switches, and couplers, is negligible. The CPW structure length is 10 mm.

The simulation results of the high-resistivity (HR) silicon and low-resistivity (LR) silicon are shown in Fig. 4.26. The resistivity of HR silicon is 4000 $\Omega \times$ cm, while that of LR silicon is 20 $\Omega \times$ cm. The thickness of the metal layer is 2 μm The insertion losses for HR silicon and LR silicon at 5 GHz are 0.3 and 8.5 dB, respectively. Similarly, the insertion loss for the HR silicon at 15 GHz is 0.7 dB and for LR silicon is 10 dB. Therefore, it can be concluded that the CPW structure realized on LR silicon has higher attenuation compared to HR silicon. As a result, silicon with high resistivity is preferred in RF MEMS devices.

4.5.4 Effects of Metal Thickness

The effect of metal thickness t of the CPW transmission line at the fixed frequency of 20 GHz is shown in Fig. 4.27. As expected, the attenuation rises rapidly when the metal thickness becomes less than two to three times the skin depth δ Figure 4.28 shows the EM simulation results of the effect of the metal thickness on the insertion loss. The metal is gold (Au) with a conductivity of 4.1×10^7S/m. When the metal thickness is 4 and 6 μm the insertion losses are 0.2 dB at 5 GHz and 0.40 dB at 15 GHz, respectively. When the metal thickness is reduced to 2 μm, a higher insertion loss of 0.75 dB at 15 GHz is observed. Therefore, it can be concluded that the thicker the deposition layer of Au, the lower the conductor loss.

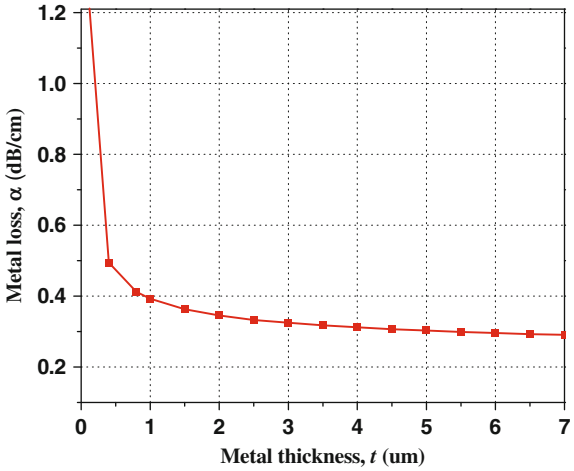


Fig. 4.27 Simulation result of the conductor loss versus different conductor thicknesses t at 20 GHz. Copyright/used with permission of/courtesy of IEEE

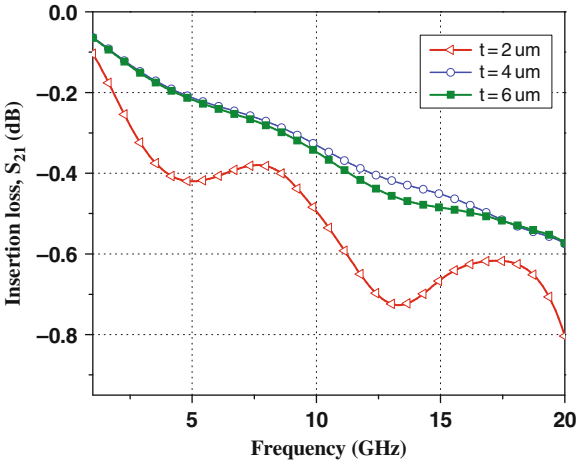


Fig. 4.28 Simulations results of the insertion loss versus frequency with different metal thicknesses as parameter. Copyright/used with permission of/courtesy of IEEE

4.5.5 Experimental Results and Discussions

The RF performance of the silicon CPW structure are measured using the HP 8510C vector network analyzer with gold tip –150 μm pitch from cascade microtech ground–signal–ground coplanar probes. The system is calibrated using standard short-open-load-through (SOLT) on wafer calibration technique. A 5-mm plastic plate is placed between the probe chuck and the sample to remove higher order modes of propagation. All experiments are performed in the room environment without packaging. SEM image of the CPW structure is shown in Fig. 4.29.

The dimensions of the CPW structure are $S = 70$ μm and $W = 115$ μm. The CPW structure length is 10 mm. It is fabricated using high-resistivity silicon

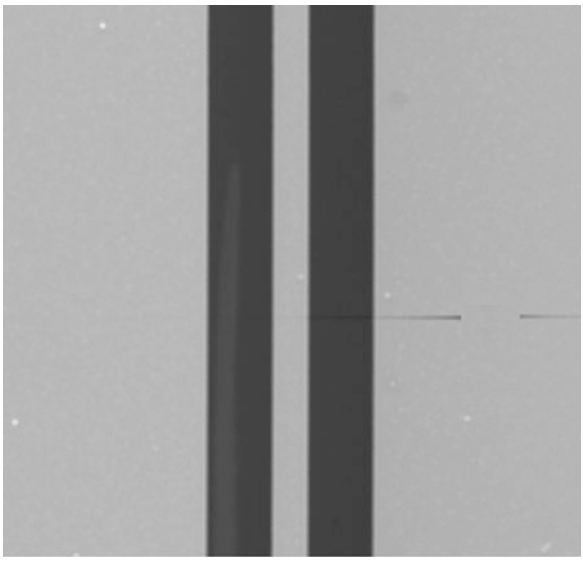


Fig. 4.29 Top view of SEM image of the CPW structure

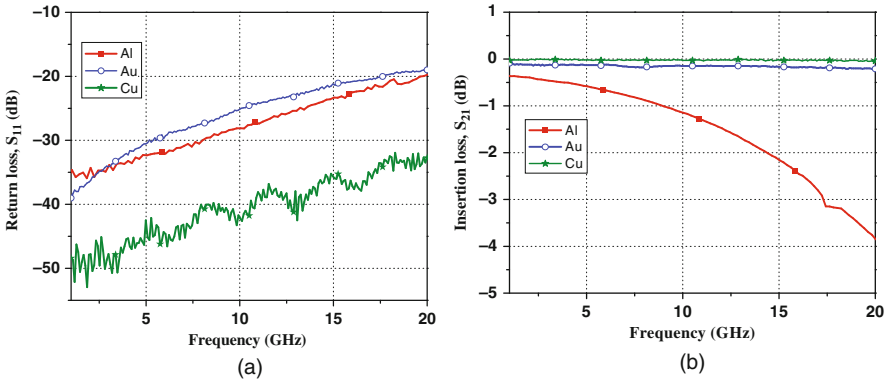


Fig. 4.30 Measurement results of RF properties of the CPW using different materials for the conductor layer: **(a)** return loss S_{11} and **(b)** insertion loss S_{21}. Copyright/used with permission of/courtesy of IEEE

substrate. The conductor layers are deposited using three different types of metal materials. The measurement results are shown in Fig. 4.30. Aluminum (Al) has a high insertion loss of 0.5 dB at 5 GHz and 2.1 dB at 15 GHz. Gold (Au) and copper (Cu) materials show excellent result in terms of insertion loss. Gold has an insertion loss of 0.17 dB at 5 GHz and 0.2 dB at 15 GHz, whereas copper is slightly better with an insertion loss of 0.08 dB at 5 GHz and 0.13 dB at 15 GHz. However, the CPW transmission line and RF MEMS switch are fabricated using gold as the conductor layer. The reason for this is that, although copper shows a better RF performance, gold is more advantageous due to its resistance to oxidation, increased reliability, and stability.

4.6 Summary

In this chapter, the Si-core metal-coated CPW is studied. The design and the full-wave EM simulation of the Si-core CPW are presented. The losses of the Si-core CPW transmission line related to the substrate material, the core material, and the process variations are analyzed using the *RLGC* model. The analysis shows that the substrate material and the core material have influence on the dielectric loss. High-resistivity and low-loss material is more favorable for the substrate and the core material for the low-loss Si-core CPW transmission line. The process variations, including the thickness of the silicon backbone and the undercut dimensions, also significantly affect the RF performance of the Si-core CPW. The experimental results also verify that the Si-core CPW supports quasi-TEM mode propagation up to 25 GHz with attenuation of less than 4 dB/cm. It is found that the conductor loss dominates the attenuation of the Si-core CPW. Some useful guidelines for low-loss Si-core CPW are as follows: (i) depositing sufficiently thick metal layer and improving the step coverage of the metal deposition; (ii) utilizing low-loss substrate, such as glass; and (iii) using high-resistivity silicon as core material.

The surface-micromachined CPW transmission line is also designed, fabricated, and experimented. The study shows that material properties play an important role in the performance of the CPW transmission line. Different metal thickness is analyzed for better insertion loss performance. Even though copper is found to be slightly better than gold in terms of performance, gold is still preferred and used in the practical implementation because of its low oxidation and high reliability. High-resistivity (HR) silicon substrate is used for better RF performance. The insertion loss at 5 GHz for HR silicon and LR silicon is 0.3 and 8.5 dB, respectively. Similarly, the insertion loss at 15 GHz for HR silicon and LR silicon is 0.7 and 10 dB, respectively. The measurement results for gold show an insertion loss of 0.17 dB at 5 GHz and 0.2 dB at 15 GHz.

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