Chapter 10
Surface Planarization Process

Surface planarization process is discussed in this chapter. Compared to bulk micromachining process, surface micromachining process is more suitable for the fabrication of capacitive switches. It is always important to planarize the sacrificial layer under the metal bridges to achieve flat metal bridges. Besides surface planarization, surface roughness is another important consideration to improve the intimate contact between the metal bridges and the dielectric layer when the metal bridges are driven down. Detailed discussion will be given in this chapter.

10.1 Surface Planarization Process

The process flow described in this section is mainly for the fabrication of a single capacitive switch. However, the same process flow can also be used to fabricate DC-contact capacitive switches and tunable band-pass devices.

Since the planarization of the metal bridge plays a significant role in reducing the contact area between the bridge and the dielectric layer, a planarization process is proposed by filling the CPW slot with photoresist which can effectively improve the flatness of the bridge.

Surface micromachining fabrication process with five masks is used to fabricate the switch [1]. High-resistivity (>4000 Ω cm) silicon wafers with thickness of 500 μm are used as substrate. The fabrication process flow is shown in Fig. 10.1 and described as follows: (a) plasma-enhanced chemical vapor deposition (PECVD) 1-μm-thick SiO_2 is deposited as the buffer layer in a Plasma-Therm 790 series RIE system from Material Co. USA; (b) a layer of 2-μm-thick aluminum (Al) thin film is evaporated and patterned as the CPW transmission line with the first mask. The pressure and the deposition rate are 6×10^{-5} Pa and 10 Å/s, respectively. Wet etching is used to pattern the Al metal bridge. The etchant used is a mixture of H_3PO_4:HNO_3:HAc:H_2O = 4:1:4:1, and the etching temperature is 35°C. The etching rate is approximately of 1500 Å/min; (c) a 0.15-μm PECVD SiN is deposited with SiH_4 (diluted in nitrogen at a concentration of 20%) flow rate of 24 sccm and

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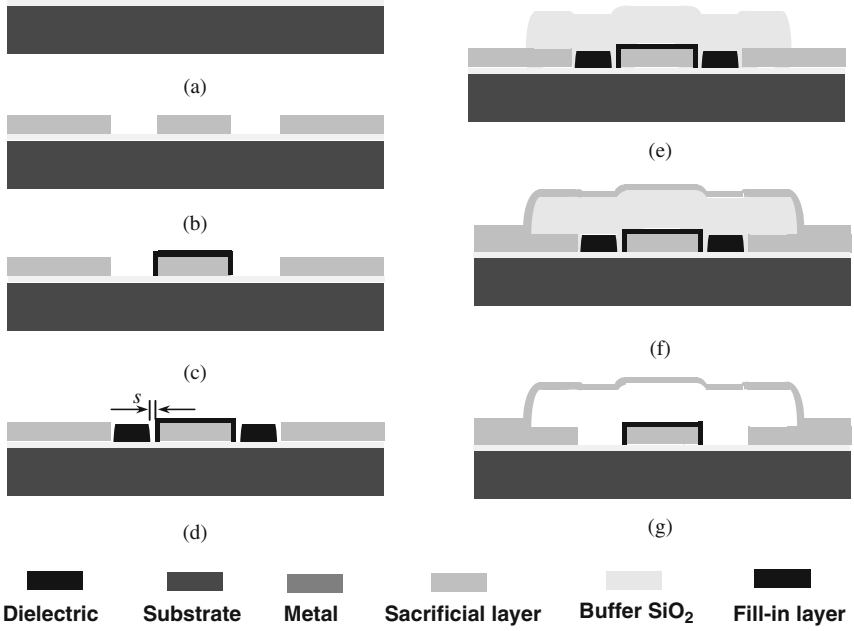


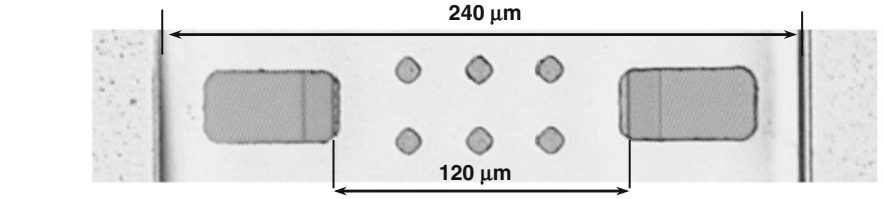
Fig. 10.1 Fabrication process flow [1]. Copyright/used with permission of/courtesy of Elsevier B.V

NH_3 flow rate of 7.1 sccm at a pressure of 1.1 Torr and temperature of 250°C in the same Plasma-Therm 790 series machine. The temperature is 100°C lower than the temperature at normal PECVD SiN deposition. This reduces the surface roughness of the capacitance area. In the process of etching the SiN layer, 2-μm-thick photoresist (Sumitomo PFI26A) is used as soft mask and patterned with the second mask. The SiN layer is etched using reactive ion etching (RIE) with a CHF_3 flow rate of 31 sccm and an O_2 flow rate of 2.6 sccm. The etching power is 235 W and the pressure is 60 mTorr. The self-bias voltage is 350 V and the plasma frequency is 13.56 MHz. The etching rate is 400 Å/min. The photoresist is stripped away after SiN etching with PRS3000 solution; (d) a layer of photoresist with 1.5-μm thick (Sumitomo PFI26A) is spun coated and patterned with the third mask to fill in the CPW slot (refer to this layer of photoresist as fill-in photoresist and this process is known as the planarization step). This is the key step to obtain a flat metal bridge; (e) a 2-μm-thick photoresist (Sumitomo PFI26A) sacrificial layer is spun coated and patterned (refer to this layer of photoresist as sacrificial photoresist); (f) a layer of 0.6-μm Al is evaporated and patterned as the metal bridge with the fourth mask; (g) finally, the metal bridges are released by etching away the photoresist with oxygen plasma also in a Plasma-Therm 790 series machine. After releasing, the metal bridge is free to deform out of plane following the relief of internal stress.

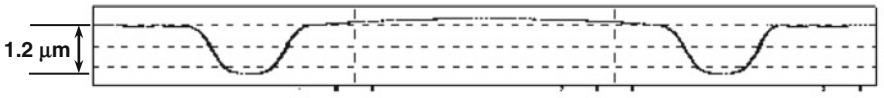
Based on this process flow, after filling the CPW slots with the fill-in photoresist in planarization step (d), the sacrificial photoresist is coated and patterned as in step (e) immediately. Therefore, the hard-bake temperature T_f must be higher than the hard-bake temperature T_s, (e) in order to avoid the peeling-off of the fill-in photoresist. In this process, T_f is 150°C, whereas T_s is 115°C. Another factor that has to be taken into consideration is the mask alignment and tolerance control in the fabrication process. The gap spacing (s) between the patterned fill-in photoresist and the CPW structure, as indicated in Fig. 10.1d, varies between 1 and 3 μm. It is observed that 3 μm is the most optimal as the mask alignment mismatch does not affect the patterns of the fill-in photoresist in this case.

Based on the proposed planarization strategy, two switches, switch A and switch B, are fabricated with different fabrication processes. Switch A is fabricated without the planarization and switch B is fabricated with the planarization. Figure 10.2a, b shows the surface profiles of the two switches. These profiles are obtained after the wet etching and before the release of the bridge. For switch A, the portion of the bridge above the CPW slot is 1.2 μm lower than the portion of the bridge above the CPW central conductor. For switch B, the portion of the bridge above the CPW slot is 0.5 μm higher than the portion of the bridge above the CPW central conductor.

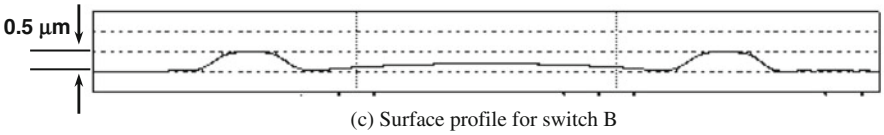
Correspondingly, Fig. 10.3 shows the SEM image of the two switches after releasing. The etching holes on the bridge make the release of the bridge easier and also reduce the damping effect [2]. Figure 10.3a shows that the g_{slot} is smaller



(a) Optical image of the metal bridge



(b) Surface profile for switch A



(c) Surface profile for switch B

Fig. 10.2 Surface profiles of the capacitive shunt switch: **(a)** Optical image of the metal bridge; **(b)** surface profile for switch A without fill-in photoresist; and **(c)** surface profile for switch B with fill-in photoresist [1]. Copyright/used with permission of/courtesy of Elsevier B.V

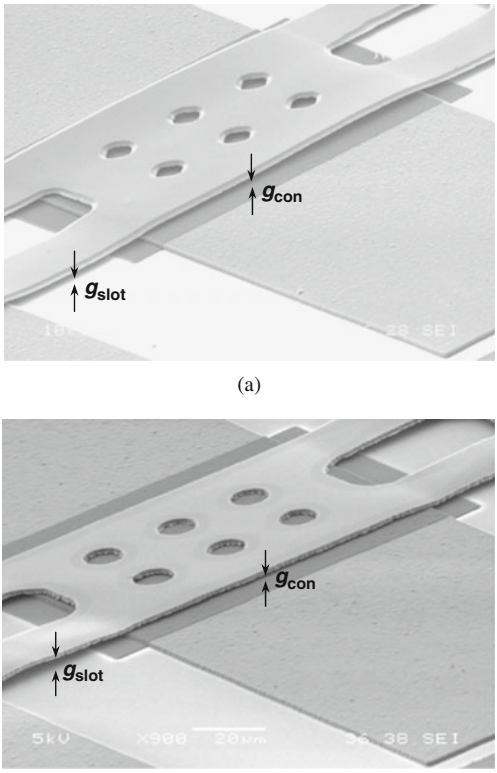


Fig. 10.3 SEM images of the capacitive shunt switch **(a)** without fill-in photoresist and **(b)** with fill-in photoresist [1]. Copyright/used with permission of/courtesy of Elsevier B.V

than g_{con} in switch A. When switch A is driven down, it touches the CPW slot edges first. After that, it is difficult to pull down further, making closer contact between the metal bridge and the dielectric layer impossible. On the contrary, Fig. 10.3b shows that g_{slot} is larger than g_{con} in switch B. Thus, the metal bridge touches the dielectric layer first when it is driven down. This improves the contact between the bridge and the dielectric layer.

10.2 RF Measurement and Analysis

The RF performance of the switch is characterized using an HP8510C vector network analyzer and RF probe station. A full thru–reflect–line (TRL) routine is used to calibrate with NIST software MULTICAL.

Figure 10.4 shows the RF measurement and simulation results of the two switches. All the simulations are conducted using Ansoft's high-frequency simulation software (HFSS) [3]. Figure 10.4a, b shows that the up-state performances of

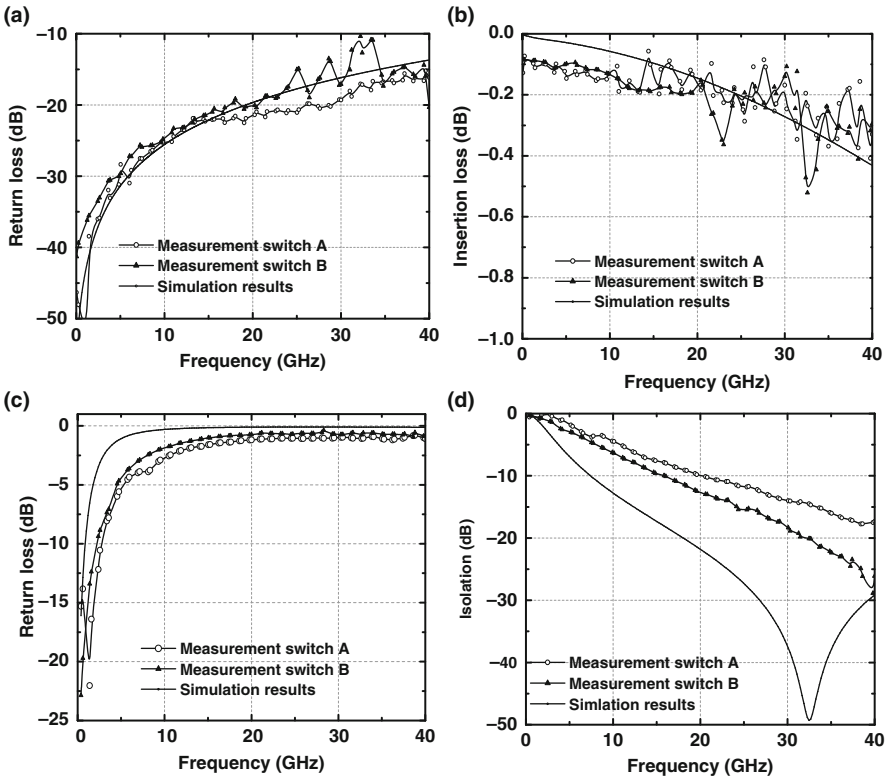


Fig. 10.4 Comparison of simulated and measured *S*-parameters: **(a)** up-state return loss; **(b)** up-state insertion loss; **(c)** down-state return loss; and **(d)** down-state isolation [1]. Copyright/used with permission of/courtesy of Elsevier B.V

switch A are comparable to the simulation results. The extracted up-state capacitance (C_u) is 34.4 fF. However, the down-state isolation of switch A is more inferior compared to the simulation results, as listed in Table 10.1 and shown in Fig. 10.4d. The extracted down-state capacitance of switch A (C_{dA}) is 1 pF, which is 33% ($C_{dA} = 33\%\ C_d$) of the simulation results. In Fig. 10.4d, the simulation results are obtained by assuming that the entire bridge area above the CPW center conductor contacts the dielectric layer when the bridge is pulled down. As a result, the simulated down-state capacitance is 3.01 pF and the resonant frequency of the bridge is

Table 10.1 Comparison of down-state isolation and capacitances

	Switch A	Switch B	Simulation
Isolation at 15 GHz (dB)	7.5	9.7	18.0
Isolation at 40 GHz (dB)	17	27	28
Down-state capacitance (pF)	$C_{dA} = 1.0$	$C_{dB} = 1.3$	$C_d = 3.01$

shifted to 32 GHz. However, the down-state capacitance of switches A and B is 1 and 1.3 pF, respectively. Therefore, the isolations of switches A and B are smaller than the simulation results.

From the RF experimental results, both switches are found to have similar up-state RF performance. However, the isolation of switch B can be improved by 2.2 dB at 15 GHz and 10 dB at 40 GHz compared to that of switch A. These are listed in Table 10.1. Table 10.1 also provides the extracted down-state capacitances of switch B, C_{dB}, at 15 GHz. The down-state capacitance of the switch B is 0.3 pF (30%) larger than that of switch A. The results indicate that the contact area between the metal bridge and the dielectric layer increases after surface planarization.

Table 10.2 shows that the down-state capacitance of switch B is smaller than the simulation results ($C_{dB} = 43\%\ C_d$). The roughness of the contact area between the bridge and the dielectric layer is the main contribution factor for this discrepancy. The average roughness is 24 nm approximately. The roughness of the contact area reduces the capacitance $C_d^{'}$ and the overall down-state capacitance C_d becomes smaller. This surface roughness can be solved using a refractory metal (such as tungsten) as the bottom electrode under the PECVD SiN.

Table 10.2 Down-state capacitances with various diameters of etching holes

Diameter of etching holes (μm)	0	2	4	10
Isolation at 15 GHz (dB)	18.34	18.27	18.00	17.37
Down-state capacitance (pF)	3.14	3.11	3.01	2.8

There are other factors that contribute to the degradation of the down-state capacitance. First, the bridge is warp due to the residual stress in the metal bridge (the residual stress is 20 MPa). This reduces the contact area and increases the gap between the bridge and the dielectric layer. Second, polymer residues due to the incomplete removal of the sacrificial photoresist may also make the intimate contact between the bridge and the dielectric layer difficult. Third, the designed diameter of the etching holes in the metal bridge is 4 μm, but the final diameter of the fabricated etching holes is 10 μm due to over wet etch of the Al metal bridge. The etching holes reduce the ratio of the contact area p. Figure 10.5 shows the simulated down-state isolation in the frequency range of 12–18 GHz for various sizes of the etching holes. The extracted down-state capacitances at 15 GHz from the simulation results are listed in Table 10.2. When the diameter of the holes is 2 μm, the down-state capacitance and isolation are not affected. When the diameter of the holes is 4 μm, the extracted down-state capacitance is 95.9% of the capacitance of the bridge without the holes. This indicates that the effect is still relatively small. However, when the diameter of the holes is 10 μm, the down-state capacitance is only 89.2% of the capacitance of the bridge without the holes. As a result, it can be concluded that the diameter of the etching holes must be carefully considered in the design of the switch.

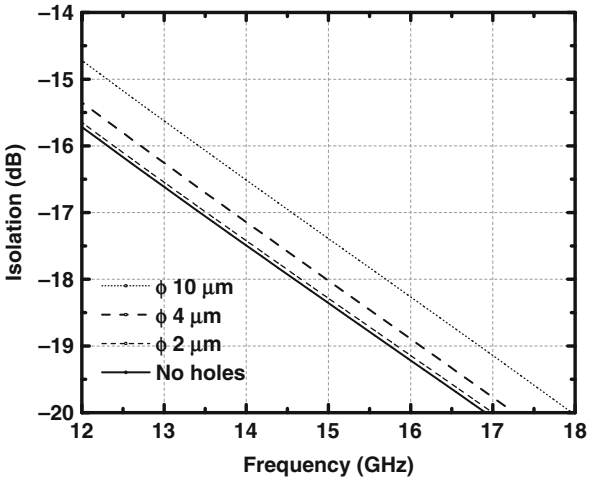


Fig. 10.5 Simulation results for various sizes of the etching holes [1]. Copyright/used with permission of/courtesy of Elsevier B.V

In general, the down-state capacitance of the switch usually varies from 10 to 70% of the expected down-state capacitance [4]. In the current design, this down-state capacitance is 43%. The ratio of the down-state capacitance and the up-state capacitance, C_{dB}/C_u, is approximately 38.

10.3 Effects of Dry Releasing of Metal Bridge

10.3.1 Etch Rate of Photoresist

As mentioned in the process flow in Section 10.1, photoresist is used as the sacrificial layer and oxygen plasma is used to remove the sacrificial photoresist and release the metal bridge. Compared to wet releasing, dry releasing is easier and can prevent the damage of the passivation dielectric and metal thin film by the aggressive etchant.

In this section, the effects of RIE process parameters on the dry releasing process are studied [5]. Figure 10.6a, b shows the optical images of the sacrificial photoresist under the metal bridge before releasing and after 50-min oxygen plasma etch, respectively. The discussion of the fabrication of the lower DC pad and the dielectric layer is not included since they do not have any impact on the sacrificial photoresist releasing. The metal bridges are removed using Al wet etchant. It can be seen clearly that after 50 min of oxygen plasma etch, the edge of the photoresist circle becomes larger and after 70 min of oxygen plasma etch, all the photoresist is etched away and the metal bridge is released. During the oxygen plasma etch, less than 10-nm-thick Al metal bridge is also removed.

For the release process, two main process parameters such as the etching power and the oxygen pressure are investigated. The flow rate of oxygen is fixed at 30 sccm

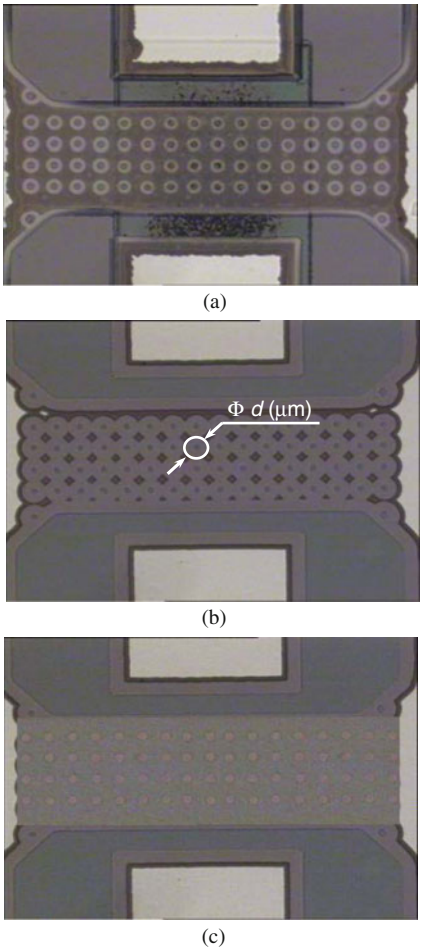


Fig. 10.6 Surface profile of sacrificial photoresist with different release times: **(a)** before release, **(b)** after 50-min etching, and **(c)** after 70-min etching

for all experiments. The lateral etching rate that changes with the pressure is shown in Fig. 10.7. The lateral etching rate is defined as

$$R = \frac{1}{2}\frac{d - d_0}{t} \tag{10.1}$$

where d_0 is the diameter of the photoresist circles before oxygen plasma etch and d is the diameter of the photoresist circles after time t (equal to 50 min in this study) of oxygen plasma etch.

It is shown that the lateral etching rate increases slowly with pressure when the pressure is lower than 500 mTorr and becomes constant when the pressure is higher than 500 mTorr. This phenomenon can be explained since the oxygen atom creation rate increases by increasing the oxygen pressure whereas the mean free

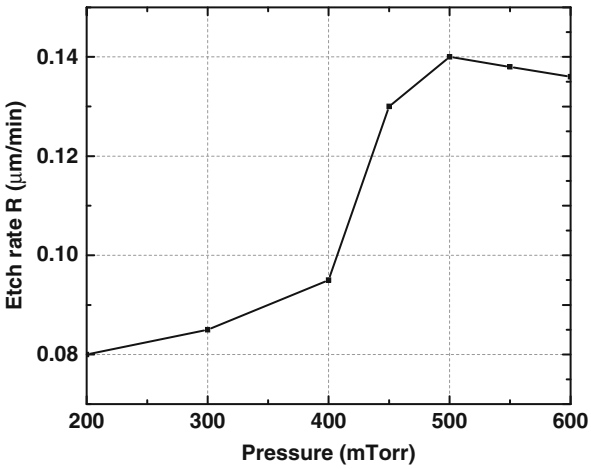


Fig. 10.7 Lateral etching rate versus pressure (power = 430 W; t = 50 min) [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

path length of the oxygen plasma decreases by increasing the oxygen pressure. As a result, the effect of isotropic etching increases [6] and the lateral etching rate increases first. When the pressure increases further, the oxygen atom recombination increases. At certain pressure, the oxygen atom creation and recombination are balanced. Therefore, there is a trade-off between the pressure and the lateral etching rate.

Another important process parameter that may affect the release process is the power. Figure 10.8 shows that the lateral etching rate increases with the power. Until 600 W, there is no saturation point.

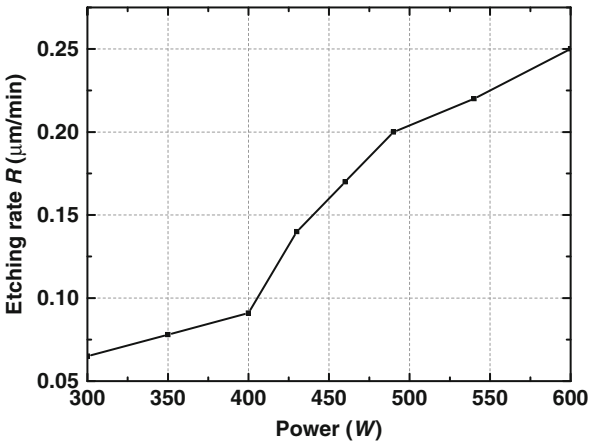


Fig. 10.8 Lateral etching rate versus power (pressure = 500 mTorr; t = 50 min) [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

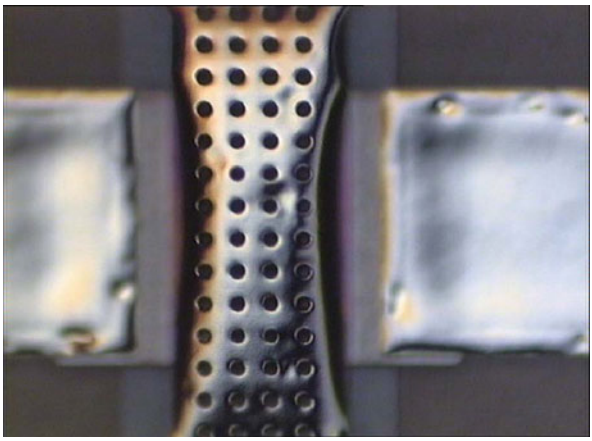


Fig. 10.9 Post-buckling of metal bridge after releasing with power of 500 W [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

However, high power may cause buckling of the metal bridge as shown in Fig. 10.9. Because high plasma power leads to stronger bombardment on the surface of the metal bridge that can change the surface status of the Al thin film, the metal bridge buckles in the process. The compressive stress is due to the bomb of the metal bridge by high energy particles. During the oxygen plasma releasing process, the oxygen absorbed at the surface of the film decreases the surface mobility of the arriving atoms. This results in a less-ordered structure with vacancies and interstitial atoms. Atoms in the grain boundaries and interstitials in the Al thin film produce high compressive stress. Therefore, the etching power in this work is fixed at 430 W.

10.3.2 Structural Stress

Thin film structures can deform undesirably as a result of residual stress; on the other hand, these deformations can be exploited to diagnose the state of stress in the film. Different testing structures have been used to diagnose the state of stress in the film [7]. Normally, microcantilever beam is one of the simplest and most frequently used test structures to investigate different combinations of uniform mean stress and stress gradient [8]. Therefore, an array of micro-cantilevers is fabricated on the same wafer with the capacitive switches to measure the in situ stress, as shown in Fig. 10.10. The cantilever beams are 50-μm wide, with length ranging from 200 to 410 μm in 15-μm increments.

In order to obtain a flat metal bridge after releasing, it is important to control the stress and the stress gradient in the metal bridge. The global stress in the thin film can be extracted from measuring the change in wafer curvature due to the film deposition [9]. However, the stress level in the final structure may be different from

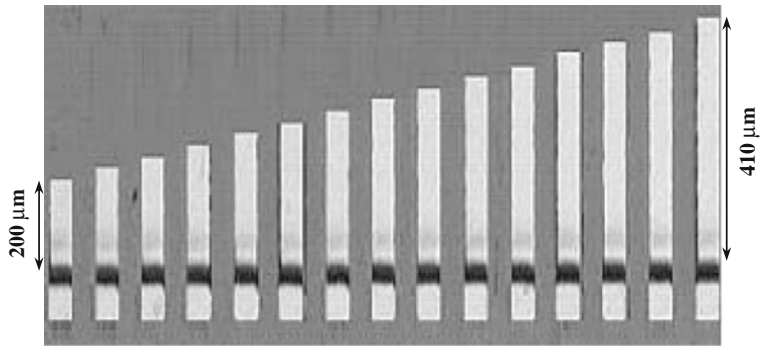


Fig. 10.10 Optical photo of the testing structure of the cantilever beams array [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

that of the as-deposited state, because the film undergoes various micromachining processes, such as various thermal cycles in different process steps or exposure to plasma bombardment with dry release process. Therefore, instead of measuring the global film stress by measuring the wafer curvature, it is more important to measure the mean stress and the stress gradient in the released structure.

The beam is assumed to be fully clamped at one end and free at the other end. The total stress in the beam can be divided into a constant mean stress and a gradient stress. Assuming a linear stress profile within the beam, the stress can be divided into two components that can be expressed as [7, 9]

$$\sigma(z) = \sigma_0 + \sigma_1 \frac{z}{t/2} \tag{10.2}$$

where $z \in (-t/2,\ t/2)$ is the coordinate normal to the surface of the beam with an origin chosen at the film's mid-plane as shown in Fig. 10.11, t is the thickness of the beam, $\sigma(z)$ is the stress distribution along the thickness of the metal beam, σ_0 is the constant mean stress, and σ_1 is the gradient stress. The uniform stress σ_0 accounts for the in-plane elongation of the beam whereas the stress gradient component σ_1 causes the out-of-plane deflection.

The stress distribution leads to a moment M_0 which can be defined as

$$M_0 = \int_{-t/2}^{t/2} \sigma(z) w z dz \tag{10.3}$$

Substituting Eq. (10.2) into Eq. (10.3), the net moment M_0 acting on the beam can be expressed as

$$M_0 = \frac{wt^2}{6}\sigma_1 \tag{10.4}$$

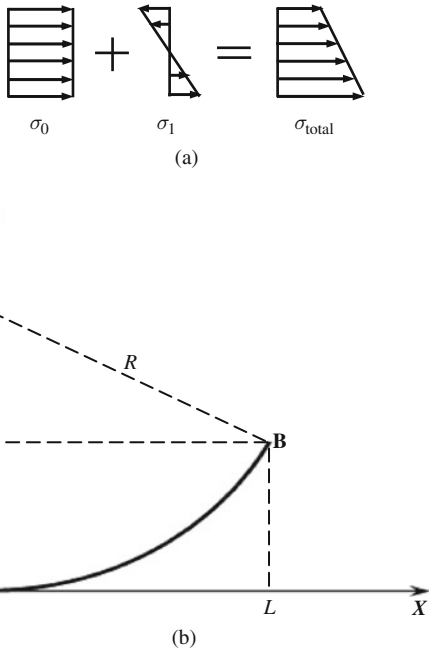


Fig. 10.11 **(a)** Stress in metal bridge and **(b)** schematic drawing of beam deflection [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

The moment M_0 causes the out-of-plane deflection of the cantilever beams. Assuming the curled cantilever beams are perfectly circular and fixed-support at one end, the radius of curvature can be written as [10]

$$R = \frac{E}{d\sigma/dz} \tag{10.5}$$

Substituting Eq. (10.2) into Eq. (10.5), the radius of the curvature can be given as

$$R = \frac{EI}{M_0} = \frac{Et}{2\sigma_1} \tag{10.6}$$

The relationship between the radius and the displacement throughout the cantilever beam can be calculated from trigonometry as shown in Fig. 10.11.

In Fig. 10.11b, the contour of the released cantilever beam arc AB can be expressed as

$$\sin\left(\text{arctg}\frac{z_{\text{tip}}}{L}\right) = \sqrt{L^2 + z_{\text{tip}}^2}/(2R) \tag{10.7}$$

where L is the length of the deflected cantilever projected on the X-axis and z_{tip} is the deflection of the tip of the cantilever beam.

Substituting Eq. (10.6) into Eq. (10.7), the gradient stress can be expressed as

$$\sigma_1 = \frac{2Et \sin\left(\text{arctg}\left(z_{\text{tip}}/L\right)\right)}{\sqrt{L^2 + z_{\text{tip}}^2}} \tag{10.8}$$

At the same time, the length of the cantilever beam after release s can be calculated from Fig. 10.11b as

$$s = R \times 2\frac{\pi \arcsin\left(\sqrt{L^2 + z_{\text{tip}}^2}/2R\right)}{180} \tag{10.9}$$

Then, the in-plane residual stress σ_0 can be determined by

$$\sigma_0 = E\varepsilon = E\frac{s - l}{l} \tag{10.10}$$

where ε is the strain of the cantilever beam after release and l is the original length of the cantilever beam.

Based on Eqs. (10.6), (10.7), (10.8), (10.9), and (10.10), the mean stress and the stress gradient can be obtained by curve-fitting method through the following steps: (1) measuring the deflection z of a cantilever beam at different positions and calculating σ_1 according to Eq. (10.8); (2) based on Eq. (10.6) and the calculated σ_1, the radius of the curved cantilever beam R can be calculated; (3) s can be obtained based on Eq. (10.9) and the values of R, L, and z_{tip}; and (4) σ_0 is calculated according to Eq. (10.10).

Figure 10.12 shows the measured 1D profile of the cantilever beam with the length of 400 μm using WYKO NT3300 optical profiler in vertical scanning interferometry (VSI) mode. The WYKO system utilizes white light passed through a

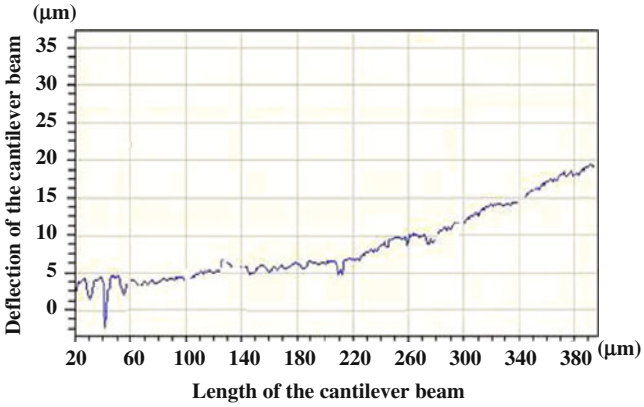


Fig. 10.12 Measured deflection of cantilever beams [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

beam splitter to form interference fringes as a function of height on the sample; objective height is controlled by a piezoelectric transducer. This is a non-contact method to measure the contour of the structures and it has the advantage of being fast and non-destructive [11, 12]. Other cantilever beams can also be used to analyze the stress status in the thin film. The beam with 400-μm length is selected because its deflection is the largest and its length is similar to the length of the metal bridge. As a result, its measurement results provide useful information for the metal bridge design.

Figure 10.13 shows that the measured and curve-fitted deflection of the cantilever beam varies with the position along the beam. These measured deflections can be obtained from Fig. 10.12. Curve fitting is based on Eqs. (10.6), (10.7), (10.8), (10.9), and (10.10). It is found that the fitted mean stress and the stress gradient are $\sigma_0 = 21.8$ Mpa and $\sigma_1 = 3.6$ MPa, respectively. Under this stress status, two curves match closely. From Fig. 10.13, it can be seen that for short cantilever beams, deflections of the beam are not sensitive to the stress status since the deflections are small. When the length of the cantilever beam is longer than 150 μm and the deflection is larger than 5 μm, the stress status can be clearly identified by the curve-fitting method.

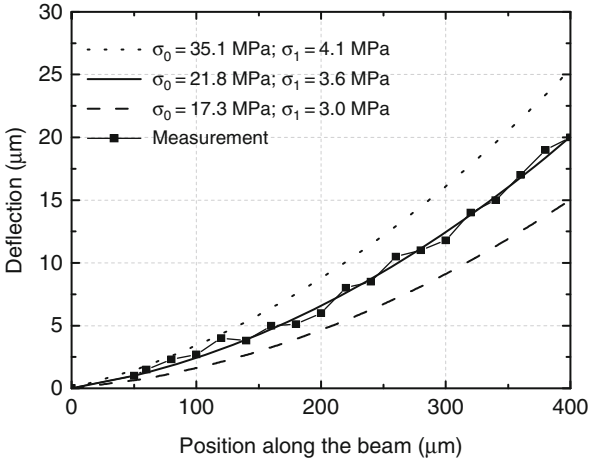
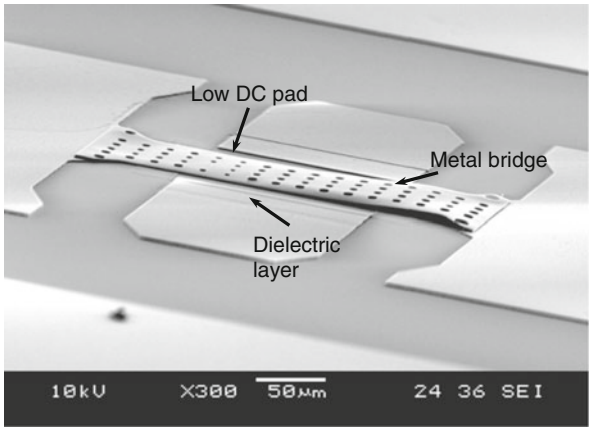


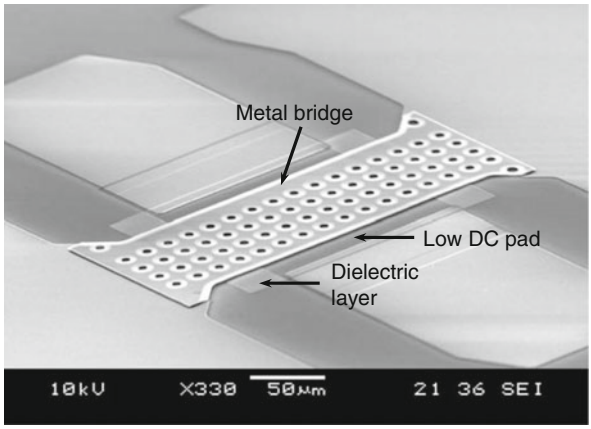
Fig. 10.13 Measured and simulated tip deflection of cantilever beams [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

As mentioned, the intrinsic stress in the metal bridge can cause buckling or curling of the metal bridge. Figure 10.14 shows the two SEM images of capacitive shunt switches released at power of 500 and 430 W, respectively. It is seen that the metal bridge released at 430 W is much flatter than that of the metal bridge released at 500 W.

The effects of the residual stress on the mechanical characteristics of the RF switch can be expressed as



(a)



(b)

Fig. 10.14 SEM images of the fabricated capacitive switches: **(a)** switch with release power of 500 W and **(b)** switch with release power of 430 W [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

$$V_{\mathrm{PI}} = \sqrt{\frac{8k_{\mathrm{eff}}g_0^3}{27\varepsilon_0 wW}} \tag{10.11}$$

$$k_{\mathrm{eff}} = k' + k'' \tag{10.12a}$$

$$k' = 32Ew\left(\frac{t}{l}\right)^3\left(\frac{27}{49}\right) \tag{10.12b}$$

$$k'' = 8\sigma_0(1-\upsilon)w\left(\frac{t}{l}\right)\left(\frac{3}{5}\right) \tag{10.12c}$$

where V_{PI} is the pull-in voltage of the switch, k_{eff} is the effective spring constant of the metal bridge, k' is the stiffness caused by the restoration force of the metal bridge, and k'' is the stiffness caused by the mean residual stress in the metal bridge, g_0 is the initial gap of the switch, w is the width of the metal bridge, W is the width

of the CPW transmission line under the metal bridge, l is the length of the metal bridge, υ is Poisson's ratio of aluminum (Al).

Figure 10.15 shows the variation of k' and k'' with the length of the metal bridge. It can be seen that the spring constant of the metal bridge is mainly determined by the residual stress in the metal bridge. Therefore, the pull-in voltage of the metal bridge is also affected by the residual stress in the metal bridge.

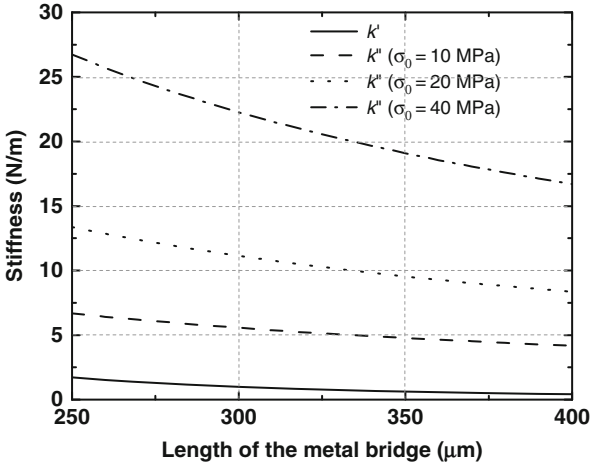


Fig. 10.15 Variation of stiffnesses with length of the metal bridge

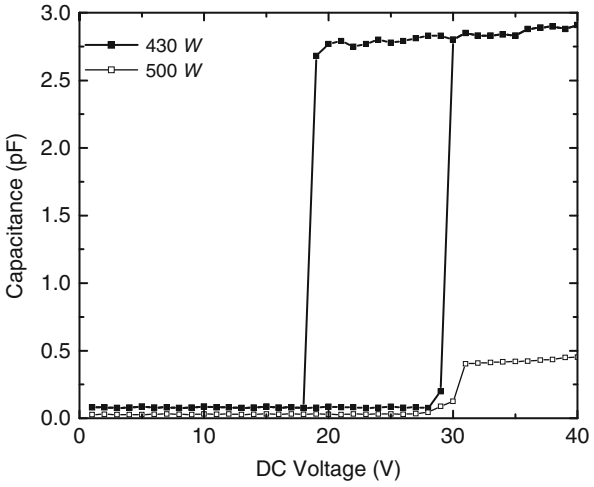


Fig. 10.16 Measured *C–V* curve of the capacitive switch [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

10.3.3 Characterization of Capacitive Switch

Figure 10.16 presents the measured *C–V* curves of the two switches. The curves are measured with an HP 4275A multi-frequency LCR meter with an internal bias option. For the switch with the release power of 500 W, the up-state capacitance is 35 fF and the down-state capacitance is 420 fF even when the applied voltage is as high as 40 V. The metal bridge cannot bounce back after removing the applied voltage because of the high applied voltage. For the switch with release power of 430 W, the pull-down voltage can be clearly identified as 30 V and the hold-down

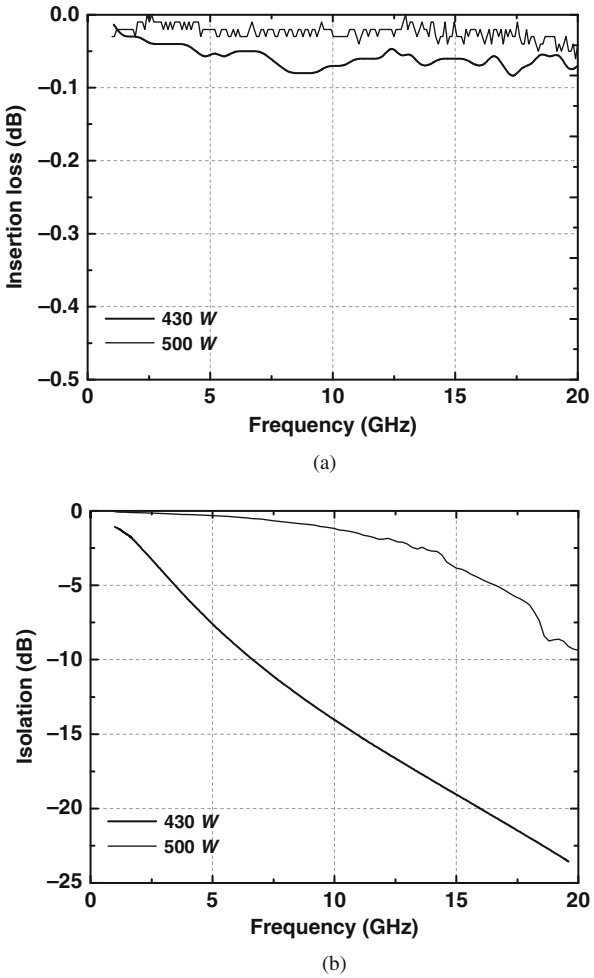


Fig. 10.17 Measured isolation of the two switches at released power of 430 and 500 W: **(a)** up-state and **(b)** down-state [5]. Copyright/used with permission of/courtesy of IOP Publishing Limited

voltage is 20 V. The up-state capacitance is 80 fF and the down-state capacitance is 2.8 pF.

The differences of the capacitance values between the two switches are because that after releasing at 500 W, the metal bridge buckles up due to the compressive stress in it. Therefore, the average gap between the metal bridge and the lower DC pad is larger than the designed value of 2 μm (approximately 4 μm) and the up-state capacitance is only 35 fF. When the metal bridges are driven down, the metal bridge of the switch released at 430 W is flatter than that of the switch released at 500 W; therefore, after the bridge is driven down, the contact between the metal bridge and the lower DC pad is much better for the switch released at 430 W and the down-state capacitance is larger.

Figure 10.17 shows the measured up-state and down-state of RF properties of the two switches. It is seen that for the switch released at 500 W, both the insertion loss and the isolation are smaller than those of the switch released at 430 W. This is because both the up-state and down-state capacitance values are smaller than those of the switch released at 430 W.

10.4 Effects of Surface Roughness

10.4.1 Greenwood–Williamson Model

The modeling of the surface roughness is based on the random process of surface shape. One of the first models which model the contact between two rough surfaces was developed by Greenwood and Williamson [13]. The contact characteristics are statistically studied based on the following assumptions: (a) all asperities on a rough surface have the same radius of curvature, (b) the asperity height is a Gaussian distribution, and (c) the asperities are independent of each other.

The GW model contains three parameters. These are the radius of the spherical asperities, R; the standard deviation of the asperity height, σ_s; and the asperity density, D_{SUM}. The radius of the spherical asperities is assumed to be constant. The standard deviation of the asperity height is assumed to follow a Gaussian distribution. The standard deviation of the asperity height is referred to as root mean square (RMS) roughness when the reference plane is the same as the mean plane [14]. When $\pi R^2 D_{SUM} < 1$, the asperities are assumed to be independent of each other.

In addition to these parameters, three spectral moments of surface topography m_0, m_2, and m_4 are defined as [15, 16]

$$m_k = (2\pi)^n \int_{-\infty}^{\infty} \lambda^n f(\lambda) d\lambda, \quad k = 0,\ 2,\ 4 \tag{10.13}$$

where λ denotes a general spatial frequency in cycles/unit length and $f(\lambda)$ is the spectral density function of the profile. In the space domain, the nth order spectral moments is the mean squared value of the $(n/2)$th derivative of the surface profile. Normally, m_0 is related to the mean square asperity height, m_2 represents the mean square scope, and m_4 indicates the curvature of the surface profiles.

The relationships between the spectral moments and R, σ_s, and D_{SUM} are expressed as [17]

$$\sigma_s^2 = \left(1 - \frac{0.8968}{\alpha}\right) m_0 \tag{10.14a}$$

$$R = \frac{3\sqrt{\pi}}{8\sqrt{m_4}} \tag{10.14b}$$

$$D_{SUM} = \frac{1}{6\sqrt{3}\pi} \frac{m_4}{m_2} \tag{10.14c}$$

where α is the bandwidth parameter and its value depends on the shape and extent of the spectrum of the roughness profile. It is expressed as [11]

$$\alpha = m_0 m_4 / {m_2}^2 \tag{10.15}$$

The spectral moments m_0, m_2, and m_4 can be first calculated from the measured data of the surface topography, then R, σ_s, and DSUM can be obtained from Eqs. (10.14a), (10.14b), (10.14c), and (10.15) [17].

10.4.2 Analysis of Surface Roughness Effects

Figure 10.18 shows the schematic cross section of the capacitive shunt switch with the metal bridge at up-state and down-state positions. The SEM image of the capacitive switch is shown in Fig. 10.19. The planarization of the metal bridge is not realized by fill in the CPW slot under the metal bridge. However, a thin layer of less than 0.5-μm metal film is used as the lower DC pad under the metal bridge. This lower DC pad is also part of the center conductor of the CPW transmission line, which may cause 0.1- to 0.2-dB insertion loss [18]. The reason to use this planarization method is that different materials can be used for the lower DC pad and provide different surface roughness of the capacitance area. When the metal bridge is driven down, the contact area (capacitance area) between the metal bridge and the dielectric layer is affected by the surface roughnesses of the dielectric layer, as shown in Fig. 10.18b. The characteristic impedance of the CPW transmission line is 50 Ω, with dimensions of $W/S/W = 80/150/80$ μm. The gap between the metal bridge and the asperity mean height plane g_{ma} (which is equal to the thickness of the sacrificial layer) is 2 μm, the thickness of the SiN dielectric layer t_d is 0.15 μm, and the width of the metal bridge w is 100 μm. In the following statistical calculation, the metal bridge is assumed to be perfectly planar and smooth. The holes in the metal bridge do not affect the up-state capacitance because the fringing field covers the holes

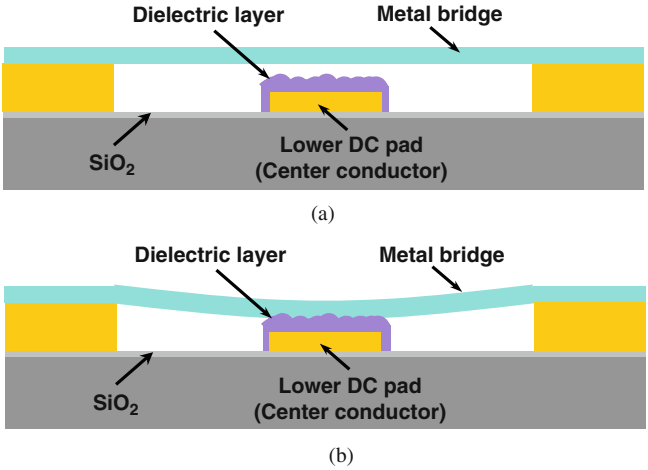


Fig. 10.18 Schematic cross section of capacitive switch: **(a)** up state and **(b)** down state

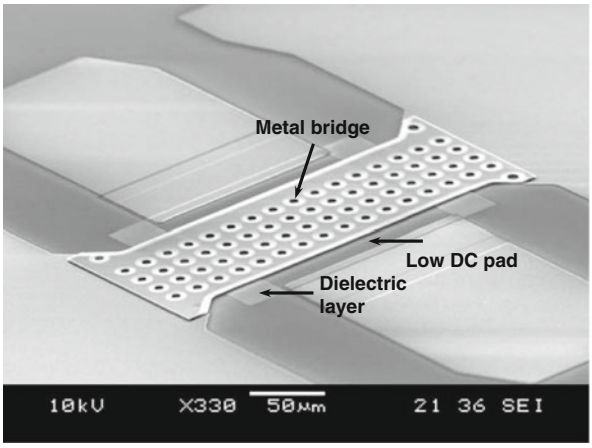


Fig. 10.19 SEM images of capacitive switch [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

completely; while at the down-state of the switch, the apparent contact area and the designed capacitance have removed the area of the holes [18].

There is no contact between the metal bridge and the dielectric layer when the metal bridge is at its up-state position. As shown in Fig. 10.20a, the real up-state capacitance C_u^r can be defined as [20, 21]

$$C_u^r = D_{SUM} A_0 \int_{-3\sigma_s}^{3\sigma_s} \overline{C}(z)\, \phi(z)\, dz \tag{10.16}$$

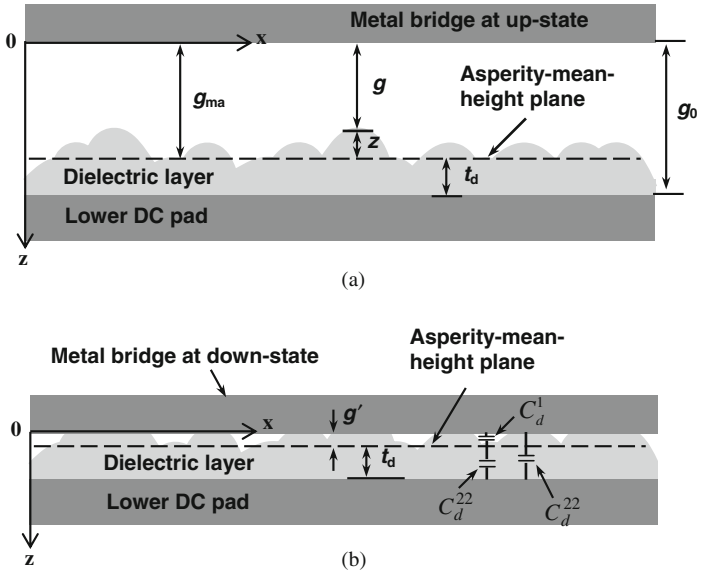


Fig. 10.20 Schematic view of surface roughness with metal bridge: **(a)** up-state position of the switch (not to scale) and **(b)** down-state position of the switch (not to scale) [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

where z is the height of the asperity tips which have a Gaussian distribution. Due to the deposition process of the lower DC pad and the SiN dielectric layer, the RMS roughness can be controlled to 100 nm or smaller [19]. A_0 is the apparent overlap area between the metal bridge and the dielectric layer, $\overline{C}(z)$ is the capacitance from one asperity, and $\phi(z)$ is the Gaussian probability density function. $\overline{C}(z)$ and $\phi(z)$ can be expressed as

$$\overline{C}(z) = 2\pi\varepsilon_0 R \ln\left[1 + \frac{R}{g_{\text{ma}} - z}\right] \tag{10.17}$$

$$\phi(z) = \frac{1}{\sqrt{2\pi}\sigma_{\text{s}}} \exp\left[-0.5\left(\frac{z}{\sigma_{\text{s}}}\right)^2\right] \tag{10.18}$$

where ε_0 is the dielectric constant of air, g_{ma} is the initial gap height between the metal bridge and the asperity mean height plane.

According to Eq. (10.16), the limits of integration are selected to be three times of the standard deviation of the height; 99.7% of surface asperities are included in this range for a Gaussian height distribution function. Therefore, the effect of the vast majority of surface asperities is considered [20].

Substituting Eqs. (10.17) and (10.18) into Eq. (10.16) and assuming

$$\ln\left[1+\frac{R}{g_{\mathrm{ma}}-z}\right]\cong\frac{R}{g_{\mathrm{ma}}-z}$$

when $g_{\mathrm{ma}}-z\gg R$, the real up-state capacitance of Eq. (10.16) can be simplified as

$$C_{\mathrm{u}}^{\mathrm{r}}=C_{\mathrm{u}}^{\mathrm{a}}\sqrt{2\pi}D_{\mathrm{SUM}}R^2\left[2.72+2.66\left(\frac{\sigma_{\mathrm{s}}}{g_{\mathrm{ma}}}\right)^2\right] \tag{10.19}$$

where $C_{\mathrm{u}}^{\mathrm{a}}$ is the apparent up-state capacitance. When the fringing field effect is neglected, $C_{\mathrm{u}}^{\mathrm{a}}$ can be calculated as

$$C_{\mathrm{u}}^{\mathrm{a}}=\frac{1}{\frac{g_{\mathrm{ma}}}{\varepsilon_0 A_0}+\frac{t_{\mathrm{d}}}{\varepsilon_0\varepsilon_{\mathrm{r}}A_0}}=\frac{\varepsilon_0 A_0}{g_{\mathrm{ma}}+\frac{t_{\mathrm{d}}}{\varepsilon_{\mathrm{r}}}}\cong\frac{\varepsilon_0 A_0}{g_{\mathrm{ma}}}\qquad\left(g_{\mathrm{ma}}\gg\frac{t_{\mathrm{d}}}{\varepsilon_{\mathrm{r}}}\right) \tag{10.20}$$

where ε_{r} is the dielectric constant of the SiN dielectric and $\varepsilon_{\mathrm{r}}=7$.

When the switch is at the up-state position, the capacitance is actually two capacitors in series. One is due to the SiN dielectric and is equal to $\varepsilon_0\varepsilon_{\mathrm{r}}A_0/t_{\mathrm{d}}$; another is due to the air gap and is equal to $\varepsilon_0 A_0/g_{\mathrm{ma}}$. However, the capacitance value due to the SiN dielectric is much larger than the capacitance value due to the air gap ($\varepsilon_0\varepsilon_{\mathrm{r}}A_0/t_{\mathrm{d}} > 50\ \varepsilon_0 A_0/g_{\mathrm{ma}}$). Therefore, the capacitor due to the SiN dielectric is negligible.

The normalized up-state capacitance is expressed as

$$C_{\mathrm{u}}^{*}=\frac{C_{\mathrm{u}}^{\mathrm{r}}}{C_{\mathrm{u}}^{\mathrm{a}}}=\sqrt{2\pi}D_{\mathrm{SUM}}R^2\left[2.72+2.66\left(\frac{\sigma_{\mathrm{s}}}{g_{\mathrm{ma}}}\right)^2\right] \tag{10.21}$$

Figure 10.21 shows that the normalized up-state capacitance varies with the RMS roughness for different initial gap heights g_{ma}, assuming $R=40$ nm and $D_{\mathrm{SUM}}=100/\mu m_2$. It is shown that C_{u}^{*} increases with the RMS roughness for a specific g_0.

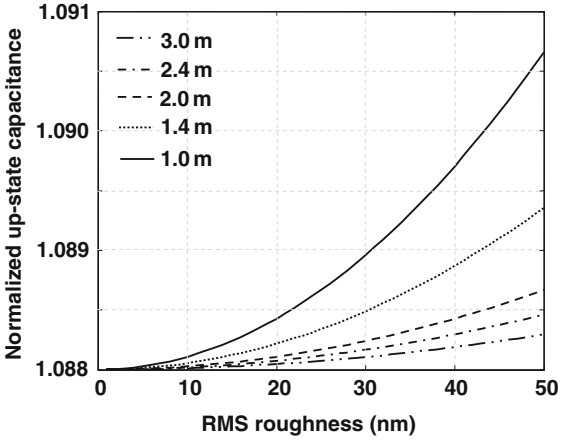


Fig. 10.21 Influence of roughness on the normalized up-state capacitance [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

This is because when the roughness is larger, the equivalent gap between the metal bridge and the asperity mean height plane g_{ma} becomes smaller, since the tips of the asperities are nearer to the metal bridge.

From Fig. 10.21, it is noted that the smaller the initial gap g_0, the larger the normalized up-state capacitance. Generally, when the metal bridge is at the up-state position, the initial gap varies between 1 and 3 μm and the roughness is less than 10 nm. Therefore, according to Fig. 10.21, the increase in capacitance is approximately 9%.

A higher up-state capacitance results in a larger insertion loss. The relationship between the up-state capacitance and the insertion loss can be expressed as

$$S_{21} = 20 \log \left| \frac{1}{1 + j\omega C_u Z_0/2} \right| \tag{10.22}$$

where S_{21} is the insertion loss in decibels, ω is the angular frequency, Z_0 is the characteristic impedance of the CPW line (50 Ω in this example), and C_u is the up-state capacitance.

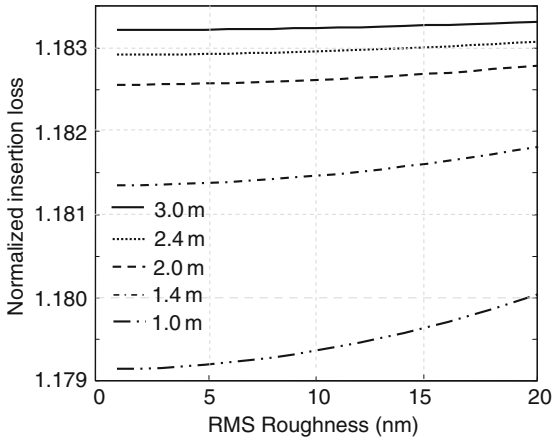
Figure 10.22a shows the normalized up-state insertion loss for different initial gaps at 10 GHz with the RMS roughness varies from 0 to 20 nm, assuming $A_0 = 100 \times 150\ \mu m^2$. The normalized insertion loss is expressed as S_{21}^r/S_{21}^a, where S_{21}^r is the real insertion loss after considering the effect of the surface roughness and S_{21}^a is the insertion loss. It is noted that the normalized insertion loss increases with the RMS roughness. This is because the larger the RMS roughness, the larger the up-state capacitance. Figure 10.22b shows the normalized up-state insertion loss for different initial gaps at 10 GHz with the RMS roughness which is as high as 50 nm. It is observed that the gap lines cross over at 45-nm RMS roughness point. This is because when the RMS roughness is small, the normalized insertion loss is determined mainly by S_{21}^a. When the initial gap is smaller, the insertion loss S_{21}^a is larger. This results in smaller normalized insertion loss for smaller RMS roughness. As the RMS roughness increases, the normalized insertion loss increases with the real insertion loss S_{21}^r and the increase is more significant for a smaller initial gap. At a specific RMS roughness point, the gap lines cross over at a point (45 nm in this chapter) for different initial gaps.

Figure 10.20b shows a schematic cross section when the metal bridge is driven down. The metal bridge contacts high points on the surface of the dielectric layer first, producing real contact at a finite number of asperities.

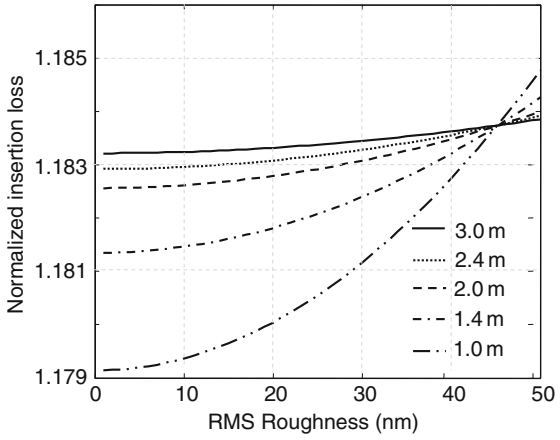
Based on the GW model, the real contact area with respect to the apparent contact area A_0 can be expressed as [15]

$$A^* = \frac{A_c}{A_0} = 0.064(\alpha - 0.8968)^{1/2} \times \int_{g'}^{\infty} \left(\frac{z - g'}{\sigma_s} \right) \phi(z) dz \tag{10.23}$$

where A^* is the normalized contact area, A_c is the real contact area, and g' is the separation between the metal bridge and the asperity mean height plane. As the metal bridge approaches the dielectric layer, g' decreases.



(a)



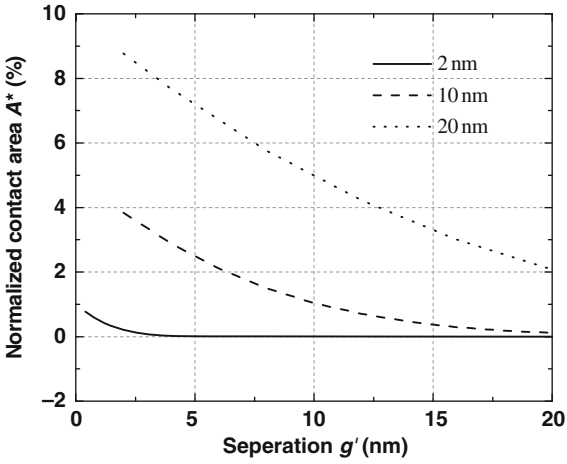
(b)

Fig. 10.22 Influence of *RMS* roughness on the normalized up-state insertion loss: RMS roughness varies **(a)** from 0 to 20 nm and **(b)** from 0 to 50 nm [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited (Copyright IOP Publishing Limited)

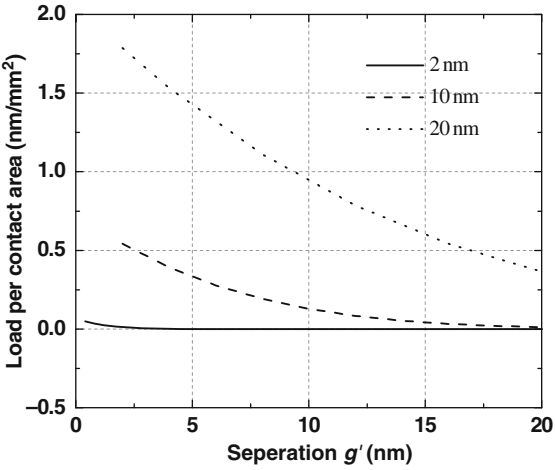
Figure 10.23a shows how the normalized down-state contact area changes with the separation of the two surfaces when σ_s is equal to 2, 10, and 20 nm, respectively. It is observed that A^* is less than 10% and decreases rapidly when the separation increases. When the separation is larger than $3\sigma_s$, the contact area is less than 0.95%. According to the roughness distribution, the separation is larger than most of the RMS roughness and therefore the two surfaces hardly have any contact.

The separation g' is related to the applied load. The total load P with respect to the apparent contact area A_0 can be calculated as [15]

$$P^* = \frac{P}{A_0} = 0.0333E^* m_2^{1/2}(\alpha - 0.8968)^{3/4} \times \int_{g'}^{\infty} \left(\frac{z - g'}{\sigma_s}\right)^{3/2} \phi(z)dz \quad (10.24a)$$



(a)



(b)

Fig. 10.23 **(a)** Variation of normalized contact area with separation and **(b)** variation of load with separation [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

$$E^* = \left(\frac{1 - \upsilon_1^2}{E_1} + \frac{1 - \upsilon_2^2}{E_2} \right)^{-1} \tag{10.24b}$$

where E^* is the combination of Poisson's ratios and Young's moduli of the metal bridge and the SiN layer. In the study, $E_1 = 70$ GPa, $\upsilon_1 = 0.35$ for the metal bridge (Al) [22] and $E_2 = 295$ GPa, $\upsilon_2 = 0.25$ for the SiN dielectric layer [23].

The effect of the applied load on the separation g' is shown in Fig. 10.23b. The separation is smaller when the applied load is larger. This is because a larger applied load forces the asperities to deform elastically and pushes the two surfaces nearer.

The load P on the switch comes from the combination of the electrostatic force and the mechanical restoring force. When the metal bridge is driven down, a DC bias voltage which is called hold-down voltage is needed to balance the mechanical restoring force and to hold the metal bridge at the down-state position. As a result, the load P on the metal bridge can be simplified as

$$P = F_{\mathrm{e}} - F_{\mathrm{k}} \tag{10.25a}$$

$$F_{\mathrm{e}} = \frac{1}{2} C_{\mathrm{d}}^{\mathrm{r}} \frac{V^2}{t_{\mathrm{d}}} \tag{10.25b}$$

$$F_{\mathrm{k}} = k(g_0 - t_{\mathrm{d}} - g') \tag{10.25c}$$

where F_{e} and F_{k} are the electrostatic force and the mechanical restoring force, respectively. $C_{\mathrm{d}}^{\mathrm{r}}$ is the real down-state capacitance, k is the effective spring constant, t_{d} is the thickness of dielectric layer, and V is the applied hold-down voltage.

When all the asperities are assumed to be independent of one another, the real down-state capacitance can be expressed as

$$C_{\mathrm{d}}^{\mathrm{r}} = C_{\mathrm{d}}^{1} + C_{\mathrm{d}}^{2} \tag{10.26}$$

where C_{d}^{1} is the capacitance results from the area where the metal bridge contacts with the SiN surface, while C_{d}^{2} is the capacitance results from the area where the metal bridge does not contact with the SiN surface. The C_{d}^{2} can be further divided into two parts, C_{d}^{21} and C_{d}^{22}, which come from the air gap between the metal bridge and the SiN and the SiN itself, as illustrated in Fig. 10.20b. For simplicity, all these micro-capacitors are assumed as parallel plate capacitors that can be expressed as

$$C_{\mathrm{d}}^{1} = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}} A_0 A^*}{t_{\mathrm{d}} + g'} \tag{10.27}$$

$$\frac{1}{C_{\mathrm{d}}^{2}} = \frac{1}{C_{\mathrm{d}}^{21}} + \frac{1}{C_{\mathrm{d}}^{22}} \tag{10.28a}$$

where

$$C_{\mathrm{d}}^{21} = \frac{\varepsilon_0 A_0 (1 - A^*)}{g'} \tag{10.28b}$$

$$C_{\mathrm{d}}^{22} = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}} A_0 (1 - A^*)}{t_{\mathrm{d}}} \tag{10.28c}$$

where ε_{r} is the dielectric constant of SiN.

Therefore, the normalized down-state capacitance can be expressed as

$$C_{\mathrm{d}}^{*} = \frac{C_{\mathrm{d}}^{\mathrm{r}}}{C_{\mathrm{d}}^{\mathrm{a}}} \tag{10.29}$$

where C_d^a is the apparent down-state capacitance which can be expressed as

$$C_d^a = \frac{\varepsilon_0 \varepsilon_r A_0}{t_d} \tag{10.30}$$

Based on Eqs. (10.23), (10.24a), (10.24b), (10.25a), (10.25b), (10.25c), (10.26), (10.27), (10.28a), (10.28b), (10.28c), (10.29), and (10.30), Fig. 10.24 shows how the normalized contact area changes with the applied hold-down voltage. The effective stiffness k is assumed to be 40 N/m. It is seen that the normalized contact area increases with the applied hold-down voltage for the same roughness; when the applied hold-down voltage is kept constant, the larger the roughness, the smaller the normalized contact area.

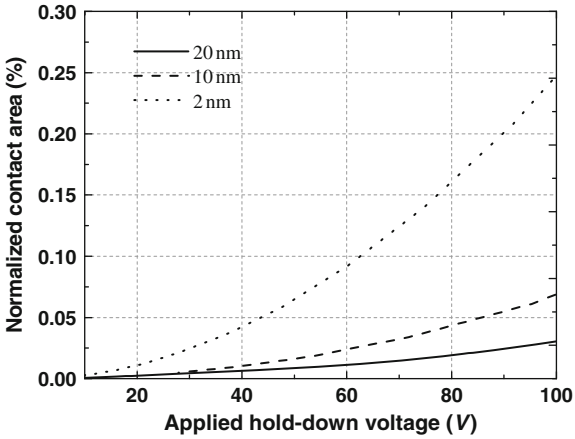


Fig. 10.24 Variation of normalized contact area with applied hold-down voltage [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

Figure 10.25a shows the variation of C_d^1 with the applied hold-down voltage when the RMS roughness σ_s is equal to 2 nm, Fig. 10.25bb presents C_d^{21}, C_d^{22}, and C_d^2 change with the applied hold-down voltage, and Fig. 10.25c shows the variation of C_d^r and C_d^* with the applied hold-down voltage. As a result, it is interesting to conclude that (a) the down-state capacitance increases with the applied hold-down voltage and (b) C_d^2 is much larger than C_d^1; therefore, C_d^r is mainly determined by C_d^2, which means that the down-state capacitance of the capacitive switch is actually determined by the capacitance area where the metal bridge does not contact with the SiN surface.

Figures 10.24 and 10.25 can be explained as the average load P added between the metal bridge and the rough surface increases with the applied hold-down voltage. Therefore, when the gap g' becomes smaller the down-state capacitance becomes larger.

The variations of C_d^1, C_d^2, C_d^r, and C_d^* with the applied hold-down voltage for different RMS roughnesses σ_s are shown in Fig. 10.26. It can be concluded that

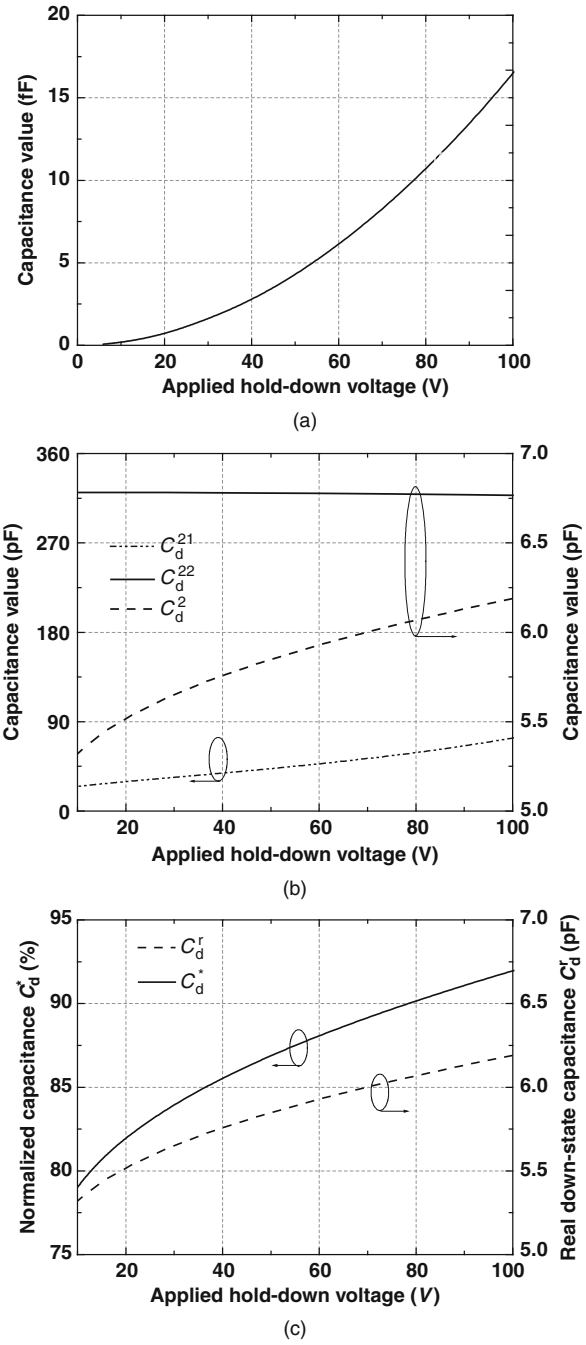


Fig. 10.25 Variation of down-state capacitance with applied hold-down voltage for 2 nm RMS roughness: **(a)** C_d; **(b)** $C_d{}^{21}$, $C_d{}^{22}$, and $C_d{}^2$; and (**c**) $C_d{}^r$ and $C_d{}^*$ [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

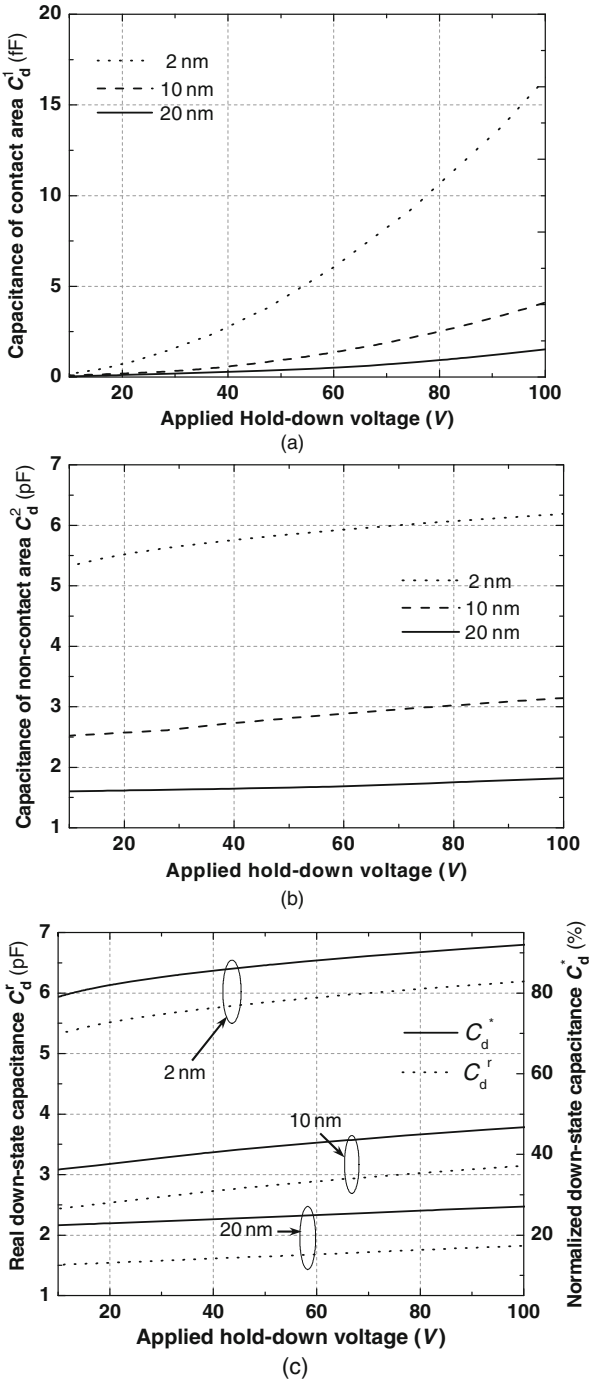


Fig. 10.26 Variation of down-state capacitance with the applied hold-down voltage: **(a)** C_d^1, **(b)** C_d^2, and **(c)** C_d^r and C_d^* [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

when the RMS roughness increases, all the C_d^1, C_d^2, C_d^r, and C_d^* decrease for the same hold-down voltage.

The reduction in the down-state capacitance leads to a smaller isolation when the metal bridge is driven down. The relationship between the down-state capacitance and the isolation can also be calculated according to Eq. (3.6), where C_u is replaced by the down-state capacitance C_d and S_{21} is the down-state isolation. Assuming $A_0 = 100 \times 150\ \mu m^2$ and $t_d = 0.15\ \mu m$, the relationship between the normalized down-state isolation and the applied hold-down voltage at 10 GHz is shown in Fig. 10.27. It can be seen that the isolation increases with the applied hold-down voltage slowly but decreases as the RMS roughness increases. This variation can be attributed to the fact that the real down-state capacitance increases with the hold-down voltage and decreases with the RMS roughness.

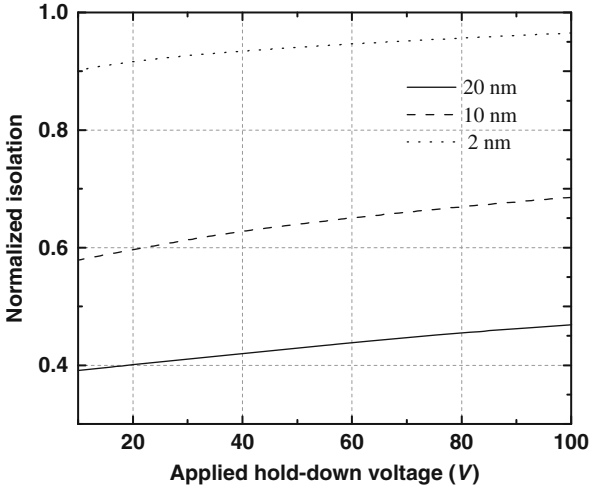


Fig. 10.27 Variation of normalized isolation with the applied hold-down voltage [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

10.4.3 Experimental Results and Discussions

The roughness of the dielectric layer arises from the dielectric itself and, more importantly, from the lower DC pad surface damaged by the fabrication steps at elevated temperature, such as the dielectric layer deposition process. The commonly used dielectric layer is SiN which is deposited by PECVD within the temperature range of 250–300°C. High temperature leads to the so-called hillock [24–26] or larger grain size of the metal thin film [27]. The driving force is the compressive stress caused by a large mismatch of thermal expansion coefficients between the metal film and the material under it. It is believed that high strength material, such as Ti and refractory metals, deposited with free of pinholes can reduce this effect.

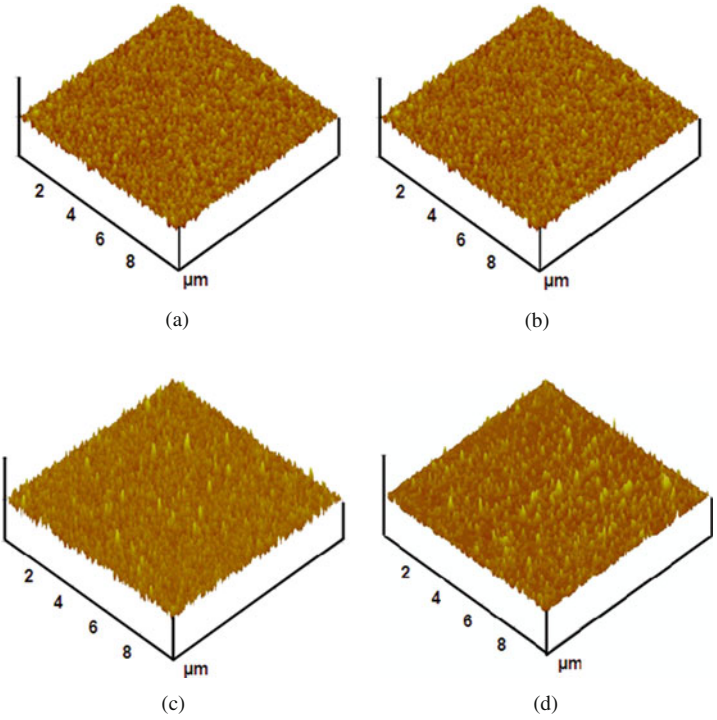


Fig. 10.28 Surface roughness of different metal thin films after sputtering: **(a)** Ti, **(b)** Cr, **(c)** Al, and **(d)** Cu (the thickness of all metal films is 0.5 μm) [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

However, the refractory metal usually has lower resistivity and hence leads to a higher insertion loss in the CPW transmission line.

Figure 10.28 shows the surface roughness for different metal thin films after sputtering. The surface roughness is examined with an atomic force microscopy (AFM). The substrates used are Si substrate with 2-μm PECVD SiO_2 deposited on them. The metal thickness is 0.5 μm. It can be seen that all these metal surfaces have similar roughness under the state of sputtering. However, their surface roughness changes differently after a 0.15-μm SiN is deposited on these metal films that used as lower DC pad as shown in Fig. 10.29. For Cr and Ti thin films, the roughness is almost the same, while for Al and Cu, the roughness becomes larger. The increase in the roughness of Al thin film is mainly caused by the "hillock" produced in the film whereas for the Cu thin film it is mainly because of the agglomeration and coalescence of grains. All the parameters of the metal layer are calculated using the GW model based on the measured roughness data listed in Table 10.3.

Figure 10.30a shows the measurement results of the insertion loss of the switches with different types of metallic thin film under the SiN layer. The insertion losses have been de-embedded by subtracting the insertion loss of the CPW transmission

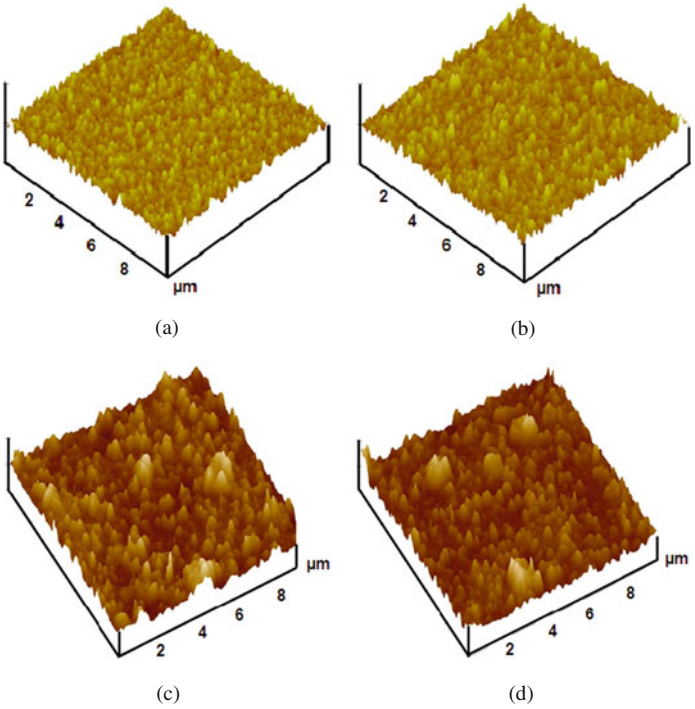


Fig. 10.29 Surface roughness of different metal thin films after SiN deposition: **(a)** Ti, **(b)** Cr, **(c)** Al, and **(d)** Cu (the thickness of SiN is 0.15 μm) [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

Table 10.3 Parameters of surface roughness characterization for different metal thin films before and after SiN deposition

		σ_s (nm)	R (nm)	D_{SUM} (/μm^2)	m_0 (nm^2)	m_2	m_4 (/μm^2)
Before	T_i	2.162	30.05	160	169	0.0935	489
	C_r	3.067	35.50	101	262	0.1060	350
	Al	4.196	39.50	99	260	0.0875	283
	C_u	4.314	48.15	95	270	0.0618	192
After	T_i	2.192	31.11	158	159	0.0831	456
	C_r	4.471	41.05	96	266	0.0835	262
	Al	12.29	59.18	50	398	0.0771	126
	C_u	14.81	63.22	41	450	0.0828	111

line without the MEMS switches; therefore, these losses are mainly due to the up-state capacitance value. It can be seen that the larger the RMS roughness of the film, the higher the insertion loss. This is consistent with the theoretical analysis results. The ripples in the measured insertion loss are due to the measurement noise. Table 10.4 lists the calculated and measured normalized up-state capacitance and insertion loss. It can be seen that the measured up-state capacitance and isolation

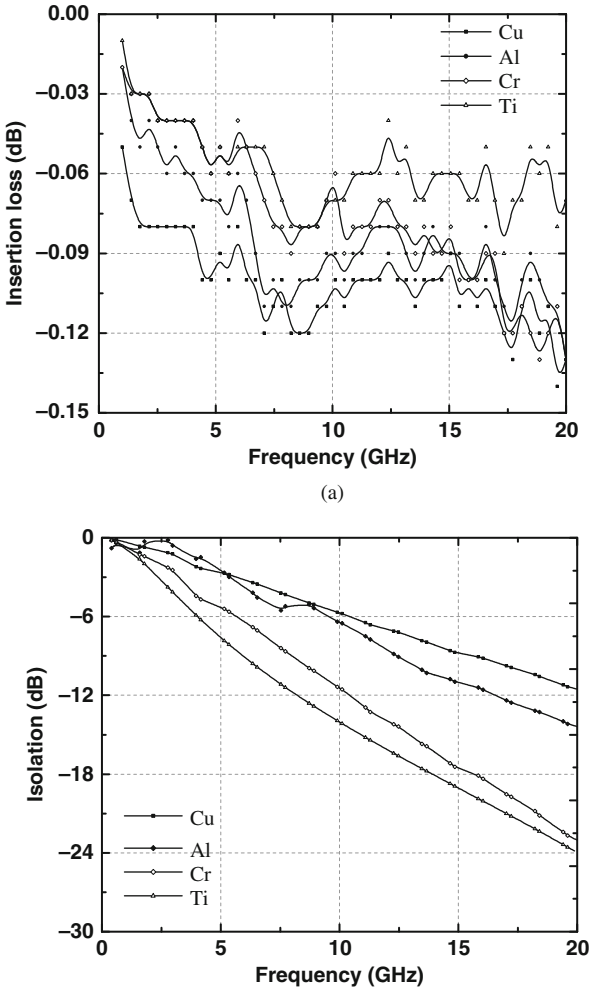


Fig. 10.30 Measurement results of RF properties versus different metal materials: **(a)** insertion loss and **(b)** isolation (with applied hold-down voltage of 30 V) [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

Table 10.4 Comparison of calculated and measured normalized up-state capacitance and insertion loss (10 GHz)

		Ti	Cr	Al	Cu
Capacitance	Calculation	1.08	1.21	1.41	1.39
	Measurement	1.21	1.24	1.47	1.51
Insertion loss	Calculation	1.04	1.10	1.19	1.18
	Measurement	1.47	1.51	2.16	3.25

Table 10.5 Comparison of calculated and measured normalized down-state capacitance and isolation (10 GHz with 30-V hold-down voltage)

		Ti	Cr	Al	Cu
Capacitance	Calculation	0.75	0.68	0.32	0.29
	Measurement	0.53	0.35	0.25	0.22
Isolation	Calculation	0.88	0.83	0.53	0.50
	Measurement	0.69	0.56	0.41	0.37

increase with the RMS roughness. However, the measured capacitance values and insertion loss are higher than the calculated values. This is because the calculation does not consider the capacitance of the fringing field effect.

Figure 10.30b shows the measurement results of the isolation when the metal bridge is driven down. It is obvious that the isolation of the switches with Cu or Al thin films under the SiN dielectric layer is lower compared to the isolation of the switches with Ti or Cr thin films. This is because the RMS roughness of Cu or Al thin film is larger. Table 10.5 provides the calculated and measured normalized down-state capacitance and isolation. It can be observed that the measured normalized down-state capacitance and the isolation are much smaller than the calculated values. This is because only the effect of the surface roughness is considered in the calculation. Actually, besides the surface roughness, other factors such as non-planarization of the metal bridge and via hole in the metal bridge also have significant impact on the down-state capacitance and the isolation.

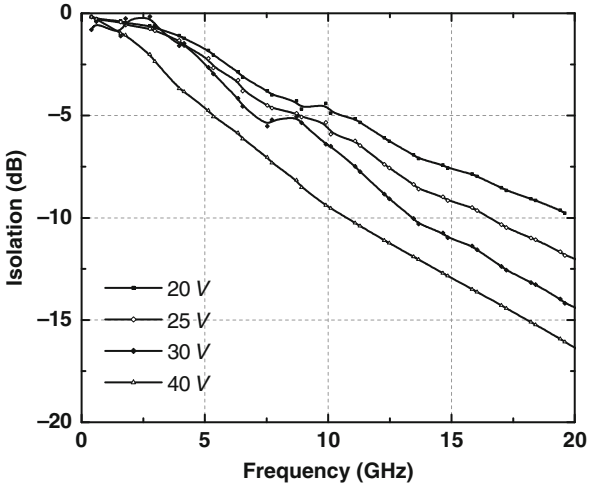


Fig. 10.31 Measurement results of the variations of isolation with the applied hold-down voltage with Al thin film under the SiN layer [19]. Copyright/used with permission of/courtesy of IOP Publishing Limited

Figure 10.31 indicates the relationship between the measured isolation and the hold-down voltage when Al metal film is deposited under the SiN layer. It is shown that the higher the applied hold-down voltage, the higher the isolation. This further re-enforces the prediction in Fig. 10.27.

10.5 Summary

The fabrication process of the capacitive switches, especially the dry etching of the sacrificial photoresist with the oxygen plasma, is characterized and optimized. For the dry etching process, the etching rate of the sacrificial photoresist increases with etching power and oxygen pressure. However, when the etching power is higher than 500 W, the metal bridges are easily damaged. The intrinsic stress in the metal film can be divided into the mean stress and the stress gradient which are determined by the curve fitting of the measured deflection of the cantilever beams and the stress model. For the dry releasing process, when the release power is higher than 500 W, the negative stress gradient in the metal bridge leads to the warp up of the metal bridge and hence increases the pull-down voltage of the metal bridge. The optimized etching power and oxygen pressure used in the releasing process are 430 W and 500 mTorr, respectively.

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