55. Packaging Materials

This chapter is a high-level overview of the materials used in an electronic package including: metals used as conductors in the package, ceramics and glasses used as dielectrics or insulators and polymers used as insulators and, in a composite form, as conductors. There is a need for new materials to meet the ever-changing requirements for high-speed digital and radio-frequency (RF) applications. There are different requirements for digital and RF packages that translate into the need for unique materials for each application. The interconnect and dielectric (insulating) requirements are presented for each application and the relevant materials properties and characteristics are discussed. The fundamental materials characteristics are: dielectric constant, dielectric loss, thermal and electric conductivity, resistivity, moisture absorption, glass-transition temperature, strength, time-dependent deformation (creep), and fracture toughness. The materials characteristics and properties are dependant on how they are processed to form the electronic package so the fundamentals of electronic packaging processes are discussed including wirebonding, solder interconnects, flip-chip interconnects, underfill for flip chip and overmolding. The relevant materials properties are given along with requirements (including environmentally friendly Pb-free packages) that require new materials to be developed to meet future electronics needs for both digital and RF applications.

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An electronic package is a configuration of materials that interconnects electronic signals form one area to another. This scheme must isolate these signals so that there is no interference and must also protect the electronics from a degrading environment. A package typically consists of the semiconductor, mounted and interconnected (with solder or Au wires) to a dielectric substrate (with a leadframe or with metal traces), which is encapsulated to seal the device from the environment. The electronic package must serve four functions:

- provide electrical (or photonic) contact to and from the chip,
- act as an electrical space transformer to take electronic functionality from the dense surface of the chip to the coarser pitched *outside world*,
- provide environmental isolation to the semiconductor, and
- provide an avenue for conduction of heat away from the device.

In the past, advances in silicon semiconductors had little or no affect on the electronic package design or process. New advances in silicon devices have driven increases in chip speed, device density (e.g., the number of transistors/mm^2), and power dissipation. These changes, and those planned in the future, require larger numbers of interconnects to and from the devices, improved electrical performance, more effective thermal management, software systems to design and model the assembly, and different sets of materials to make these changes happen. Furthermore, the package is shrinking to a minimalist version of the products that traditionally have been called packaging. The chip and board have become a conjugate packaging system that must provide the traditional levels of electrical, mechanical, thermal interfaces, and environmental protection, with the additional challenge of increased performance. Furthermore, the boundary between where the device ends and where the package begins has become blurred with passive devices (e.g., resistors, capacitors, etc.) in the package and redistribution layers that act as space transformers on the chip. Electronic packaging is becoming one of the greatest challenges in manufacturability, performance, and reliability in advanced electronics applications. With the tremendous growth of wireless telecommunication, radio-frequency (RF) applications are beginning to drive many areas of microelectronics traditionally led by the development of the microprocessor. An increasingly dominant factor in RF microelectronics is electronic packaging and the materials needed to create the package, because the package materials strongly affect the performance of the RF electronics. Many challenges also remain for packaging of microprocessors. These challenges include increased speed, numbers of input/output (I/O), decreased pitch, and decreased cost.

55.1 Package Applications

Electronic packages are divided into four levels, three of which exist beyond the integrated circuit.

Level 0: semiconductor chip level (integrated circuits). The materials are the semiconductor (Si, SiGe, GaAs, etc.), metallization on the circuit (Al, Cu, Au) and interconnects on the die.

Level 1: chip in a carrier. The die is bonded (with a conductive, or nonconductive, adhesive or solder)

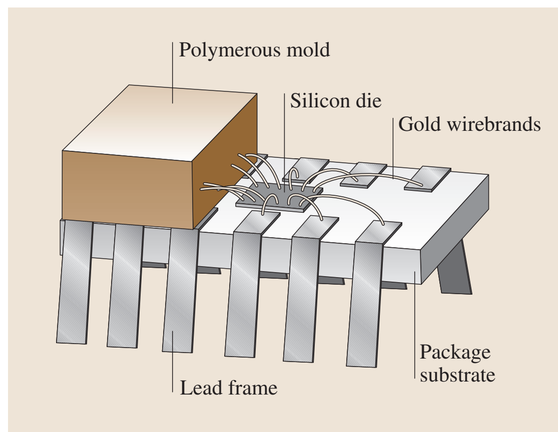

Fig. 55.1 Isometric section schematic that illustrates a peripheral package showing a dual-in-line package (DiP) that is wirebonded

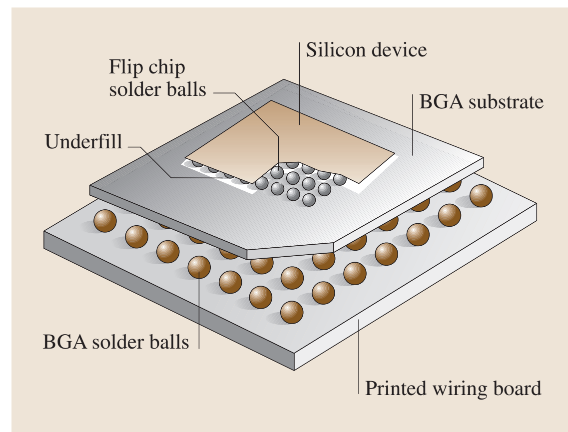

Fig. 55.2 Schematic illustration of an area-array package with a flip-chip device interconnect and a ball grid array package

into a package carrier (substrate or leadframe) and interconnected by either wirebonds or bulk conductive interconnects (flip chip) of solder or conductive adhesives. An example of a wirebonded package is shown in Fig. 55.1, while Fig. 55.2 shows a flip-chip package interconnect. The die is protected either by a lid or encapsulated with a polymer overmold.

Level 2: the chip carrier mounted to a board. The package is solder, or conductive adhesive, attached to a circuit board. An example of a package mounted to a board using area array interconnects is shown in Fig. 55.2.

Level 3: board-to-board interconnects. The boards are interconnected to the final electronic system using friction interconnects, solder interconnects, or fiber-optic connectors.

55.2 The Materials Challenge of Electronic Packaging

Electronic packaging is arguably the most materials-intensive application today. The families of materials included in a package include: semiconductors, ceramics, glasses, composites, polymers, and metals. A list of the types of materials used in an electronic package are shown in Table 55.1. The processes required to assemble a package are equally varied: welding, soldering, curing, cold and hot working, sintering, adhesive bonding, laser drilling, and etching.

Each of these materials and how it is used in an electronic package could be the topic of an entire book. This chapter is a high-level overview of the materials used in an electronic package. The focus is on the following classes of materials:

Metals are used as conductors in the package, primarily electrical but also thermal for power devices. This includes the thin metal interconnects on the integrated circuit made of Al, Cu or Au and the interconnects between the integrated circuit and the package that are either wirebond interconnects or solder joints. Metals are also used to act as heat sinks for power devices and as shields for RF applications.

Table 55.1 Examples of materials used in electronic packaging

Semiconductors	Si, SiGe, GaAs
Metals	Solders for interconnects (Sn–Pb, Sn–Ag, Sn–Ag–Cu, Sn–Au, Sn–Sb) Au wirebonds Cu leadframes (Kovar, CuBe, Alloy 42) Cu traces in substrates W, Mo traces in co-fired ceramics Ag, Au, Pd for thin/thick films on ceramics Ni diffusion barrier metallizations Al heat sinks
Ceramics	Al_2O_3 substrates modified with BaO, SiO_2, CuO, etc. LTCC substrates Al_2O_3 modified with low-temperature glass (e.g., PbO) SiN dielectrics Diamond heatsinks
Polymers	Epoxies (overmold) Filled epoxies (overmold) Silica-filled anhydride resin (underfills) Conductive adhesives (die bonding, interconnects) Laminated epoxy/glass substrates Polyimide dielectric Benzoyclobutene Silicones Photosensitive polymers for photomasks (acrylates, monomers, etc.)
Glasses	SiO_2 fibers for optoelectronics Silicate glasses for sealing Borosilicate glass substrates Glass fibers for epoxy/glass substrates (FR-4)

Ceramics and glasses are used as dielectrics or insulators. Ceramics are used in devices as dielectrics to form capacitors and inductors. In the package itself, the ceramics are used as insulating materials for substrates that provide a structural base that electrically isolates lines and pads.

Polymers are used as insulators and, in a composite form, as conductors. As an insulator, polymers are encapsulants, underfills and substrates (note: in these applications, polymers are used as composites with silica or glass fillers). Polymers are also used as insulating adhesives to glue components to a substrate or board to provide mechanical strength. The addition of metal particles to the polymer can make it a conductive material as a conductive adhesive interconnect.

Composite materials are a mix of materials that can be tailored for either mechanical behavior improvements or thermal enhancement as an electrical conductor. Many of the composite materials used in packages are based on a polymer matrix, as noted in the polymer section above.

There is a wealth of general information on materials in electronic packaging. Some additional resources are found in [55.1–8].

55.2.1 Materials Issues in High-Speed Digital Packaging

The ability to decrease line width and feature size in semiconductor technology is decreasing below 90 nm. As the feature size shrinks, the function per unit area on the die increases. This increased functionality means either smaller die or more I/O per die. The reduced die size also reduces the available perimeter of the package for wirebond pads while increased functionality requires more I/O. The decreased perimeter area also drives wirebond capability down to 44-μm pitch with 10-μm gold wire. An attractive solution to this decreasing size is to use the entire surface of the chip (flip chip) rather than just the periphery (wirebond). Figure 55.3 shows a comparison of available I/O for a given chip size for standard, and state-of-the-art, wirebond and flip-chip pitch.

From an overall digital package perspective, the trend is to move from perimeter-bonded die and packages, to array packages, then to array die bonds in an array package that offers increased numbers of I/O and performance potential. This trend is shown in Fig. 55.4. Materials used in the package and substrate [e.g., ceramic (Al_2O_3), low-temperature co-fired ceramic (LTCC) and organic laminants] and the package style affect performance as well as area array versus peripheral interconnects. Ceramic packages are the material of choice for hermetic high-performance applications. Ceramic is typically 96% Al_2O_3 with tungsten metallization. The ceramic is fired and sinters at high temperatures that precludes the use of Cu or Al metallization that would melt in the ceramic sintering process. Multilayer ceramic packages with thin-film metallizations also offer a thermal expansion coefficient similar

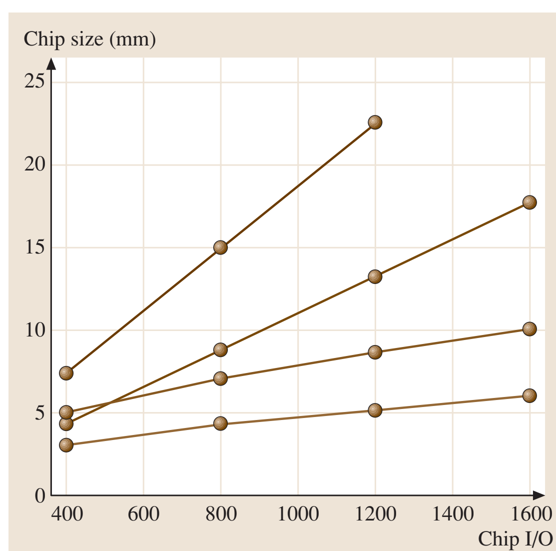

Fig. 55.3 Plot of bond pitch requirements as a function of I/O and die size for current wire bond (75 μm) and flip chip (250 μm) and state-of-the-art wirebond (44 μm) and flip chip (150 μm)

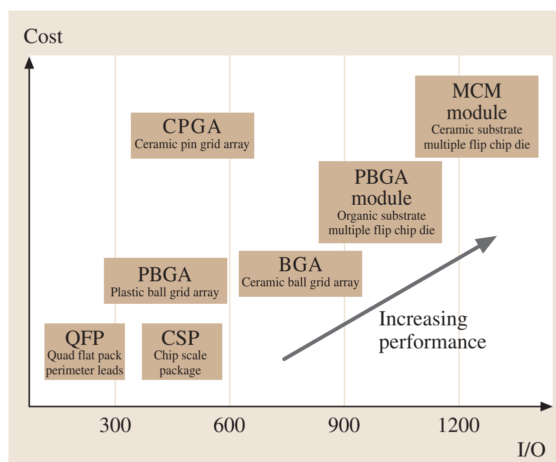

Fig. 55.4 Plot of package style as a function of cost and I/O

Table 55.2 Dielectric constants of packaging substrate materials

Material	Dielectric constant (ε_r)
Epoxy	5.0
FR-4	3.5–4.0
Other laminates	2.5–4.5
Kapton	3.1–3.5
Multilayer ceramic	5.0–9.5
Low-temperature co-fired ceramic (LTCC)	3.9–7.8

to the Si die (6×10^{-6} /°C for alumina ceramic versus 3×10^{-6} /°C for Si) so strain that may arise during thermal cycling can be minimized. However, Al_2O_3 ceramic is expensive and has limited use in commercial applications. LTCC is growing in interest because it offers the hermeticity and thermal expansion advantageous of ceramic at a lower cost. LTCC is an alumina ceramic/glass composite that is fired at sufficiently low temperatures that Cu or Ag can be used as the metallization.

For the interconnects in the package, flip chip appears to provide substantial improvements in I/O and pitch but wirebonding will remain as a packaging solution because there is a great deal of capital invested in wirebond equipment that cannot be ignored.

In addition to smaller size driving finer pitch, increased signal speed will drive package requirements. Digital signal delays must be minimized. The total delay is a function of the total distance and the delay per unit length, which is a function of the transmitting medium's dielectric constant and is the square root of the dielectric constant (ε_r) times the free-space delay in vacuum (33 ps/cm). Therefore, a material with a high dielectric constant increases the delay. Table 55.2 shows a variety of dielectric constants used in packaging.

For minimal signal delays, an optimal dielectric substrate material is required. The signal length can also be shortened by changing from a wirebond solution to flip chip.

55.2.2 RF Packaging Materials Issues

High-speed and microwave circuits are defined for digital devices with clock speeds faster than 100 MHz and 0.1–100 GHz for analog circuits. For analog, these are also termed radio-frequency (RF) circuits. The microwave, or RF, circuit module is defined by microstrip elements composed of transmission lines and matching networks on a substrate with discrete components (resistors, inductors, capacitors and transistors)

Table 55.3 Coefficients of thermal expansion of a sampling of materials used in area-array electronic packages

Material	CTE (10^{-6} /°C)
Metals	
304 Stainless Steel	17.8
Ag	19.7
Al	23.5
Alloy 42	4.9
Au	14.2
Cu	16.8
Invar	1.6
Kovar	5.5
Mo	5.1
Ni	13–15
Solder: 63Sn–37Pb	25
Solder: 95Pb–5Sn	28
Ti	10
W	4.5
Ceramics	
AlN	4.3
Alumina (96%)	6.4
Alumina (99.5%)	6.5
BeO	7.8
BN	3.7
Fused silica glass	0.56
Quartz	13
SiC	3.8
SiN	3
Semiconductors	
GaAs	5.8
Si	2.7
Organic materials	
Epoxy resins	50–80
FR-4 (x–y plane)	15.8
FR-4 (z-axis)	80–90
Polycarbonates	50–70
Polyimide glass (x–y plane)	12–14
Polyimide glass (z-axis)	60
Polyimides	40–50
Polyurethanes	180–250
RTV (room temperature vulcanized) polymer	800
Sylgard	300

attached, or embedded, in the substrate. A monolithic microwave device has all the above elements integrated onto a semiconductor die. The semiconductor used for RF applications is typically GaAs because of its high resistivity and suitability for circuits that operate at high

frequencies. The following is a discussion of critical packaging materials issue related to RF devices and modules.

One of the most significant differences between RF and digital packaging is that the package is part of the RF circuit due to the interaction of the RF electric field with all adjacent conductors and insulators. This is one of the most significant challenges in the design of RF circuits. This will be further exacerbated as the trend moves from single-die RF packages to multiple die with passive components in RF modules. For example, the wireless-communication industry is striving toward a solution of a *phone in a package* where the entire electronic functionality of a cellular phone can fit into a package with a size on the order of 1 cm^2. Materials used in the package of these RF applications are significant for the performance and cost of the solution.

It is clear that the electronic package is a complex materials system that is driven by a variety of thermal, mechanical and electrical performance requirements. These requirements are also application dependent for both digital and RF packages. The remainder of this chapter is an overview of the key materials required for microelectronic packaging.

55.3 Materials Coefficient of Thermal Expansion

The coefficient of thermal expansion (CTE) is the length of increase of a macroscopic sample for a given temperature increase. The units of the CTE are length/length°C. The CTE is a critical physical property of materials used in an area array package. A wide variety of materials with a wide variety of CTEs, such as metals, ceramics, and polymers are joined together in an electronic package assembly. As processing (or in-use) temperatures change, the materials expand or contract to various degrees that could result in the formation of extensive and nonuniform strains in the package assembly. A set of materials typically used in electronic packages and their CTEs are shown in Table 55.3.

55.4 Wirebond Materials

Wirebonding is the process where a thin wire (that can be less than 25 μm in diameter) made of Au or Al is bonded to the surface of an integrated circuit, then to a pad or leadframe in the package (Fig. 55.1). Gold-ball thermosonic bonding is the typical method used to form these interconnects. The thermocompression bond is a weld between two metals where thermal energy (preheating of the capillary tool and wire), force and ultrasonic energy are imparted to the wire, causing it to melt on the surface and rapidly interdiffuse with the bond pad to form a joint. The integrated circuit pad's surface finish is typically Al or Au and the package bond pad finish is typically Au or Cu.

55.4.1 Wirebonds for Digital Applications

The challenges for decreased wirebond pitch are primarily process related to accurate machine control to move bonding heads to shorter distances (44-μm pitch) with increased accuracy. However, there are also materials challenges. The metallurgical challenges of wirebonding Au to Al have been well addressed. The classic, early failures were dominated by *purple plague* and the definitive work in this area is by *Philofsky* [55.9]. Purple plague resulted when the Au of the wirebond extensively reacting with Al to form brittle $AuAl_2$ that resulted in bond failures. (Purple plague derives its name from the purple tinge of the $AuAl_2$ intermetallic.) This was addressed by reducing the wirebond process temperature to below 300 °C, which reduces the extent of $AuAl_2$ formation. Current wirebond failures are the result of surface impurities or corrosion. These are addressed by plasma or ultraviolet (UV)–ozone cleaning of the surface prior to wirebonding.

Wirebonding problems have also been caused by plating impurities in Au bond pads. Impurities in the Au diffuse to the molten front that occurs during wirebonding and concentrate in a plane in the bond. If there are a sufficient number of impurities, they precipitate and act as sinks for vacancies that can become voids and lower the bond strength. The impurities have been identified as Ni, Fe, Co and B [55.10]. The contaminants are present in the Au film as a result of the plating process. This can be addressed by optimizing the plating process to form pure metallic Au.

With finer-pitch wirebonding comes the requirement for thinner Au wire, approaching 10 μm in diameter. This thin wire poses a materials challenge. The wire

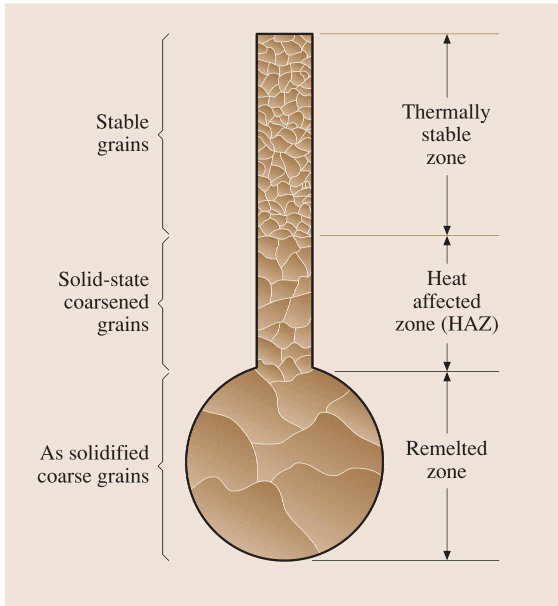

Fig. 55.5 Schematic illustration of the grain size in a Au wirebond. (After [55.11])

must have sufficient ductility to deform to the required wirebond shape but retain sufficient strength not to deform or move during the molding process (wire sweep). The Au alloy must be optimized for these opposing requirements. Au wire is typically stabilized with Cu and Ag dopants at levels below 100 ppm by weight. These dopants keep the grain size small to retain strength without deleteriously affecting ductility. As the Au wire decreases in width, the levels of dopants may need to be increased, reducing the Au to less than the current 99.9% level. Proposed dopants include Be and Cu. The critical region in the wirebond is above the ball and below the wire, known as the heat-affected zone (HAZ). A schematic of the zone is shown in Fig. 55.5. This zone forms above the ball that was melted and cools to form a very large as-solidified grain size. The HAZ forms a large grain size while coarsening in the solid state as the molten ball is created. [The ball is formed under a flame or high current, solidifies, and is then placed on a Au or Al pad and with the addition of energy (pressure/heat/vibration) forms a solid-state ball bond.] The strength in the HAZ is reduced by the Hall–Petch relationship that states that strength is inversely proportional to grain size. The HAZ would be susceptible to potentially high levels of strain during molding and would be the most likely failure location. In thinner wires, an increased grain size is even more critical and alloying elements are needed to stabilize the structure and retain sufficient strength without affecting the ductility required to form the wirebond.

55.4.2 Wirebonds for RF

At RF frequencies, wirebonds affect electrical performance. At sub-RF' frequencies, the wirebonds can be neglected as their resistance and inductance are in the noise with respect to performance. In RF applications, the wirebonds experience parasitic losses due to inductance with adjacent wirebonds, resulting in signal disturbance. RF-circuit designers typically add at least 1-nH inductance per wirebond but the effect can be variable and must by physically compensated by tuning the circuit. In effect, the wirebonds act as discrete inductors. The materials issues for RF wirebonds are the same as those described above for digital circuits but the effect of the wirebonds themselves is more significant in RF compared to digital and must be accounted for in the design of the device.

55.5 Solder Interconnects

For surface-mount and area array applications, the role of solder in the package is significant. In these advanced designs, the solder is an electrical interconnect, a mechanical bond and must often serve as a thermal conduit to remove heat from the joined device. The interconnects become more critical as chip size, chip carrier size, and the number of I/Os increase, while the solder joint size and cost decreases. Furthermore, some of the use environments are becoming increasingly severe. For example, some automotive electronics are being placed in locations under the hood with temperature extremes that could range from −55–180 °C. Portable devices, such as cellular telephones are expected to withstand severe shock environments caused by dropping a phone.

A solder interconnect consists of the solder alloy and the pads to which it is joined. The solder alloy is a low-temperature-melting metal that wets and reacts with metal pads or leads to form a metallurgical bond. During the wetting process the solder reacts with the

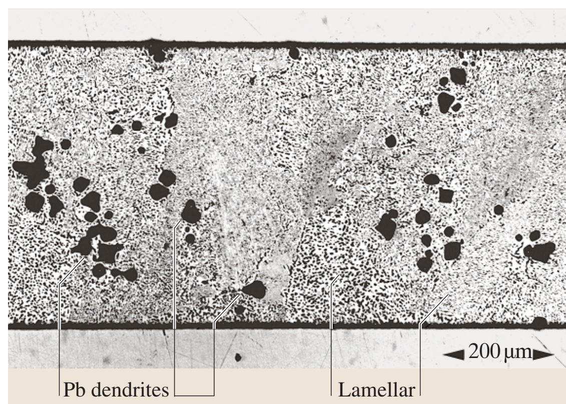

Fig. 55.6 Optical micrograph of the near-eutectic 63Sn–37Pb solder microstructure with the lamellar Sn- and Pb-rich phases and dendrites indicated

pad metallization, forming an intermetallic compound (IC) on the pad surface that continues to grow when the solder is in the solid state.

The most commonly used solder alloy for electronic interconnects is near-eutectic Sn–Pb with a composition of 63Sn–37Pb (by *wt%*). The microstructure of this alloy is shown in the optical micrograph in Fig. 55.6 and consists of Sn- and Pb-rich lamella. The lamella are oriented as cells after solidification with the slightly coarsened regions that separate the individual cells as the last part of the solder to solidify. This alloy melts at 183 °C. Pb-rich Sn–Pb alloys (such as 95Pb–5Sn or 97.5Pb–2.5Sn) are used for soldering temperature hierarchies as these alloys melt at temperatures in excess of 300 °C. The microstructure of Pb-rich alloys consists of a matrix of large Pb grains decorated with Sn precipitates. In flip-chip applications die are soldered to substrates with high-Pb solder. The substrates are soldered to a board with near-eutectic Sn–Pb. The Sn is the active components of these solder alloys and reacts with metallizations such as Cu or Ni to form intermetallic compounds.

Other solder alloys have found some use in electronic packaging, including Sn–Ag, Pb–In, Sn–Sb, etc. These alloys are used for a variety of applications including creating a soldering temperature hierarchy (higher or lower than Sn–Pb) or slowing the reaction rate with the metallization (e.g., In), or changing the mechanical properties of the joint. These alloys either form as a single-phase matrix with precipitates or as two-phase structures similar to eutectic Sn–Pb. The focus of this section, however, is on the most commonly used solder alloy, eutectic Sn–Pb.

The microstructure of the solder influences the mechanical behavior and reliability of the interconnects by governing the deformation and failure process. Typical deformation depends on the motion of dislocations and the growth and reconfiguration of grains and this is more sensitive to the structure of the solder than its chemistry. Therefore, depending upon processing conditions, the same solder alloy can respond differently to imposed stress and strain. Additionally, solders

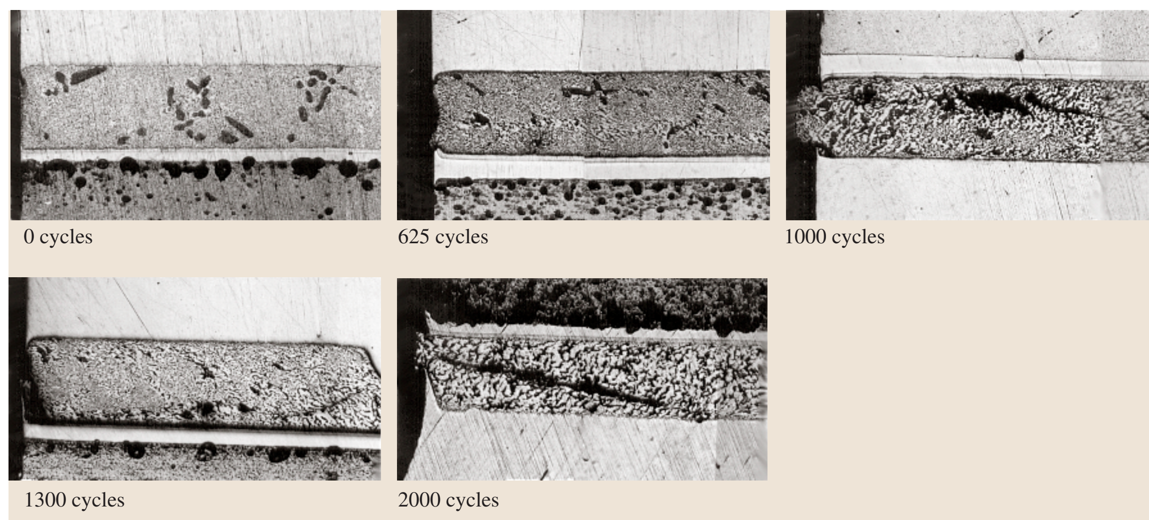

Fig. 55.7 Optical micrographs that show heterogeneous coarsening of the eutectic Sn–Pb microstructure at colony boundaries after thermomechanical fatigue

are low-melting-temperature materials that are used at a significant fraction of their melting point and are thermodynamically unstable. As the joint ages (at temperature and under strain) the microstructure changes and the mechanical properties and reliability change. The microstructure changes by grain (or phase) coarsening, which may be heterogeneous or homogeneous. Furthermore, the interfacial intermetallic grows in thickness and coarsens with time at temperature. All of this must be comprehended to determine the reliability of solder interconnects.

Thermomechanical fatigue occurs when materials with different CTEs are joined and used in an environment that experiences cyclic temperature fluctuations resulting in imposed cycling strain. Thermomechanical fatigue is a major deformation mechanism affecting solder interconnects in electronic packages. Even small temperature fluctuations can have a large effect, depending upon the joint thickness and CTE difference of the joined materials. The strain imposed on the solder joints follows the relation:

$$\Delta\gamma = \Delta\alpha \Delta T a / h ,$$

where $\Delta\gamma$ is the shear strain imposed, $\Delta\alpha$ is the difference in coefficient of expansion between the joined materials, ΔT is the temperature change, a is the distance from the neutral expansion point of the joined materials, and h is the thickness of the interconnect. After a critical number of thermal excursions, such as machine on/off cycles, solder joints experience fatigue failure. The type and magnitude of strains in solder joints under conditions of thermomechanical fatigue are often quite complex. For surface-mount applications, the strain is nominally shear. However, tensile and mixed-mode strains can occur due to bending of the chip carrier or board.

The combination of strain and temperature during thermomechanical fatigue has a large effect on the microstructure, and microstructural evolution of eutectic Sn–Pb solder joints. The microstructural evolution of 60Sn–40Pb solder as a function of the number of thermal cycles ($-55-125\,^{\circ}\mathrm{C}$) is shown in Fig. 55.7. The microstructure evolves through deformation that concentrates at the colony boundaries closely parallel to the direction of imposed shear strain, causing the cells to slide or rotate relative to one another. The structure within the cell boundaries becomes slightly coarsened relative to the remaining solder-joint microstructure and, thus are the weak links of the joint. Damage (in the form of defects or dislocations) is created at the cell boundaries at the low-temperature portion of a thermal cycle. As the temperature rises, the deformation is annealed by recrystallization or stress-assisted diffusion, where material diffuses to regions of high stress. This results in coarsening of the Sn-rich and Pb-rich grains and phases in colony boundaries. The heterogeneously coarsened colony boundaries are weaker than the rest of the joint and any further deformation concentrates in the coarsened regions, resulting in further coarsening. Failure eventually occurs due to cracks that form in the coarsened regions of a joint. The first indications of impending failure are associated with cracking of coarsened Sn-rich grains in the heterogeneous region whose initial as-solidified grain size is in the submicron range. When cracks initiate during thermomechanical fatigue, the Sn-grains have grown to $5-10\,\mu\mathrm{m}$. Failure occurs when grains can no longer slide and rotate to accommodate the imposed strain, resulting in intergranular separation.

Lead-rich Pb–Sn alloys undergo thermomechanical fatigue behavior but show little evidence of microstructural evolution. These solders undergo intergranular failure caused by void coalescence and growth at Pb grain boundaries. The strain imposed during thermomechanical fatigue cannot be accommodated by large Pb grains, resulting in intergranular failure. However, Pb loses the work-hardening effect quickly so that damage in the form of cracks does not propagate easily.

Other solder alloys, such as the Pb-free Sn–3.5Ag eutectic-based solders, experience thermomechanical fatigue damage and failure at Sn grain boundaries. The microstructural evolution in these alloys tends to be phase coarsening with minimal grain-size coarsening. Sn–Ag–X alloys tend to have longer thermomechanical fatigue lifetimes than near-eutectic Sn–Pb solders.

Intermetallic compounds form between pad metallization and the active components of the molten solder (typically Sn). For Cu metallization, the Sn reacts to form Cu_3Sn and Cu_6Sn_5 intermetallics. For Ni, the Sn reacts to form Ni_3Sn_4. After solidification, the intermetallic compounds continue to grow by solid-state diffusion. Over long periods of time, the intermetallic layers can grow to significant thicknesses ($> 20\,\mu\mathrm{m}$) and the solder–intermetallic interface may contain easy sites for crack initiation and propagation. Excessive growth also consumes the base metal, or finish, that can result in the loss of adhesion to the underlying metal that is not solder-wettable or create a plane of weakness owing to the stress generated from an intermetallic layer that is too thick. The metallized pad thickness must generally be greater than that consumed by the solder.

The transformation of solder-wettable coatings into intermetallics by solid-state reactions can also result in excessive intermetallic growth that degrades mechanical properties. The interfacial intermetallics are brittle and may fracture when strain is imposed, especially if the strain is tensile in nature. Solder-joint interfacial intermetallics are brittle because they typically have complex crystal structures with few crystallographic planes available to accommodate stress by strain relief, i. e., plastic deformation via a slip mechanism. The failures are characteristically brittle and occur through the intermetallic or at the intermetallic/solder interface under low-load conditions.

55.5.1 Flip-Chip Interconnects

Recent developments in under-bump metallurgy (UBM) and solder joints have resulted in lower cost and higher performance flip-chip interconnects. The UBM serves as an electrical, thermal, and mechanical interface between the silicon bond pads and the package substrate. The structure of the UBM is designed to adhere to the Al on the Si, act as a diffusion barrier between the solder and Si, and be a wettable surface to join to the solder. The most common UBM is the evaporated Cr/Cr–Cu/Cu/Au developed by IBM [55.12] for use with an evaporated high-Pb-content Pb–Sn alloy joined to a ceramic substrate. This UBM is expensive and new UBM systems with sputtered or plated metallizations have been developed. Plated metallizations are the lowest cost UBMs.

A significant change in flip-chip interconnects is the move toward a lower-melting-point solder alloy, such as eutectic 63Sn–37Pb ($wt\%$) that can be processed below 220 °C as opposed to 350 °C for high-Pb solder. New materials on the die (low-k dielectric) and substrate (organic materials) require this lower processing temperature. The change in solder alloy also requires a change in the UBM. Traditional UBM systems are based on a thin Cu layer that dissolves into high-Sn solders, resulting in spalling and dewetting. Eutectic-solder UBM systems utilize a layer of Ni for solder wetting. The Ni is wet by Sn–Pb solder but reacts much more slowly than Cu. The addition of $\approx 9\%$ V to Ni reduces the ferromagnetic behavior of the Ni and enables the use of sputtering of the Ni. Electroless plating of Ni–9%P is the lowest-cost UBM and has the advantage that plating occurs only where desired on the metal pads on the silicon. To plate onto Al, the pads are zincated, then immediately plated with Ni. One issue with Ni-based UBMs is the intermetallic layer between the solder and Ni (Ni_3Sn_4). Although very thin, this intermetallic layer can be brittle and the long-term reliability must be fully characterized and understood.

There are three solder deposition techniques available for flip chip. Traditionally, high-Pb solder is evaporated onto the UBM then reflowed to form metallurgical bonds. Evaporation is expensive because the masks must be regularly cleaned and there is excessive scrap solder. The composition of evaporated solder is difficult to control outside the high-Pb regime. Solder paste is a lower-cost alternative to evaporation and involves screening the paste onto the UBM then reflowing. Solder paste reduces waste, cleaning is inexpensive, and the paste comes in a variety of compositions, including eutectic Sn–Pb. The difficulty with paste arises in fine-pitch applications where the rheology of the paste makes it difficult to force into the required small holes in the screen. Solder may also be plated, which is inexpensive (no waste and easy cleaning) and has excellent fine-pitch coverage. Solder bumps at a pitch of 25 mm have been achieved by plating. The difficulty with plating is achieving ball and compositional uniformity.

The trend in flip-chip interconnect pitch is that the current 250-µm pitch will continue to shrink. The driving force for this pitch shrink is to satisfy the requirements for high-performance silicon devices. These requirements include a dramatic increase in the number of I/O due to increases in the number of signal lines and power requirements. Higher-power devices require more signal and ground lines and, to limit point sources of heat the power and ground interconnects should be spread evenly across the area array.

There are a number of materials and processing challenges associated with finer pitches. As the pitch shrinks, the methods to deposit the solder become more limited. Solder paste is very difficult to deposit using a silk-screen method at pitches below 150 µm due to rheological limitations of forcing a semi-solid (the paste) into small holes (the silk screen). Evaporation is difficult because developing a metal screen mask with the required tolerances is prohibitively expensive. Solder plating is still a good option but the solder must be very uniform across each die. Solder ball uniformity is critical because large variations between die could result in electrical opens, for small balls, and shorts, for large balls. At 250 µm, ball uniformity across a die is 10%, at 150 µm this decreases to 5% and the change in dimension tolerance is 12.5 µm down to 3.75 µm. An additional issue with a decrease in ball size is that the joint gap between the substrate and the die decreases to the point that it may

become very difficult to flow underfill completely under the die. At 100-µm pitch the gap between the die and substrate could be significantly less than 25 µm, below the limit of underfill flow. For these very-fine-pitch applications an alternative underfill technique will need to be developed because flow under the chip will not be possible. One alternative would be to deposit the underfill material on the wafer immediately after flip-chip solder bumping then underfill cure would simultaneously occur during solder relfow. New underfill materials and processes must be developed to implement this process.

55.5.2 Flip Chip for RF

Flip chip provides substantial improvements in off-circuit RF performance because the inductance is decreased as the ball height and shape is very consistent and predictable. Wirebond lengths can vary (typically ±100 µm), resulting in parasitic variations not observed in flip-chip interconnects. The number of I/O on an RF circuit is generally small so the pitch of the interconnects is generally quite large.

The die interconnects on GaAs are typically Au whereas on Si they are Al. A UBM is required for Si applications because solder does not wet Al. The solder would wet the Au of the GaAs but the Au layer is very thin and would dissolve the entire Au layer very quickly so a UBM is also required for GaAs. The UBMs available for Si can also be applied to GaAs but can be simpler because the adhesion of other metals to Au is easier to achieve than it is on Al.

The solder alloys for GaAs flip-chip bumps tend to be similar to that for Si but with a greater emphasis on Au-based alloys because of the desire to use a highly conductive material such as Au for very-high-speed applications. Eutectic Au–Sn, Ag and In alloys have been commonly used but the wetting of these solders is typically poor. For finer-pitch applications on GaAs (due to the small die size, not large numbers of I/O) other materials with good wetting are needed. Conductive adhesives have been explored for GaAs bumps. Work by *Lin* et al. [55.13] found no significant difference in electrical performance up to 2 GHz between a conductive adhesive and Au–Sn solder. The use of underfill for flip-chip packages can cause a major loss in RF energy because the high dielectric constant of the underfill polymer is greater than that of air. With a conductive adhesive localized to just the bond pads, not the entire surface of the die, this RF loss will not be observed.

55.5.3 Pb-Free

The electronics industry extensively uses Pb–Sn solder alloys in flip-chip applications as well as in many other interconnects in the electronic package. However, medical studies have shown that Pb is a heavy-metal toxin that can damage the kidneys, liver, blood, and central nervous system. Less than one percent per year of global Pb consumption is used in solder alloys for electronic products but electronics and electrical systems make up an increasingly larger fraction of landfills [55.14]. The issue of Pb leaching from landfills into the water table has raised alarm as a potential source of long-term contamination of soil and ground water. Concerns about the presence of Pb in the environment and potential exposure scenarios that could result in the ingestion of Pb by humans and wildlife have prompted a concerted effort to limit the use of Pb in manufactured products (notably gasoline, plumbing solders, and paint). International laws have recently been proposed to expand Pb control laws to limit or ban the use of Pb in manufactured electronics products. The most aggressive and well known effort is the European Union's Waste in Electrical and Electronic Equipment (WEEE) directive that proposes a ban on Pb in electronics by 2006. The Japanese Environmental Agency has proposed that Pb-containing scrap must be disposed of in sealed landfills to prevent Pb leaching. Electronics manufacturers have responded to these proposed bans in a variety of ways. Many companies have not taken a stance, hoping that legislation will not be enacted. Other companies have aggressively pursued solutions to the proposed bans and are using Pb-free products as a *green* marketing strategy. Extensive research on Pb-free solders has been published. A comprehensive review of the status of Pb-free solders, primarily focused on carrier-to-board (surface-mount and through-hole) interconnects, can be found in the literature [55.15–19]. A growing requirement is Pb-free solders for flip-chip interconnects.

One benefit of a Pb-free flip-chip interconnect is the reduction of Pb^{210}-created alpha-particle radiation. All mined Pb contains a small amount of radioactive Pb^{210} that decays and emits alpha particles. When an alpha particle enters an active element of the Si (such as a memory cell) it has sufficient energy to cause the stored charge to be released with the result of changing stored memory from a 1 to a 0 state. There is no permanent damage to the Si itself so this radiation-induced fault is termed a *soft error*. The alpha particles have a low energy that is dissipated over relatively short distances. However, due to their proximity to active

elements, the flip-chip solder interconnects have sufficient levels of alpha-particle radiation to induce soft errors in complementary metal–oxide–semiconductor (CMOS) technology, which become more critical as the cell size on the die is reduced [55.20, 21]. For Pb–Sn solders, one solution to alpha-particle radiation is to use elemental Pb that was mined many, many years ago where the majority of Pb^{210} has decayed. The source of this Pb is typically found as the ballast of shipping vessels that sank almost 2000 years ago and is relatively expensive. The elemental constituents of Pb-free solders (Sn, Cu, Ag, Bi, In, Sb), however, do not radioactively decompose so alpha-particle radiation is minimal.

Flip-chip interconnects are the electrical and mechanical connections between the semiconductor integrated circuit and the package [or board for direct chip attach (DCA)]. These interconnects are formed on the periphery or in an area array on the top surface of an active die. Flip-chip interconnects are formed by depositing solder onto a metallized Si wafer in the form of discrete balls, solder paste or by directly plating onto the pads on the wafer. The solder must wet and join to the pads on the Si devices so an under-bump metallurgy (UBM) is typically deposited on the Al or Cu pads on the Si. The UBM typically consists of a barrier metal (e.g., Ti or W) followed by a solder-wettable layer (e.g., Cu or Ni). The top layer of the Ni metallization is covered with a noble metal, such as Au, to prevent oxidation that would inhibit solder wetting. The UBM also acts as a diffusion barrier between the Si and the solder and must be thick enough to withstand interactions (intermetallic formation) between the solder and UBM. Flip-chip interconnects are smaller (on the order of 100 μm in diameter) than surface-mount joints and are projected to have pitches that will shrink below 150 μm. Flip-chip interconnects have a unique set of requirements. These joints must be able to withstand a potentially high level of strain mismatch between Si and an organic substrate. Flip-chip technology has moved from ceramic packaging with high-Pb solder (97.5Pb–2.5Sn) to an organic package that requires lower-temperature reflow ($< 260\,°C$). This can be accomplished by bumping the die with high-Pb solder then joining it to an organic board with eutectic Sn–Pb but this is a cost increase that is eliminated with a monolithic solder. The joints must withstand board-level reflow environments compatible with joining to organic substrates that, again, have a maximum reflow temperature of 260 °C. The Pb-free solder must meet these requirements and perform at, or above, the level of performance of the Sn–Pb solder it is intended to replace. The flip-chip solder alloy is typically deposited on Si wafers either as solder paste stencil-printed on the defined UBM pads or by direct plating on the UBMs. The simplicity and low cost of plating the solder for flip-chip interconnects makes electrochemical deposition the most attractive choice for flip-chip bumping.

55.6 Substrates

The move to organic substrates is the focus of extensive development effort worldwide by both printed circuit board manufacturers and traditional suppliers that requires significant amounts of capital. Cost savings are expected by replacing ceramic substrates with organic substrates. One stated reason for moving to an organic substrate is based on the belief that, in volume production, organic materials are less expensive than ceramics due to the nature of printed circuit board processing. The organic substrate also offers an increase in electrical performance due to its lower dielectric constant (therefore, less capacitance and better speed) of 3.5 for organic versus 5.0 for ceramics.

Advanced substrates for flip chip must also provide increased wireability while delivering improved electrical performance with reliability levels at least equivalent to current surface-mount applications. The board interconnect density for flip-chip substrates must accommodate the increasing density of off-chip interconnect, and cost-effective substrate capability that combines the necessary fine-line and micro-via features must be developed. Micro-vias are the metal-filled holes that provide a conduction path between copper lines in the multiple layers of an organic substrate. Micro-via capability must also scale with line width/spacing in order to provide the *via in line* structures which will be necessary to support bump pitch densification. At a pitch of 250 μm, micro-vias can be created using a photolithographic process. At finer pitch, laser drilling techniques are used to create the required small via size to support the smaller capture pads and facilitate the dense routing required for flip chip.

Materials with dielectric constants approaching 2.0 with coefficients of thermal expansion approach-

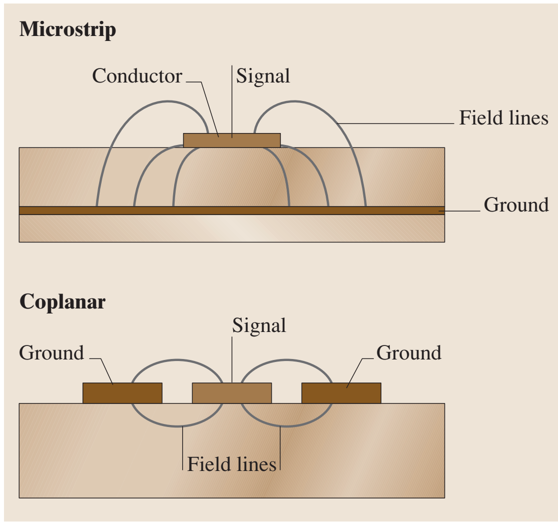

Fig. 55.8 Schematic illustration of RF electric-field lines in the microstrip and coplanar designs

ing 6.0 ppm/°C are necessary to meet fine pitch requirements. Furthermore, uniformity and flatness requirements must be improved on organic substrates to ensure uniform joint size and bonding across each die as the interconnect pitch decreases.

The change in substrate materials drives the need for a lower-melting-temperature solder to replace the high-Pb-content Sn–Pb alloys that are processed in excess of 300 °C for ceramic substrates. The organic materials in a substrate are typically epoxy-based and char or burn at temperatures in excess of 250 °C. The most common solder alloy candidate is near-eutectic Sn–Pb, which can be processed well below 250 °C ($T_{mp} = 183$ °C). However, this could result in a situation where the flip-chip interconnect melts every time a subsequent solder reflow occurs. Multiple reflows of the solder interconnects accelerates intermetallic growth between the tin of the solder and the metallized pads for the UBM and substrate. One way to circumvent this issue is to deposit low-melting-temperature eutectic Sn–Pb solder on the substrate lands, or on the high-melting-temperature solder bump. Reflow to the substrate can be performed at eutectic Sn–Pb soldering temperatures but the mixing between the high-Pb-content and eutectic solder results in a higher-melting-temperature composition. Subsequent reflows, at eutectic Sn–Pb processing temperatures, will not remelt the *composite-alloy* flip-chip joint. This addresses the low-temperature processing requirements for organic substrates but does not address the low-κ-dielectric low-temperature processing requirements because the high-Pb-content solder must still be reflowed on the silicon.

55.6.1 RF Substrate Materials

Optimum electrical performance is achieved in an RF module when the signal-carrying conductor is adjacent to the ground plane to contain the electric field. In microstrip designs the conductor is above the ground plane, in coplanar designs the conductor is sandwiched between ground plans, as shown schematically in Fig. 55.8. These designs affect the materials in the package. The impedance of the lines is desired to be 50 Ω (which matches the radiation impedance of the antenna to air). The impedance is affected by the conductor material, typically Au, and the dielectric material [Si, SiGe, GaAs, for the die and LTCC, Al_2O_3 or epoxy (organic) for the substrate].

Like its digital counterpart, RF packaging is moving away from the Al_2O_3 ceramic substrates used in RF applications to the lower-cost solution of LTCC and organic materials. The metallizations used are Cu on the interior of the substrates and Au as the top-layer metallization to improve RF performance.

Organic substrates offer a lower-cost solution. This substrate is built in a laminate structure with punched, or laser-drilled, holes that are subsequently plated for interlayer via interconnects. The laminant layers are variations of epoxy and glass optimized for low dielectric constants. LTCC substrates are also laminant structures of sheets of LTCC with laser-drilled and plated vias. Recently, LTCC materials have been optimized to not shrink in the x–y plane during the sintering process (z-direction shrinkage, however, is significant). The LTCC laminants are extremely thin, compared to organic, and offer the opportunity to build complex RF substrates.

An additional trend in RF substrate technology is to move the discrete functions of RF module circuits form surface-mounted components to embedding them in the substrate. These embedded functions are typically capacitors and inductors and occasionally resistors. This can be done because the substrate material is dielectric and metal, which are the basic components of passive devices. The advantages of embedding components are reduced size, reduced cost and improved performance. Size can be reduced because surface-mount components take up a great deal of the surface of the substrate. By embedding these components, they are thinner and the area is reduced. Cost is reduced because the embedded

passives are formed as part of the laminant layers by patterning the metal/dielectric and is essentially cost-free because the patterning would be done regardless. Performance can be increased through the smaller size of the module. The embedding of components in substrates does offer the opportunity for improved materials. Performance could be improved by finding means to alter the materials properties of regions of the laminant layers to optimize the electrical performance of discrete components that are to be embedded (i. e., *seed* regions of the substrate for optimal capacitance, inductance and resistance).

55.7 Underfill and Encapsulants

55.7.1 Underfill

Flip-chip technology demands that the space between the chip and the substrate be filled with a dielectric organic material to help mechanically interlock the chip to the substrate. Most underfill materials available are silica-filled anhydride resin polymers. The filler provides the strength in the composite polymer and the resin bonds with the die and substrate. Without the underfill the difference in coefficient of thermal expansion between the chip (3 ppm/°C) and the substrate (≈ 17 ppm/°C) would quickly result in fracture of the solder interconnects when variations in temperature occurred. New underfills must be developed to accommodate increased bump density and shrinking of bump height. As bump density increases and pitch decreases, the underfill must flow into smaller spaces. A 250-μm pitch requires an underfill with a thickness of 110 μm. At a 150-μm pitch, the dimension between the chip and substrate will be less than 50 μm but 100% fill of underfill is still required. Traditional flow dispensing and curing may not be suitable in these thin spaces due to a lack of capillary driving force (current underfill materials flow through a minimum thickness of 75 μm). For very thin fill spaces, wafer-level deposition of the underfill needs to be developed. This wafer-level deposition involves spinning on of an uncured polymer to a uniform thickness slightly less than the bump height. The wafer would then be diced and die-mounted on substrates. Reflow would form the solder joints and cure the underfill, simultaneously. The filled polymer must be spun to a uniform thickness of 25 μm or less, and bond well with silicon and substrate materials, and also be compliant.

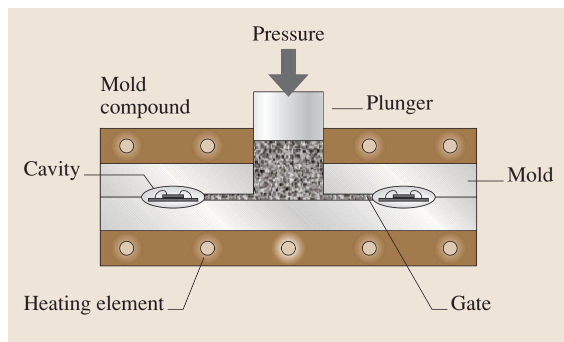

Fig. 55.9 Schematic illustration of the transfer mold process

55.7.2 Encapsulation

Encapsulation of electronic packages is required to protect the electronic components from environmental degradation such as moisture contamination, mechanical damage and must also provide electrical isolation. The encapsulation material is a polymer that flows over and covers the electronic components, and then cures into a solid. For electronic packaging, the most common method for applying the encapsulation is transfer molding. Figure 55.9 is a schematic illustration of the transfer mold process. The transfer mold compound material is typically a thermoset cross-linking polymer. The polymer resin portion forms 25–35% of the total mold compound (by weight) and consists of epoxy resin, a hardener and a curing agent. The mold compound material is filled with powders of silica (SiO_2), alumina (Al_2O_3) or glass (65–75% of the total weight) to reduce the thermal expansion coefficient of the polymer and add strength. Amorphous silica is used for minimum thermal expansion coefficient but this results in a decrease in thermal conductivity. Crystalline silica improves thermal conductivity but is abrasive to the molds themselves. Small amounts of pigments (to color the mold compound), accelerants, flame retardants, mold-release agents, getterers, and antioxidants are also added to the final mold compound. Pellets of the mold compound are placed into a heated cavity at the top of the mold and pressure is applied by a ram that pushes the liquefying materials into the mold. The material

is forced through channels and through a constriction (called the gate) that provides back-pressure and regulates the flow rate of the molten mold compound. After passing through the gate, the mold material flows across the component being encapsulated. The heat is turned off and upon cooling the polymer cross-links, with the use of a curing agent (typically an amine) that is included in the mold compound. The mold compound material has good adhesion, good stability with regards to temperature, chemicals, and the environment. It also cures rapidly, has low permeability to moisture and high dielectric strength.

The transfer mold process has the advantage that part dimensions are very well controlled. The process and materials are low cost and high-volume manufacturing is possible.

An issue with the mold compound encapsulation processing is wire sweep, where the force of the viscous encapsulant can push bond wires to short with one another. This has been addressed with optimized filler size and shape and mold temperature and pressure. After molding, the difference in thermal expansion between the cured mold compound and the rest of the package (the substrate, leadframe, semiconductor device, etc.) can result in considerable stresses at the interfaces. Furthermore, the CTE of mold compounds changes when the material goes above the glass-transition temperature, T_g. T_g is the temperature at which the polymer changes from a rigid structure to a softer, more glass-like structure. Below T_g, the CTE of typical mold compounds is 20×10^{-6} /°C but above T_g this can increase to $60{-}70\times10^{-6}$ /°C. The T_g of mold compounds varies but is usually 175–200 °C below the solder processing temperatures, which are typically in excess of 220 °C. After cooling from mold processing, the mold compound forms a compression seal with the materials that expand less (leadframe, substrate, semiconductor). However, upon heating to solder process temperatures, the stress is reversed to tensile and can result in interfacial cracking, or delamination. The interfacial cracks provide a conduit for the ingress of water or ionic contaminants that could result in corrosion of metals in the package (particularly Al bond pads). This issue must be addressed by optimizing the mold compound to the package application (materials and size) to minimize strain and to maximize interlocking mechanisms between the mold compound and the substrate/leadframe.

Mold compound encapsulation is generally detrimental to RF device performance. The encapsulant materials are nonuniform and degrade performance because the electric field generated by the RF circuit in the encapsulant is nonuniform, resulting in lossy behavior. Many high-performance RF packages are designed with a cavity and are made out of ceramic with a metal lid to form the cavity. However, plastic encapsulation is required to achieve the required low-cost reliability of the package, so a trade-off must be made for performance, reliability and cost.

55.8 Electrically Conductive Adhesives (ECAs)

Electrically conductive adhesives (ECAs) are composite materials consisting of a dielectric curable polymer and metallic conductive particles. ECAs are low-process-temperature alternatives to solder alloys. The polymer is an adhesive material that reacts chemically with metals to form a bond. The metallic particles in the adhesive form a network in the cured joint that forms a conduction path in area-array applications.

55.8.1 Adhesive Polymers

The polymer portion of the adhesive is available in two forms: thermoplastic and thermosetting. A schematic illustration of these two types of polymers is shown in Fig. 55.10. A thermoplastic polymer is a linear chain of linked monomers (nominally, hydrogen–carbon bonds). After curing, thermoplastic polymers becomes more rigid, but remain flexible. As the temperature is increased, these polymers essentially become molten. This provides a method to repair or replace components with thermoplastic joint area-array joints. Thermosetting materials are similar to thermoplastics, except that monomer chains become cross-linked in three dimensions during the curing stage. The number of cross-links determines the rigidity and the glass-transition temperature (T_g) of a thermoset polymer. In general, the more cross-links, the higher the T_g. A curing agent (e.g., a hardener) can be added to thermoplastic polymers to cause the cross-linking reaction in these materials as well. Curing can be performed using UV light, heat, or catalysts. Thermosetting materials are harder than thermoplastics, but can be processed and cured below their T_g and do not become molten above the T_g. However, the curing operation is not reversible, mak-

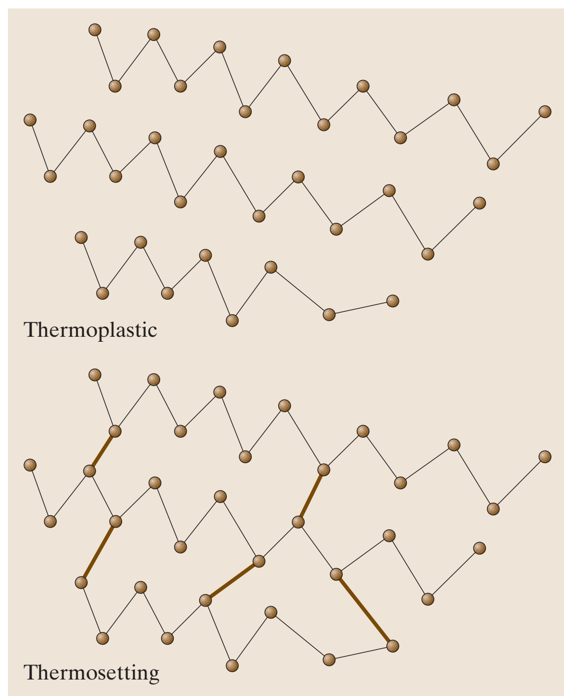

Fig. 55.10 Schematic illustration of polymer bonds for thermoplastic (linear bonds) and thermosetting (cross-linked bonds) electrically conductive adhesives

ing repair difficult. Examples of thermosetting materials include epoxies and acrylics. ECAs are typically made using either thermosetting or thermoplastic polymers, or a combination of the two.

55.8.2 Metal Fillers

A number of metals have been used to provide the electrical conductivity of ECAs. The metals are typically in the form of flakes, plates, rods, fibers, or spheres. The size of the metal particles is 5–20 μm. For the ECA to have suitable strength and electrical conduction requires a trade-off in metal filler content. The higher the metal content, the better the electrical conduction, but the poorer the strength of the adhesive. The metal content depends upon whether the adhesive is an isotropic or anisotropic conductor (described below), but does not usually exceed 40% by volume.

The metals most often used in ECAs are silver, gold, nickel, copper or variations of these (such as gold on nickel, silver on glass, or nickel on polymers). Silver-filled ECAs are the most common, because the cost of the metal is moderate and it has good electrical conductivity and low reactivity with oxygen. Gold has better physical properties than silver but the cost is prohibitive for most applications. Nickel is less expensive, but also has lower conductivity than either Au or Ag and has been found to corrode when aged in a humid environment, resulting in poor adhesion between the nickel and the epoxy matrix. Copper fillers oxidize rapidly and also delaminate from the polymer matrix.

55.8.3 Conduction Mechanisms

The mechanism of conduction in ECAs is hypothesized to occur via percolation, where current travels through a three-dimensional matrix of contacting particles. There must be a sufficient quantity of particles present in the adhesive to provide a suitable conduction path. The bulk resistivity of 60Sn–40Pb solder is 15×10^{-6} Ω cm, while that of ECAs is 7×10^{-5} to 5×10^{-4} Ω cm [55.22]. Therefore, the conduction of solder is 5–33 times better than ECAs. This difference in conductivity is due to the fact that only a portion of the joint cross section is available to provide the percolation path in ECAs whereas the entire cross section of solder joints conducts electricity. The loss of electrical conductivity does not severely affect second-level interconnects but could be an issue for first-level interconnects where good conductivity and switching speed may be required. For the current to pass from one metal particle to another, it must pass through, at a minimum, the oxide that forms on the metals or, at worst, some distance through the polymer matrix. It has been proposed that contact resistance is overcome by tunneling or bulk conduction through the semiconducting metal-oxide layer. However, measured electrical conduction has been determined to be better than any of the mechanisms described above [55.23]. It is possible that, in silver-loaded ECAs, silver diffuses out of the particles into microcracks in the polymer matrix, thereby creating additional conduction paths. To date, the details of the conduction mechanisms remain unresolved.

55.8.4 Isotropic Versus Anisotropic Conduction

ECAs are available in two types of conductors, isotropic and anisotropic. In isotropic adhesives, the conduction path is uniform in all directions with a filler-metal content sufficiently high to create a percolation path for the conductor. Anisotropic ECAs (or AECAs, also called z-axis conductors) only have one direction of conduction, useful for fine-pitched applications. In general,

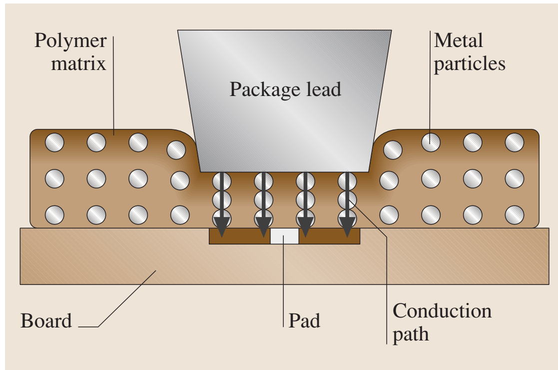

Fig. 55.11 Schematic illustration of an anisotropic electrically conductive adhesive. The adhesive is compressed, causing the conductive particles to contact one another in the z-axis and form an electrical path between the terminal pads. Outside the pad region, the metal particles are separated by the polymer and the AECA acts as a dielectric

anisotropic ECAs are prepared by dispensing metal particles into the polymer matrix at a level far below the percolation threshold. Pressure is imposed on the contact so that the particles come into contact with one another in one direction (parallel to the direction of imposed pressure). In the areas where no pressure is imposed, there is no conduction path and the adhesive is electrically insulated. This is illustrated in Fig. 55.11. In area-array applications anisotropic ECAs can be applied to the board but conduction will only take place between package and mating board pads due to the compression resulting from the cured adhesive, causing particle-to-particle contact between mating pads. No metal particle contact is made beyond the terminal pads, thus the adhesive is an insulator in those areas.

The terminal pad surface to which ECA or AECAs are to be joined must be oxide-free for the adhesive to form a cohesive joint. Bare copper typically provides very poor adhesion [55.24] because adhesives do not wet or react well with metal oxides, and in this way adhesives are similar to solder alloys. To overcome this problem, copper can be plated with nickel ($\approx 0.5\,\mu$m) and a thin layer of gold ($\approx 500\,$Å). Gold is an excellent bonding surface because it is virtually free of surface oxide and provides a diffusion barrier for nickel. Unlike solders, ECAs do not allow the luxury of using flux to remove oxides during processing so oxide-removal surface treatments must precede dispensing the adhesive. The stability of ECA joints is directly related to the quality of the bond interface with terminal-pad metallizations. In general, the less surface oxide present, the better the electrical stability. If surface oxide is present, there can be de-adhesion at the interface, which results in a reduced ability to carry electrical signals. The bonding of ECAs to other polymers, such as printed wiring board surfaces (FR-4 or polyimide) is excellent. Area-array component requirements are more stringent in the case of ECA joints compared to solder bumps. Solders only wet metal surfaces, so special processing steps are not needed to define solder-joint locations. For ECAs, the method of depositing the ECA must be precise (or an anisotropic ECA used) so that electrical shorts do not occur and this is exacerbated in area-array fine-pitch applications. Also the interconnects cannot easily be inspected because they are hidden beneath the joined component.

55.8.5 Rework

The ability to perform rework on conductive adhesive interconnects may limit the use of these materials for many applications. Thermoplastic adhesives can be reworked by heating and melting the joint, allowing components to be separated from the assembly. Thermosetting bonds are not reversible but can be softened by heating well above T_g and then removed. Some acrylic adhesives can be cleaved at room temperature and physically removed, although the brittle nature of the acrylics that allows for removal may also represent too great a joint reliability risk.

55.9 Thermal Issues

55.9.1 Thermal Issues in Digital Packaging

Increasing circuit and component density creates thermal complications that must be resolved by the packaging solution. Excessive temperatures in the devices result in degraded circuit performance or reliability issues. The thermal performance can be improved by using packaging materials with high thermal conductivity.

The operating temperature of Si directly impacts on switching speed and timing. In the operating temperature

range of 50–100 °C, a 5 °C drop in operating temperature results in a 1% increase in CMOS switching speed. From a reliability perspective, each 10 °C increase in operating temperature results in a twofold increase in the die failure rate. Therefore, packaging materials and processes that improve thermal performance are very important.

New materials is the area where the most significant improvements in thermal performance is possible. Improved thermal interface materials (greases, adhesives, tapes, phase-change materials) will improve heat flow out of the package. Improved adhesives and compliant sheets inside the package will improve heat dissipation from the die and can better accommodate CTE mismatch strains within the package.

Composite materials for package lids, heat spreaders and heat sinks are needed. Currently, these components face a dilemma of conflicting materials properties as good materials with good thermal conduction (e.g., Al) have very high CTE (e.g., $Al = 25 \times 10^{-6}$ /°C), which can result in poor reliability. Furthermore, most low-cost thermal conductors are also electrical conductors, which makes their use in dielectric packages problematic. The development of composite materials with anisotropic conductivities can provide excellent thermal conduction with matched CTE and the potential for good electrical isolation. At the die level, the use of low-cost thin-film diamond must increase. Diamond has excellent thermal conductivity and isolation but is currently too expensive for extensive use in microelectronic packaging.

55.9.2 Thermal Issues in RF Packaging

RF die can generate a great deal of heat when operating at high frequencies. This is particularly an issue with GaAs die because it has poor thermal conductivity (30 W/mK). The generated heat must be dissipated through the package. The preferred method to remove heat from wirebonded GaAs die is to thin the GaAs wafer by back-grinding to 100–125 μm. The thinner the die, the easier it is to transmit heat through the GaAs. Through-die vias are also used to help dissipate heat. The vias are formed by laser-drilling holes through the GaAs then plating the side walls with Au then thinning the wafer. Thinning the wafer not only benefits heat dissipation but also reduces the distance from the conducting layer on the surface of the die to the ground plane on the die backside, which improves impedance match in microstrip designs.

The problems with through-die vias and wafer thinning are cost and die breakage. Laser-drilling and thinning process increase the cost of the die. Furthermore, GaAs is a very brittle material and the presence of vias and thinning exacerbates the potential for cracking.

One method to reduce the thermal and mechanical problems associated with thermal issues on GaAs is to use flip-chip interconnects. For flip chip, the bumps act as electrical, mechanical and thermal interconnects. The bumps are on the front side of the die so ful- thickness die can be used. The challenge with flip chip as a thermal conductor is to put sufficient numbers of bumps on the die to dissipate the heat.

55.10 Summary

Materials are one of the most important aspects of microelectronic packaging. There is a need for new materials to be developed to meet the ever-changing requirements of high-speed digital and RF applications. Considerable resources are required to develop and characterize these materials. These materials must also be tested to determine their compatibility with assembly processesand device performance and to meet industry standards. The fundamental materials characteristics that must be understood, depending upon the material, include: the dielectric constant, dielectric loss, conductivity, resistivity, moisture absorption, glass-transition temperature, strength, time-dependent deformation (creep), and fracture toughness.

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