22. Silicon–Germanium: Properties, Growth and Applications

Silicon–germanium is an important material that is used for the fabrication of SiGe heterojunction bipolar transistors and strained Si metal–oxide–semiconductor (MOS) transistors for advanced complementary metal–oxide–semiconductor (CMOS) and BiCMOS (bipolar CMOS) technologies. It also has interesting optical properties that are increasingly being applied in silicon-based photonic devices. The key benefit of silicon–germanium is its use in combination with silicon to produce a heterojunction. Strain is incorporated into the silicon–germanium or the silicon during growth, which also gives improved physical properties such as higher values of mobility. This chapter reviews the properties of silicon–germanium, beginning with the electronic properties and then progressing to the optical properties. The growth of silicon–germanium is considered, with particular emphasis on the chemical vapour deposition technique and selective epitaxy. Finally, the properties of polycrystalline silicon–germanium are discussed in the context of its use as a gate material for MOS transistors.

Silicon–germanium ($Si_{1-x}Ge_x$) alloys have been researched since the late 1950s [22.1], but it is only in the past 15 years or so that these layers have been applied to new types of transistor technology. $Si_{1-x}Ge_x$ was first applied in bipolar technologies [22.2, 3], but more recently has been applied to metal–oxide–semiconductor (MOS) technologies [22.4–7]. This has been made possible by the development of new growth techniques, such as molecular-beam epitaxy (MBE), low-pressure chemical vapour deposition (LPCVD) and ultra-high-vacuum chemical vapour deposition (UHV-CVD). The key feature of these techniques that has led to the development of $Si_{1-x}Ge_x$ transistors is the growth of epitaxial layers at low temperatures (500–700 °C). This allows $Si_{1-x}Ge_x$ layers to be grown without disturbing the doping profiles of structures already present in the silicon wafer. $Si_{1-x}Ge_x$ layers can be successfully grown on silicon substrates even though there is a lattice mismatch between silicon and germanium of 4.2%.

The primary property of $Si_{1-x}Ge_x$ that is of interest for bipolar transistors is the band gap, which is smaller than that of silicon and controllable by varying the germanium content. Band-gap engineering concepts, which were previously only possible in compound semiconductor technologies, have now become viable in silicon technology. These concepts have introduced new degrees of freedom in the design of bipolar transistors that have led to dramatic improvements in transistor

performance. In $Si_{1-x}Ge_x$ heterojunction bipolar transistors (HBTs), the $Si_{1-x}Ge_x$ layer is incorporated into the base and the lower band gap of $Si_{1-x}Ge_x$ than Si is used to advantage to dramatically improve the high-frequency performance. $Si_{1-x}Ge_x$ HBTs have been produced with values of cut-off frequency, f_T, approaching 300 GHz [22.8], a value unimaginable in silicon bipolar transistors. Values of gate delay well below 10 ps can be achieved in properly optimised $Si_{1-x}Ge_x$ HBTs [22.9]. In $Si_{1-x}Ge_x$ MOS field-effect transistors (MOSFETs), the $Si_{1-x}Ge_x$ layer is incorporated in the channel and is used to give improved values of mobility. Initially, strained $Si_{1-x}Ge_x$ layers on silicon substrates were used to give improved hole mobility in p-channel transistors [22.7], but more recently thin, strained silicon layers on relaxed SiGe virtual substrates have been used to give improvements in both electron and hole mobility [22.4–6].

In this chapter, the properties of single-crystal silicon–germanium will first be outlined, followed by a description of the methods used for growing silicon–germanium layers. The properties and applications of polycrystalline silicon–germanium are also discussed later in the article.

22.1 Physical Properties of Silicon–Germanium

Silicon and germanium are completely miscible over the full range of compositions and hence can be combined to form $Si_{1-x}Ge_x$ alloys with the germanium content, x, ranging from 0 to 1 (0–100%). $Si_{1-x}Ge_x$ has a diamond-like lattice structure and the lattice constant is given by Vegard's rule:

$$a_{Si_{1-x}Ge_x} = a_{Si} + x\left(a_{Ge} - a_{Si}\right) , \qquad (22.1)$$

where x is the germanium fraction and a is the lattice constant. The lattice constant of silicon, a_{Si}, is 0.543 nm, the lattice constant of germanium, a_{Ge}, is 0.566 nm and the lattice mismatch is 4.2%.

When a $Si_{1-x}Ge_x$ layer is grown on a silicon substrate, the lattice mismatch at the interface between the $Si_{1-x}Ge_x$ and the silicon has to be accommodated. This can either be done by compression of the $Si_{1-x}Ge_x$ layer so that it fits to the silicon lattice or by the creation of misfit dislocations at the interface. These two possibilities are illustrated schematically in Fig. 22.1. In the former case, the $Si_{1-x}Ge_x$ layer adopts the silicon lattice spacing in the plane of the growth and hence the normally cubic $Si_{1-x}Ge_x$ crystal is distorted. When $Si_{1-x}Ge_x$ growth occurs in this way, the $Si_{1-x}Ge_x$ layer is under compressive strain and the layer is described as *pseudomorphic*. In the second case, the $Si_{1-x}Ge_x$ layer is unstrained, or relaxed, and the lattice mismatch at the interface is accommodated by the formation of misfit dislocations. These misfit dislocations generally lie in the plane of the interface, as shown in Fig. 22.1, but dislocations can also thread vertically through the $Si_{1-x}Ge_x$ layer.

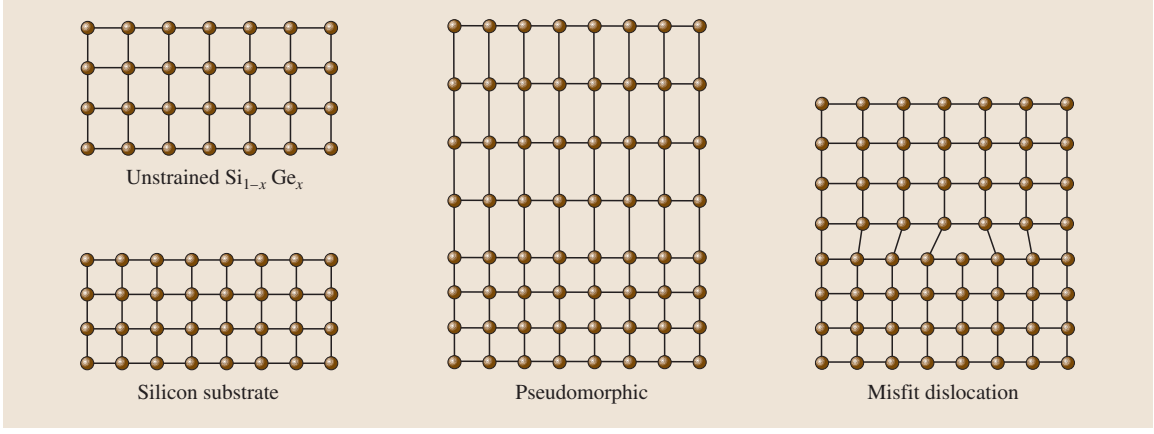


Fig. 22.1 Schematic illustration of pseudomorphic $Si_{1-x}Ge_x$ growth and misfit-dislocation formation

22.1.1 Critical Thickness

There is a maximum thickness of $Si_{1-x}Ge_x$ that can be grown before relaxation of the strain occurs through the formation of misfit dislocations. This is known as the critical thickness of the $Si_{1-x}Ge_x$ layer, and depends strongly on the germanium content, as shown in Fig. 22.2. The original calculations of critical layer thickness were made by *Matthews* and *Blakeslee* [22.11, 12] on the basis of the mechanical equilibrium of an existing threading dislocation. However, measurements of dislocation densities in $Si_{1-x}Ge_x$ showed, in many cases, no evidence of misfit dislocations for $Si_{1-x}Ge_x$ layers considerably thicker than the Matthews–Blakeslee limit. These results were explained by *People* and *Bean* [22.13] who calculated the critical thickness on the assumption that misfit-dislocation generation was determined solely by energy balance. The discrepancy between these two types of calculation can be explained by the observation that strain relaxation in $Si_{1-x}Ge_x$ layers occurs gradually. Layers above the People–Bean curve can be considered to be completely relaxed, whereas layers below the Matthews–Blakeslee curve can be considered to be fully strained. These fully strained layers are termed *stable* and will not relax during any subsequent high temperature processing. Layers lying between the two curves are termed *metastable*; these layers may be free of dislocations after growth, but are susceptible to relaxation during later high-temperature processing.

In practice, a number of additional factors influence the critical thickness of a $Si_{1-x}Ge_x$ layer. Of particular importance to both $Si_{1-x}Ge_x$ HBTs and $Si_{1-x}Ge_x$ MOSFETs, is the effect of a silicon cap layer, which has been shown to increase the critical thickness of the underlying $Si_{1-x}Ge_x$ layer. Figure 22.3 shows a comparison of the calculated critical thickness as a function of germanium percentage for stable $Si_{1-x}Ge_x$ layers with and without a silicon cap. It can be seen that the critical thickness is more than doubled by the presence of the silicon cap.

The presence of misfit dislocations in devices is highly undesirable, since they create generation/recombination centres, which degrade leakage currents when they are present in the depletion regions of devices. Threading dislocations also highly undesirable, as they can lead to the formation of emitter/collector pipes in $Si_{1-x}Ge_x$ HBTs. When designing $Si_{1-x}Ge_x$ devices, it is important that the $Si_{1-x}Ge_x$ thickness is chosen to give a stable layer, so that dislocation formation is avoided. A base thickness below the silicon cap curve in Fig. 22.3 will ensure a stable layer, which will withstand ion implantation and high-temperature annealing without encountering problems of relaxation and misfit-dislocation generation.

Considerable research has been done on the oxidation of $Si_{1-x}Ge_x$ [22.14, 15], and it has been found that the germanium in the $Si_{1-x}Ge_x$ layer does not oxidise, but piles up at the oxide/$Si_{1-x}Ge_x$ interface. This pile-up of germanium makes it difficult to achieve low values of interface state density in oxidised $Si_{1-x}Ge_x$ layers. It is therefore advisable to avoid direct oxidation of $Si_{1-x}Ge_x$ layers, particularly in $Si_{1-x}Ge_x$ MOS technologies. In $Si_{1-x}Ge_x$ MOSFETs, a silicon cap is often

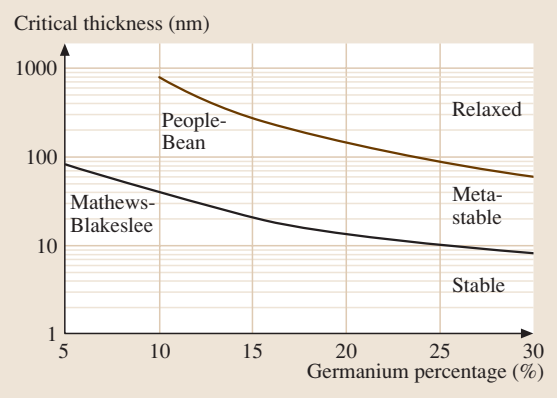


Fig. 22.2 Critical $Si_{1-x}Ge_x$ thickness as a function of germanium percentage (after *Iyer* et al. [22.2], copyright 1989 IEEE)

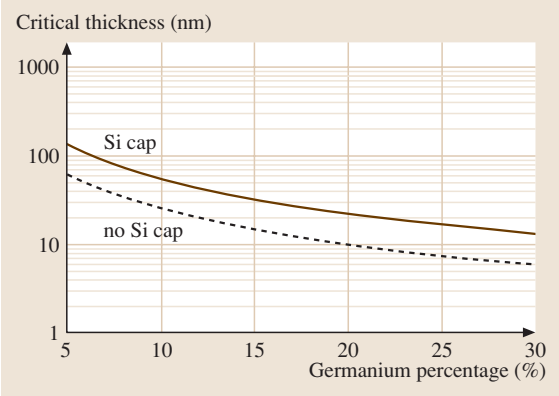


Fig. 22.3 Critical thickness as a function of germanium percentage for stable $Si_{1-x}Ge_x$ layers with and without a silicon cap (after *Jain* et al. [22.10], copyright 1992 Elsevier)

included above the $Si_{1-x}Ge_x$ layer that can be oxidised to create the gate oxide.

22.1.2 Band Structure

$Si_{1-x}Ge_x$ alloys have a smaller band gap than silicon partly because of the larger lattice constant and partly because of the strain. Figure 22.4 shows the variation of band gap with germanium percentage for strained and unstrained $Si_{1-x}Ge_x$. It can be seen that the strain has a dramatic effect on the band gap of $Si_{1-x}Ge_x$. For 10% germanium, the reduction in band gap compared with silicon is 92 meV for strained $Si_{1-x}Ge_x$, compared with 50 meV for unstrained $Si_{1-x}Ge_x$. The variation of band gap with germanium content for strained $Si_{1-x}Ge_x$ can be described by the following empirical equation:

$$E_G(x) = 1.17 + 0.96x - 0.43x^2 + 0.17x^3 \qquad (22.2)$$

The band alignment for compressively strained $Si_{1-x}Ge_x$ on unstrained silicon is illustrated schematically in Fig. 22.5. This band alignment is referred to as *type I*, and the majority of the band offset at the heterojunction interface occurs in the valence band, with only a small offset in the conduction band. Different band alignments can be obtained by engineering the strain in the substrate and the grown layer in different ways. For example, *type II* band alignments can be obtained by growing tensile-strained silicon on top of unstrained $Si_{1-x}Ge_x$. This arrangement gives large conduction- and valence-band offsets and is used in strained silicon MOSFETs.

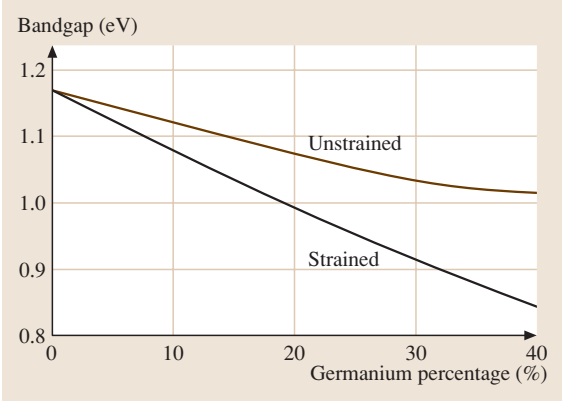


Fig. 22.4 Band gap as a function of germanium percentage for strained [22.16] and unstrained [22.1] $Si_{1-x}Ge_x$ (after *Iyer* et al. [22.2], copyright 1989 IEEE)

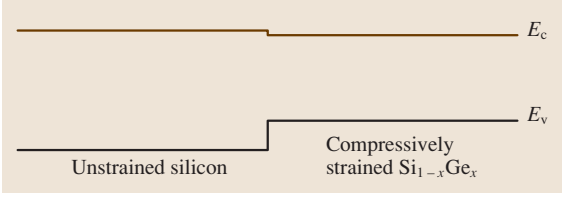


Fig. 22.5 Schematic illustration of the band alignment obtained for a compressively strained $Si_{1-x}Ge_x$ layer grown on an unstrained silicon substrate

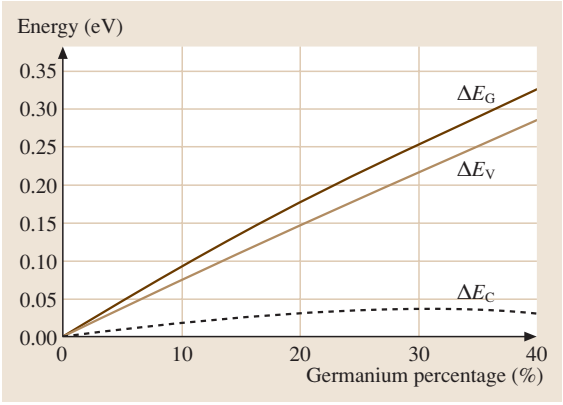


Fig. 22.6 Valence- and conduction-band offsets as a function of germanium percentage for strained $Si_{1-x}Ge_x$ grown on unstrained silicon (after *Poortmans* et al. [22.17], copyright 1993 Elsevier)

Figure 22.6 shows the variation of valence-band offset, ΔE_V, conduction-band offset, ΔE_C, and band-gap narrowing, ΔE_G, with germanium content. It can be seen that the majority of the band offset occurs in the valence band. For example for 10% germanium, the valence-band offset is 0.073 eV, compared with 0.019 eV for the conduction-band offset. The conduction-band offset can therefore be neglected for most practical purposes.

22.1.3 Dielectric Constant

The dielectric constant of $Si_{1-x}Ge_x$ can be obtained by linear interpolation between the known values for silicon and germanium [22.17] using the following equation:

$$\varepsilon(x) = 11.9(1 + 0.35x) \qquad (22.3)$$

22.1.4 Density of States

While, the density of states in the conduction band in $Si_{1-x}Ge_x$ is generally assumed to be the same as that in silicon, there is some evidence in the literature to suggest that the density of states in the valence band

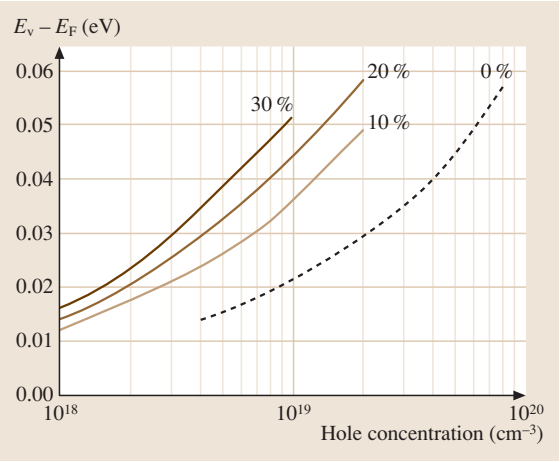


Fig. 22.7 Fermi-level position as a function of hole concentration for $Si_{1-x}Ge_x$ with four different germanium concentrations (after *Iyer* et al. [22.2], copyright 1989 IEEE)

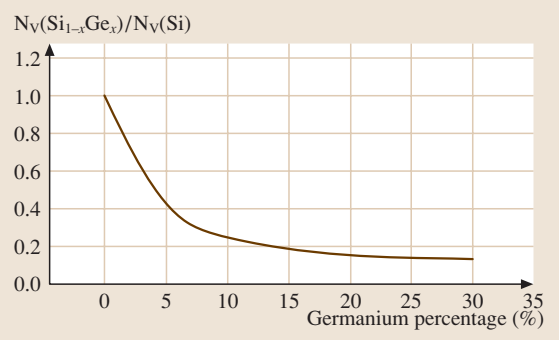


Fig. 22.8 Ratio of density of states in the valence band for $Si_{1-x}Ge_x$ to that for Si as a function of germanium percentage (after *Poortmans* [22.20], copyright 1993 University of Leuven)

is considerably smaller. *Manku* and *Nathan* [22.18, 19] have calculated the *E–k* diagram for strained $Si_{1-x}Ge_x$ and shown that the density-of-states hole mass is significantly lower, by a factor of approximately three at 30% germanium. There is some experimental evidence to support this calculation. For example, freeze-out of holes in p-type $Si_{1-x}Ge_x$ has been reported to occur at higher temperatures than in p-type silicon [22.20] and enhancements in the majority-carrier, hole mobility have been reported for p-type $Si_{1-x}Ge_x$ [22.21].

Using the calculated values of hole density of states of *Manku* and *Nathan* [22.18, 19], the hole concentration can be calculated as a function of Fermi-level position. These results are shown in Fig. 22.7 for $Si_{1-x}Ge_x$ with four different germanium contents. It can be seen that the Fermi level moves deeper into the valence band as the germanium concentration increases. Figure 22.8 shows the ratio of the calculated density of states in the valence

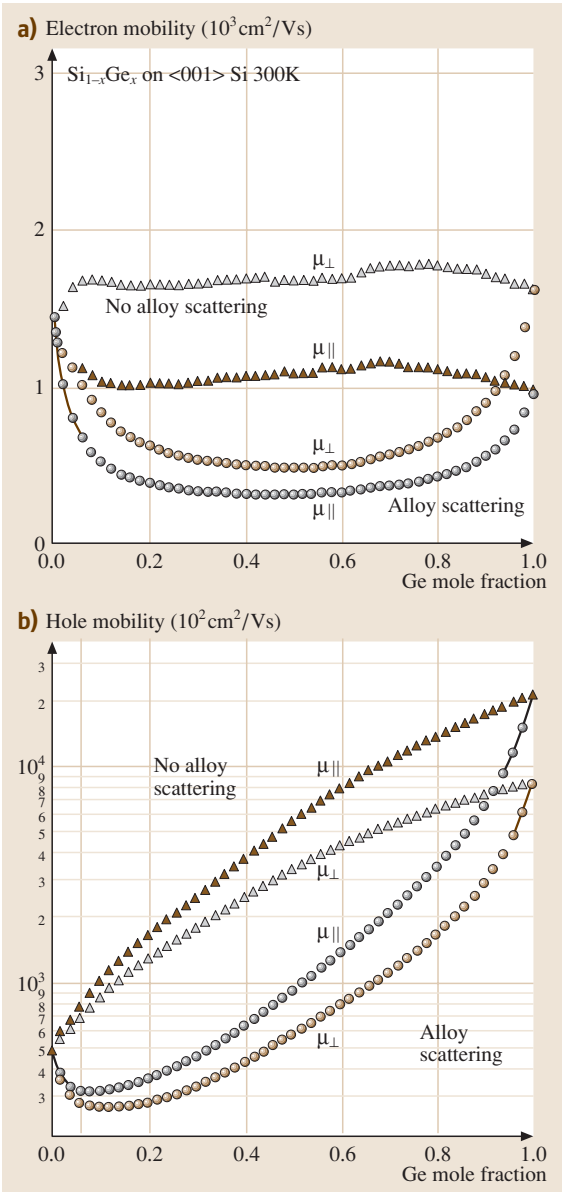


Fig. 22.9a,b Calculated 300-K electron **(a)** and hole **(b)** in-plane and out-of-plane low-field mobilities in strained $Si_{1-x}Ge_x$ grown on (100) Si (after *Fischetti* et al. [22.22], copyright 1996 American Institute of Physics)

band for $Si_{1-x}Ge_x$ to that for silicon as a function of germanium content. It is clear that the density of states in the valence band for $Si_{1-x}Ge_x$ is significantly lower than that for silicon at germanium contents of practical interest.

22.1.5 Majority-Carrier Mobility in Strained $Si_{1-x}Ge_x$

Values of in-plane and out-of-plane low-field mobility in strained $Si_{1-x}Ge_x$ grown on (100) Si have been calculated by *Fischetti* et al. [22.22], and are shown in Fig. 22.9. There is some uncertainty in the chosen values of alloy scattering parameters used in the calculations, but nevertheless the results are representative of current understanding. These results show a large enhancement of low-field hole mobility for $Si_{1-x}Ge_x$ compared with unstrained silicon, but only a modest enhancement of low-field electron mobility. These results indicate that strained $Si_{1-x}Ge_x$ channels can be used to significantly improve the mobility of p-channel MOSFETs, but little benefit is obtained for n-channel MOSFETs. For this reason, industry focus has moved away from channels realised in $Si_{1-x}Ge_x$ to channels realised in tensile-strained silicon, as discussed below.

22.1.6 Majority-Carrier Mobility in Tensile-Strained Si on Relaxed $Si_{1-x}Ge_x$

Tensile-strained silicon can be produced by growing a thin silicon layer on top of a relaxed $Si_{1-x}Ge_x$ virtual substrate. Figure 22.10 shows a typical virtual substrate for a surface-channel MOS transistor. A graded $Si_{1-x}Ge_x$ layer is grown on top of the silicon substrate with the Ge content varying from 0 to 30%. Misfit dislocations will form in this layer, but the majority of dislocations will be in the plane of the $Si_{1-x}Ge_x$ layer and only a small percentage will propagate vertically

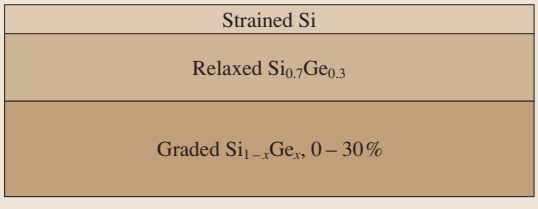


Fig. 22.10 Schematic illustration of a typical tensile-strained Si layer grown on top of a $Si_{1-x}Ge_x$ virtual substrate

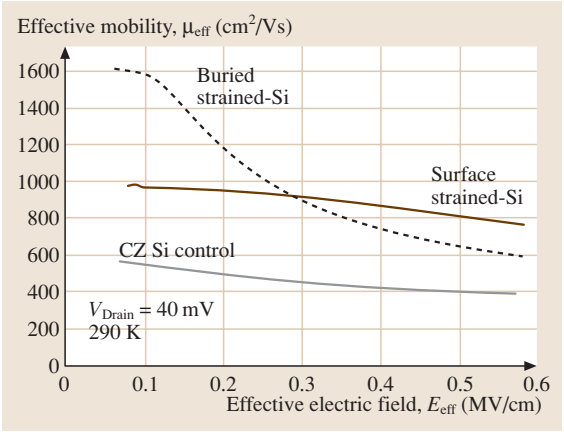


Fig. 22.11 Effective electron mobility as a function of effective electric field for strained Si MOSFETs fabricated on a 30% $Si_{1-x}Ge_x$ virtual substrate (after *Welser* et al. [22.23], copyright 1994 IEEE)

to the surface of the layer. A 30%-relaxed $Si_{1-x}Ge_x$ buffer is then grown followed by a thin tensile-strained $Si_{1-x}Ge_x$ layer in which the channel is fabricated. The key to any virtual substrate growth process is the minimisation of dislocation propagation to the surface of the wafer.

Figure 22.11 shows typical values of effective electron mobility obtained from measurements on n-channel MOS transistors for a $Si_{1-x}Ge_x$ virtual substrate with 30% Ge [22.23]. For the surface-channel strained Si device, the effective mobility is enhanced by 80% compared with the Si control transistor due to the tensile strain in the $Si_{1-x}Ge_x$ layer.

Enhanced hole mobility can also be obtained in tensile-strained Si grown on a $Si_{1-x}Ge_x$ virtual substrate, though higher germanium contents are needed to obtain a significant mobility enhancement. Figure 22.12 shows typical values of effective hole mobility in strained Si for Ge contents between 35 and 50% [22.24]. The effective mobility of the strained Si device is enhanced by 100% compared with the Si control device.

22.1.7 Minority-Carrier Mobility in Strained $Si_{1-x}Ge_x$

$Si_{1-x}Ge_x$ HBTs are minority-carrier devices and hence values of the minority-carrier mobility of more interest than the majority-carrier mobility. Unfortunately very few measurements of minority-carrier mobility have been made in $Si_{1-x}Ge_x$. *Poortmans* [22.20] inferred values of minority-carrier mobility from measure-

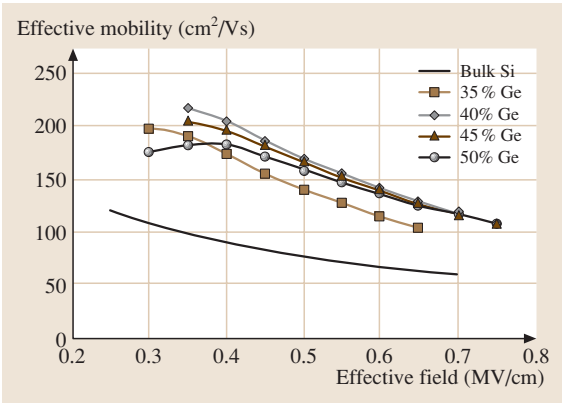


Fig. 22.12 Effective hole mobility as a function of effective electric field for strained Si MOSFETs fabricated on a $Si_{1-x}Ge_x$ virtual substrate with Ge contents in the range 35–50% (after *Leitz* et al. [22.24], copyright 2002 IEEE)

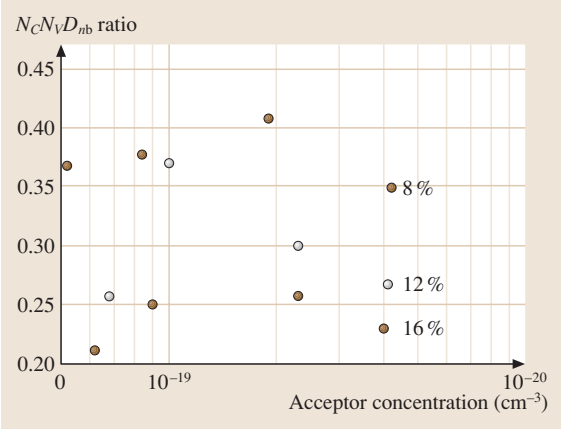


Fig. 22.13 Measured values of the ratio of $N_CN_VD_{nb}$ in $Si_{1-x}Ge_x$ to that in Si as a function of acceptor concentration (after *Poortmans* [22.20], copyright 1993 University of Leuven)

ments on $Si_{1-x}Ge_x$ HBTs and found an enhancement in mobility compared with silicon by a factor of 1.2–1.4 for base doping concentrations in the range 5×10^{18}–5×10^{19} cm^{-3}. Given the scarcity of measured data on minority-carrier mobility and density of states in $Si_{1-x}Ge_x$, the most reliable way of calculating the expected gain improvement in a $Si_{1-x}Ge_x$ HBT is to use data directly obtained from measurements on $Si_{1-x}Ge_x$ HBTs. The gain enhancement in a $Si_{1-x}Ge_x$ HBT is determined by the ratio of the product $N_CN_VD_{nb}$ in $Si_{1-x}Ge_x$ and Si, together with the band-gap narrowing due to the strained $Si_{1-x}Ge_x$. Figure 22.13 shows a graph of this $N_CN_VD_{nb}$ ratio as a function of acceptor concentration for three values of germanium content. It can be seen that for germanium contents of practical interest, in the range 11–16%, this ratio has a value of around 0.25.

22.1.8 Apparent Band-Gap Narrowing in $Si_{1-x}Ge_x$ HBTs

In $Si_{1-x}Ge_x$ HBTs, the apparent band-gap narrowing is often quoted, which combines the effect of the band-gap reduction and the effect of high doping. *Poortmans* et al. [22.17] have developed a theoretical approach that has been shown to be in reasonable agreement with experiment. Figure 22.14 shows the apparent band-gap narrowing in $Si_{1-x}Ge_x$ as a function of acceptor concentration for three values of germanium content. At low acceptor concentrations, the apparent band-gap narrowing in $Si_{1-x}Ge_x$ is slightly higher than that in silicon, but at acceptor concentrations in the range $1–2\times10^{19}$ cm^{-3}, the apparent band-gap narrowing is approximately the same. This latter doping range is the base doping range that is of practical interest for $Si_{1-x}Ge_x$ HBTs.

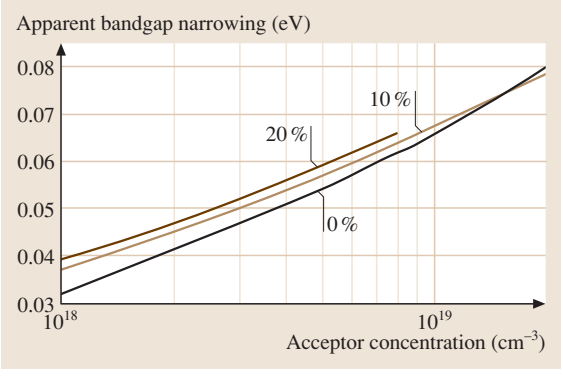


Fig. 22.14 Apparent band-gap narrowing as a function of acceptor concentration for $Si_{1-x}Ge_x$ with three different germanium concentrations (after *Poortmans* et al. [22.17], copyright 1993 Elsevier)

22.2 Optical Properties of SiGe

Interest in the optical properties of SiGe stems from the desire to design silicon-based optoelectronic devices as well as the usefulness of many optical techniques in material analysis. The optical properties of bulk SiGe provides an important starting point for any attempt at in-depth understanding, however, nearly all real applications of SiGe involve the use of thin, strained layers. Beyond this, the formation of SiGe quantum structures within silicon devices has remained one of the most promising methods by which device engineers hope to improve the largely unimpressive optical behaviour of silicon that is brought about by its indirect band gap. The growth of quantum wells, quantum wires and quantum dots in the Si/SiGe system has been extensively explored [22.26–31]. However, there has as yet been little success at using Si/SiGe quantum structures to produce efficient silicon-based light emitters, although there have been impressive attempts [22.31]. Perhaps the most promising devices based on SiGe quantum wells are near-infra-red photodetectors in which the SiGe can be used to enhance sensitivity at the optical-communications wavelengths [22.32–36]. More futuristic applications of SiGe quantum wells include devices based on transitions between the confined energy levels in quantum wells. Devices based on these *inter-subband* transitions include quantum-well infrared photodetectors (QWIPs) [22.37, 38] and quantum cascade lasers [22.39, 40].

22.2.1 Dielectric Functions and Interband Transitions

A range of 1-μm-thick $Si_{1-x}Ge_x$ films grown by MBE on Si(100) substrates have been studied by spectroscopic ellipsometry to yield their complex dielectric functions at room temperature [22.25]. Both the real (ε_1) and imaginary (ε_2) parts of the measured dielectric function for Ge compositions of 0, 0.2, 0.4, 0.6, 0.8 and 1.0 are shown in Fig. 22.15a and b, respectively.

In Fig. 22.15b the absorption structures observed at 3.4 and 4.2 eV in the spectra shown for silicon originate from direct band-to-band transitions at various regions in the Brillouin zone of silicon. The structure seen around 3.4 eV is due to E_0', E_1 and $E_1 + \Delta_1$ interband transition

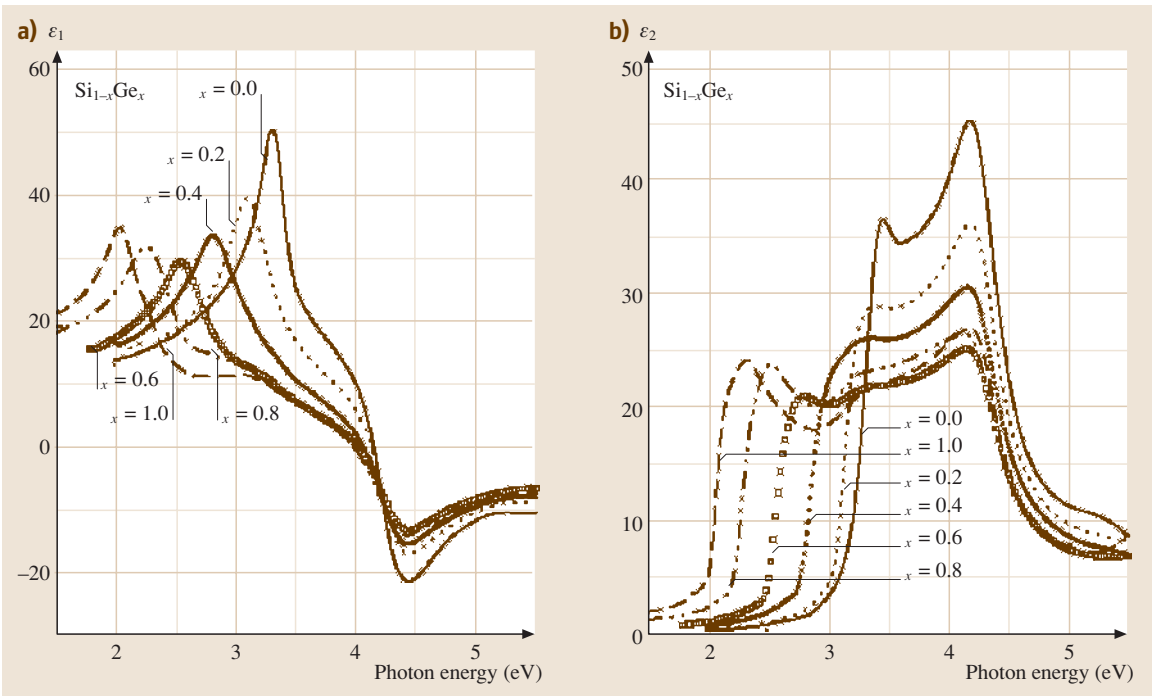


Fig. 22.15a,b Real (**a**) and imaginary (**b**) parts of the dielectric functions of relaxed $Si_{1-x}Ge_x$ alloys with composition x indicated in the legend (after *Bahng* et al. [22.25], copyright 2001, American Physical Society)

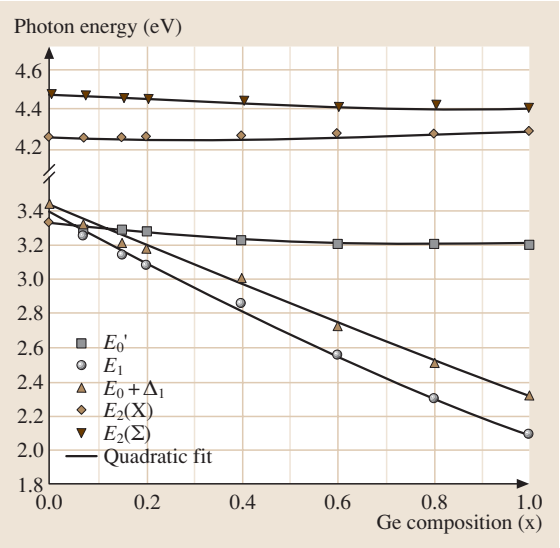


Fig. 22.16 Evolution of E_0', E_1, $E_1+\Delta_1$, E_2 (X) and $E_2(\Sigma)$ transition energies for relaxed $Si_{1-x}Ge_x$ with composition x (after *Bahng* et al. [22.25], copyright 2001, American Physical Society)

edges, whereas the structure at 4.2 eV is due to E_2 (X) and E_2 (Σ) edges [22.25]. The evolution of each of these transition edges for the full range of SiGe compositions is shown in Fig. 22.16.

The quadratic fits shown in Fig. 22.16 are as follows [22.25]:

$$E_0'(x) = 3.337 - 0.348x + 0.222x^2 \quad (22.4)$$

$$E_1(x) = 3.398 - 1.586x + 0.27x^2 \quad (22.5)$$

$$E_1 + \Delta_1(x) = 3.432 - 1.185x + 0.065x^2 \quad (22.6)$$

$$E_2(X)(x) = 4.259 - 0.052x + 0.084x^2 \quad (22.7)$$

$$E_2(\Sigma)(x) = 4.473 - 0.139x + 0.072x^2 \quad (22.8)$$

22.2.2 Photoluminescence

The emission properties of semiconductor structures are of fundamental interest to scientists as well as being an important analytical technique for engineers. In general, the features of low-temperature photoluminescence spectra are very dependent on the specific conditions under which materials are grown and treated. This is because emission energies and emission rates are often sensitive to even small variations of impurity or defect densities, as well as variations in strain or composition. A brief examination of low-temperature photoluminescence spectra is nearly always sufficient to allow a simple qualitative assessment of material quality; alternatively, detailed analysis can permit a broad range of material or structural parameters to be assessed or determined. No two photoluminescence spectra are the same. In this section and the section that follows on photoluminescence studies of Si/SiSe quantum wells, we will present a range of spectra that represent most of the key features that have been observed.

Weber and *Alonso* [22.41] have provided a very useful study of the near-band-gap photoluminescence of bulk SiGe alloys. In their study bulk SiGe samples are cut from nominally undoped polycrystalline ingots prepared by a zone-levelling technique. Figure 22.17 shows the photoluminescence spectra for a range of compositions. Samples were excited using the 514-nm line of an argon ion laser and the sample temperature was 4.2 K.

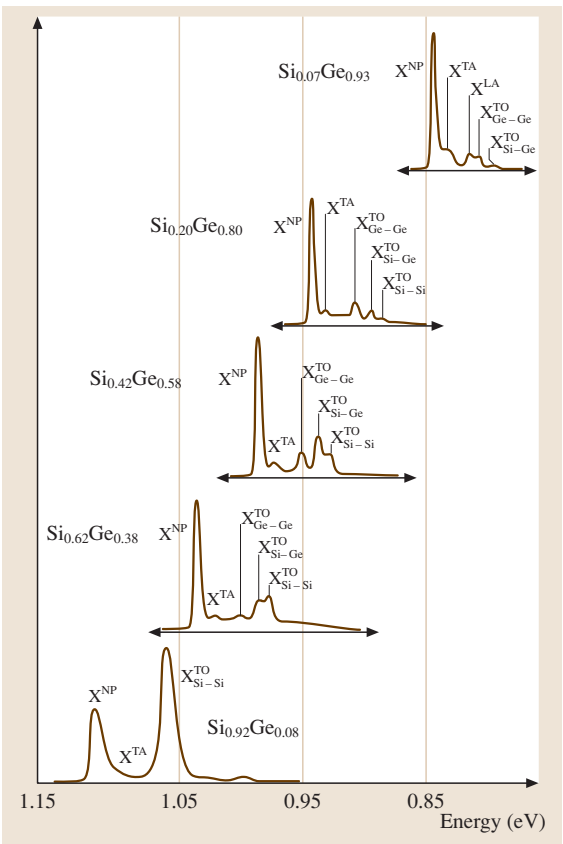


Fig. 22.17 Near-band-gap photoluminescence spectra for several bulk SiGe samples (after *Weber* et al. [22.41], copyright 1989, American Physical Society)

Excitonic emission lines are a strong feature of photoluminescence spectra when the thermal energy of the semiconductor is less than the exciton binding energy. Each spectrum featured in Fig. 22.17, across the full range of SiGe compositions, show similar *excitonic* features.

In most spectra the most pronounced peak is the no-phonon (X^{NP}) line caused by the optical recombination of excitons bound to shallow impurities. In the case of the no-phonon line, momentum is conserved through interaction with the binding impurity. There are many candidate atoms for these shallow impurities and with B, P and As having binding energies of 4.2, 5.0 and 5.6 meV, respectively [22.42]. These bound energy states will tend to dominate luminescence spectra for doped samples and will always tend to be present in nominally undoped samples. The no-phonon line is accompanied by transverse-optical (X^{TO}) or transverse acoustic (X^{TA}) phonon replicas that are created as photon emission is accompanied by the momentum-conserving creation of lattice vibrations in Si–Si, Si–Ge or Ge–Ge bonds.

Figure 22.18 shows how the spectrum from a bulk $Si_{0.915}Ge_{0.085}$ sample develops with increasing temperature [22.41]. With increasing temperature the X^{NP} line thermalises to leave the free-exciton (FE^{NP}) line. Here, emission from nominally free excitons is greatly enhanced for the alloy samples by local fluctuations in composition that provide momentum-conserving scattering centres [22.43].

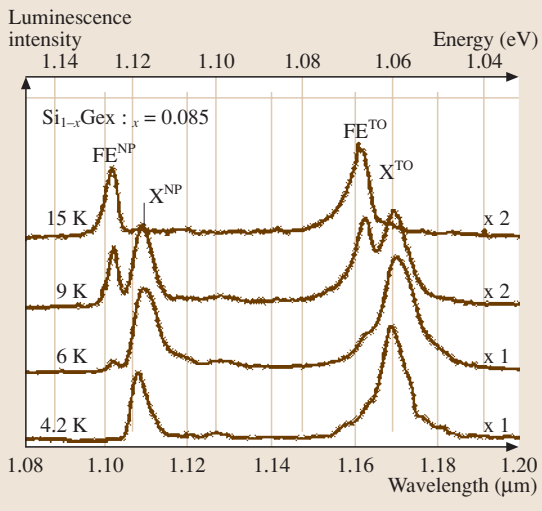


Fig. 22.18 Photoluminescence spectra of a bulk $Si_{0.915}Ge_{0.085}$ sample at different temperatures (after *Weber* et al. [22.41], copyright 1989, American Physical Society)

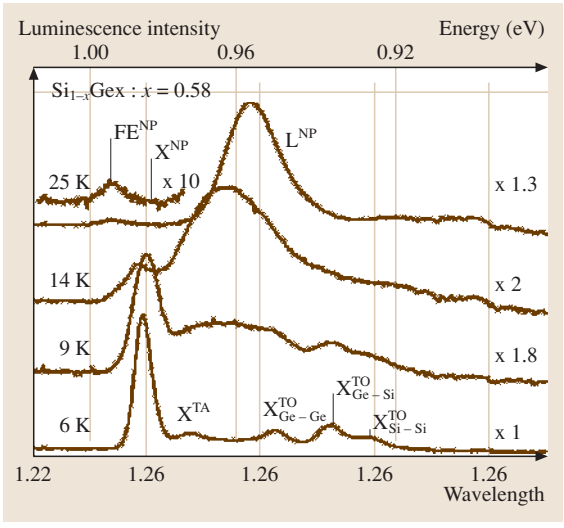


Fig. 22.19 Photoluminescence spectra of a bulk $Si_{0.42}Ge_{0.58}$ sample at different temperatures (after *Weber* et al. [22.41], copyright 1989, American Physical Society)

At higher temperatures the free-exciton line is also thermalised and all fine structure is lost, at temperatures around 25 K broad luminescence bands are commonly observed (Fig. 22.19 [22.41]. These deep luminescence bands are difficult to assign and have been ascribed to impurities, structural defects and, as in the case of the line presented in Fig. 22.19, potential wells formed by alloy fluctuations [22.41].

Weber and *Alonso* [22.41] use their data to provide analytical expressions for both the X^{NP} and L bands for bulk $Si_{1-x}Ge_x$ in the range $0 \le x \le 0.85$ as follows:

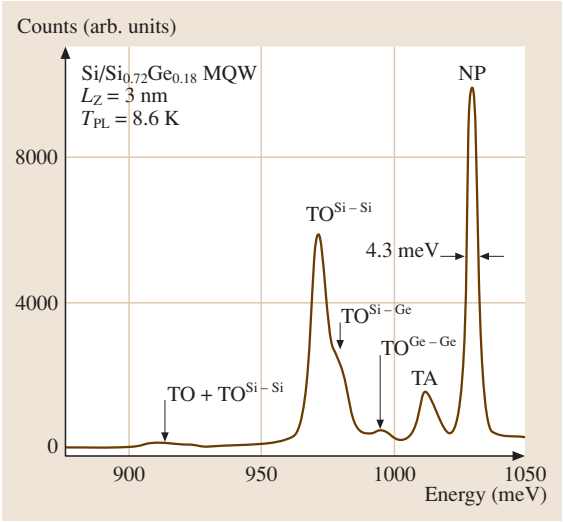
$$E_{gx}^{(x)}(x) = 1.155 - 0.43x + 0.206x^2 \text{ eV} \quad (22.9)$$

$$E_{gx}^{L}(x) = 2.010 - 1.270x \text{ eV} \quad (22.10)$$

At low temperatures narrow excitonic luminescence features are indicative of defect-free material, and in this way low-temperature photoluminescence becomes a good qualitative tool with which material quality can be assessed.

22.2.3 SiGe Quantum Wells

Figure 22.20 shows the first excitonic luminescence spectra from a Si/SiGe multiple quantum well grown by atmospheric-pressure CVD [22.28]. As we can see, many of the features seen in the photoluminescence spectra of quantum-well samples are similar to



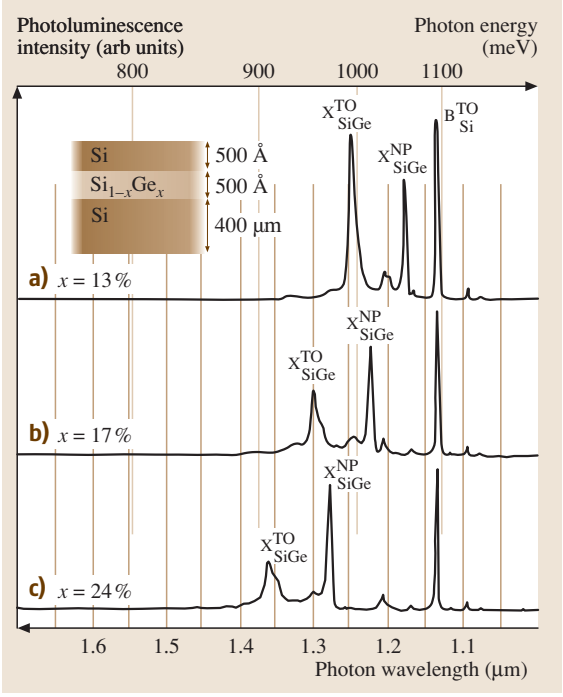


Fig. 22.20 Excitonic photoluminescence spectrum of a SiGe quantum well (after *Grutzmacher* et al. [22.28], copyright 1993, AVS)

Fig. 22.21 4.2-K photoluminescence spectra from layers with the nominal structure shown in the inset (514-nm Ar-ion laser excitation) (after *Robbins* et al. [22.26], copyright 1992, American Physical Society)

those seen from the bulk samples described in the previous section. Again, the most pronounced peak is the no-phonon (NP) line and this is accompanied by phonon replicas, including, impressively, a two-phonon replica of the NP line $\left(\mathrm{TO}+\mathrm{TO}^{\mathrm{Si-Si}}\right)$. The most significant difference between bulk and quantum well spectra is the energy positions of the excitonic features as these are shifted by quantum confinement effects.

Robbins et al. [22.26], have provided one of the most detailed studies of near-band-gap photoluminescence from pseudomorphic SiGe layers and provide analytical expressions for all factors pertaining to the energy positions of the excitonic energy gap for $Si_{1-x}Ge_x$ quantum wells in the range $0 < x < 0.24$. The effects of alloying, confinement, band offsets, alignment type and exciton binding energy are all taken into account. Samples used in the study were grown by low-pressure CVD at 920 °C; a typical set of photoluminescence spectra are shown in Fig. 22.21.

The exciton band gap at 4.2 K is considered for thick (50-nm) strained layers ($E_{\mathrm{X}}^{\mathrm{S}}$) where the energies are not affected by quantum shifts, the following expression is derived:

$$E_{\mathrm{X}}^{\mathrm{S}}(x) = 1.155 - 0.874x + 0.376x^2 \text{ eV}, \ (x < 0.25) \quad (22.11)$$

Here the presence of strain is responsible for the differences from the expression obtained for bulk samples (22.9). An expression for the exciton binding energy $E_{\mathrm{B}}^{\mathrm{C}}(x)$ is theoretically derived for the cubic alloy and the following quadratic expression is fitted:

$$E_{\mathrm{B}}^{\mathrm{C}}(x) \approx 0.0145 - 0.022x + 0.020x^2 \text{ eV}, \ (x < 0.25) \quad (22.12)$$

A strain-corrected expression is also provided but this is found to modify (22.12) only slightly. Thus by adding (22.11) and (22.12) an expression for the band gap can be obtained.

$$E_{\mathrm{C}} - E_{\mathrm{V}} \approx 1.17 - 0.896x + 0.39x^2 \text{ eV}, \ (x < 0.25) \quad (22.13)$$

22.3 Growth of Silicon–Germanium

Over the past ten years and more there have been rapid developments in techniques for the growth of Si and $Si_{1-x}Ge_x$ epitaxial layers at low temperatures. This has been made possible by a number of changes in the design of epitaxy equipment and by improvements to growth processes. There are two main prerequisites for the growth of epitaxial layers at low temperature:

- Establishment of a clean surface prior to growth [22.44–47]
- Growth in an ultra-clean environment [22.48–50]

The removal of oxygen and carbon is the main problem in establishing a clean surface prior to growth. A clean silicon surface is highly reactive and oxidises in air even at room temperature. The secret of low-temperature epitaxial growth is therefore the removal of this native oxide layer and the maintenance of a clean surface until epitaxy can begin. Two alternative approaches to pre-epitaxy surface cleaning have been developed, as described below.

22.3.1 In-Situ Hydrogen Bake

The concept that underlies this surface clean is the controlled growth of a thin surface oxide layer, followed by its removal in the epitaxy reactor using a hydrogen bake. The controlled growth of the surface oxide layer is generally achieved using a Radio Corporation of America (RCA) clean [22.44] or a variant [22.45]. The oxide created by the RCA clean is removed in the reactor using an in-situ bake in hydrogen for around 15 min at a temperature in the range 900–950 °C. The temperature required to remove the native oxide depends on the thickness of the oxide, which is determined by the severity of the surface clean.

22.3.2 Hydrogen Passivation

An alternative approach to pre-epitaxy cleaning is to create an oxide-free surface using an ex-situ clean and then move quickly to epitaxial growth before the native oxide can grow. The aim of the ex-situ clean is to produce a surface that is passivated by hydrogen atoms bonded to dangling bonds from silicon atoms on the surface. When the wafers are transferred in the epitaxy reactor, the hydrogen can be released from the surface of the silicon very quickly using a low-temperature bake or even in the early stages of epitaxy without any bake. *Meyerson* [22.46] has reported that hydrogen desorbs at 600 °C at a rate of a few monolayers per second, so the hydrogen passivation approach allows epitaxial layers to be grown at low temperatures without the need for a high-temperature bake. The hydrogen-passivated surface is stable for typically 30 min after completion of the ex-situ cleaning [22.47].

22.3.3 Ultra-Clean Epitaxy Systems

Having produced a clean hydrogen-passivated silicon surface, it is clearly important to maintain the state of this surface in the epitaxy system. This necessitates the use of low-pressure epitaxy systems if epitaxial growth at low temperatures is required. Figure 22.22 summarises the partial pressures of oxygen and water vapour that need to be achieved in an epitaxy system if an oxide-free surface is to be maintained at a given temperature [22.48, 49]. This figure shows that epitaxial growth at low temperature requires low partial pressures of oxygen and water vapour, which of course can be achieved by reducing the pressure in the epitaxy system. Research [22.50] has shown that a pressure below 30 Torr is needed to achieve silicon epitaxial growth below 900 °C.

22.3.4 $Si_{1-x}Ge_x$ Epitaxy

The growth of $Si_{1-x}Ge_x$ epitaxial layers can be achieved over a wide range of temperatures using low-pressure chemical vapour deposition (LPCVD) [22.50] or ultra-high-vacuum chemical vapour deposition (UHV-CVD) [22.51, 52]. The gas used to introduce the germanium into the layers is germane, GeH_4. The influence of germanium on the growth rate is complex, as illustrated in Fig. 22.23. At temperatures in the range 577–650 °C a peak in the growth rate is seen. At low germanium contents, the growth rate increases with germanium content, whereas at high germanium content, the growth rate decreases with germanium content. In the low-temperature regime it has been proposed that hydrogen desorption from the surface is the rate-limiting step. In $Si_{1-x}Ge_x$ this occurs more easily at germanium sites than at silicon sites and hence the growth rate increases with germanium content [22.37]. As the germanium content increases, the surface contains more and more germanium and less and less hydrogen. The rate-limiting step then becomes the adsorption of germane or silane. *Robbins* [22.53] proposed that the sticking coefficient for germane or silane was lower at germanium sites. This would slow the adsorption rate as the ger-

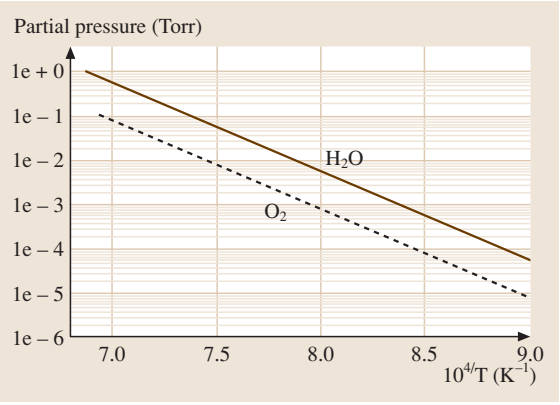


Fig. 22.22 Conditions for oxide formation in an epitaxy system. Note that 1 atm = 1.113 bar = 760 Torr = 1.113×10^5 Pa (after *Smith* and *Ghidini* [22.48, 49], copyright Electrochemical Society 1984)

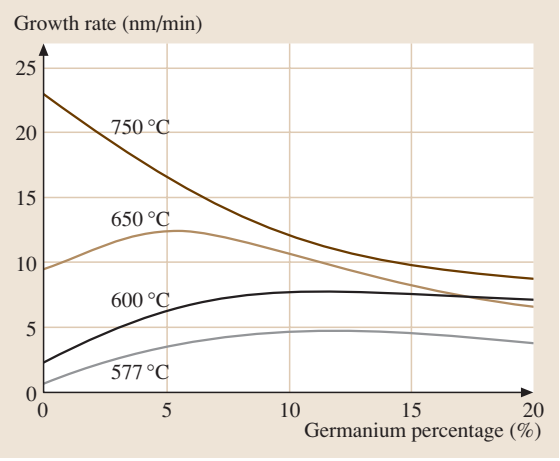


Fig. 22.23 Growth rate of $Si_{1-x}Ge_x$ as a function of germanium percentage for temperatures in the range 577–750 °C (after Racanelli et al. [22.54], copyright 1990, American Institute of Physics)

manium content increased and hence slow the growth rate.

22.3.5 Selective $Si_{1-x}Ge_x$ Epitaxy

Selective epitaxy is the growth of a single-crystal layer in a window, with complete suppression of growth elsewhere, and can be achieved in a number of different ways. The most common method of achieving both selective Si and $Si_{1-x}Ge_x$ epitaxy is by introducing chlorine or HCl into the growth chamber. This can either be done by adding chlorine or HCl as a separate gas or by using a growth gas that contains chlorine, for example dichlorosilane, SiH_2Cl_2. With chlorine chemistry, selective growth of silicon and $Si_{1-x}Ge_x$ can be achieved to both silicon dioxide and silicon nitride.

Chlorine is reported to have two effects that lead to selective growth. First it increases the surface mobility of silicon and germanium atoms, so that atoms deposited on the oxide or nitride layer are able to diffuse across the surface to the window where the growth is occurring. Second it acts as an etch [22.50] and hence can remove silicon or germanium atoms deposited on the oxide or nitride. The strength of the etching action increases with chlorine content and, if the chlorine content is too high, etching of the substrate will occur instead of epitaxial growth.

A typical growth process for selective silicon epitaxy would use silane and a few percent of HCl [22.50]. The growth rate for this process is shown in Fig. 22.24, and compared with the growth rate for dichlorosilane and silane epitaxy. It can be seen that the activation energy for the silane-plus-HCl process is very similar to that for the dichlorosilane process, indicating that the growth mechanisms are similar. One disadvantage of chlorine-based growth processes over the silane process is a lower growth rate at low temperatures, as can clearly be seen in Fig. 22.24. It is also possible to grow silicon selectively using dichlorosilane and HCl [22.55].

Selective $Si_{1-x}Ge_x$ growth is generally easier to achieve than selective silicon growth, as illustrated in

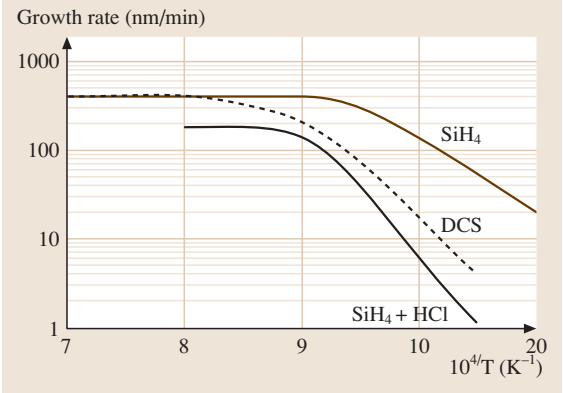


Fig. 22.24 Silicon growth rate as a function of reciprocal temperature for three different growth gases: 40 sccm of SiH_4, 80 sccm of dichlorosilane and 20 sccm of SiH_4 with 2 sccm of HCl. The hydrogen flow was 2 slm (after *Regolini* et al. [22.50], copyright 1989 American Institute of Physics)

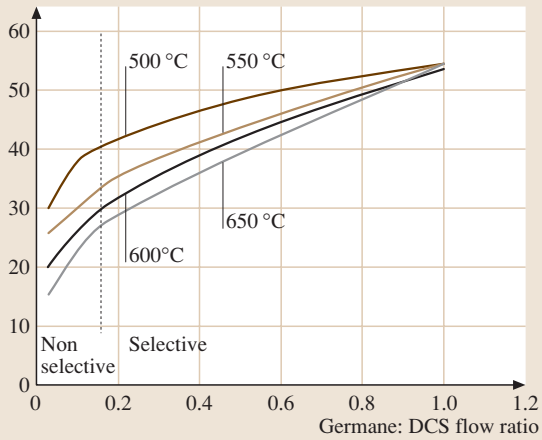


Fig. 22.25 Germanium percentage as a function of germane: dichlorosilane (DCS) flow ratio for temperatures in the range 500–650 °C showing the move from nonselective to selective growth as the proportion of germane in the gas flow increases (after *Zhong* et al. [22.56], copyright 1990, American Institute of Physics)

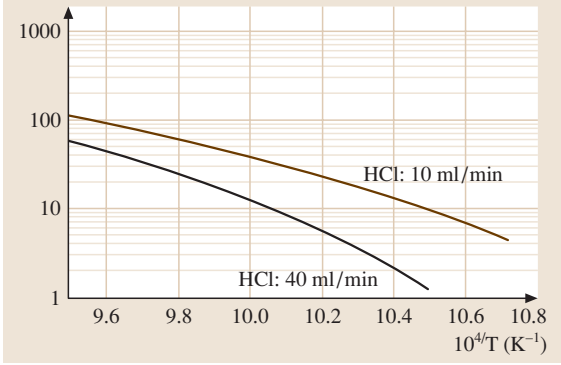


Fig. 22.26 Arrhenius plots for $Si_{1-x}Ge_x$ growth at two different HCl flow rates. The dichlorosilane and germane flow rates were fixed at 100 and 8 ml/min respectively (after *Kiyota* et al. [22.57], copyright 2002, IEEE)

Fig. 22.25 [22.56] for $Si_{1-x}Ge_x$ growth using germane and dichlorosilane. The growth moves from nonselective to selective as the proportion of germane in the gas flow increases.

Arrhenius plots for $Si_{1-x}Ge_x$ growth using germane and dichlorosilane are shown in Fig. 22.26 for $Si_{1-x}Ge_x$ layers grown using germane and dichlorosilane and for two different HCl flows. It can be seen that the growth rate decreases and the activation energy increases with increasing HCl flow. The explanation proposed for this behaviour is that the limiting growth mechanism changes from hydrogen desorption from the growing surface to chlorine or HCl desorption from the surface [22.57]. This decrease in growth rate at high HCl flows is a disadvantage because it leads to increased growth times. High HCl flows can also cause surface roughening when the $Si_{1-x}Ge_x$ layer is heavily boron-doped [22.57]. These considerations demonstrate that the HCl flow should be chosen to be to the smallest value that is consistent with good selective epitaxy.

Silane can be used for selective silicon epitaxy if the growth is performed at a high temperature. This approach relies on the fact that nucleation of growth on oxide is more difficult than that on silicon. This incubation time for growth on an oxide layer is relatively long at high temperatures but much shorter for growth at low temperatures. Selective silicon layers 1 μm thick can be grown using silane at a temperature of 960 °C [22.58], but the achievable layer thickness decreases with decreasing temperature. At 800 °C the maximum selective silicon layer thickness is around 130 nm, at 700 °C it is around 60 nm, and at 620 °C it is around 40 nm. Selective growth to silicon dioxide can be achieved using silane only, but not to silicon nitride.

22.4 Polycrystalline Silicon–Germanium

In the past ten years there has been increasing interest in polycrystalline silicon–germanium for a number of applications that require polycrystalline material deposition at low temperature (around 600 °C). Examples of potential applications are thin film transistors, gates of MOS transistors and polySiGe emitters for SiGe HBTs.

In thin-film transistor technologies [22.59–61], polycrystalline silicon–germanium is compatible with the low-thermal-budget processing that is needed to produce thin-film devices for large-area electronics. The key physical property of polycrystalline silicon–germanium that makes it attractive is its lower melting point than silicon. This means that processes such as deposition,

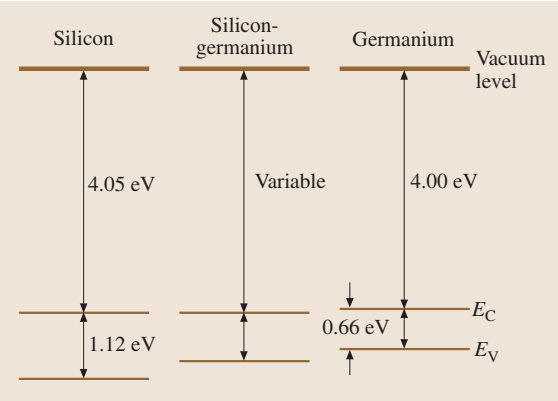


Fig. 22.27 Band-energy levels in silicon, silicon–germanium and germanium

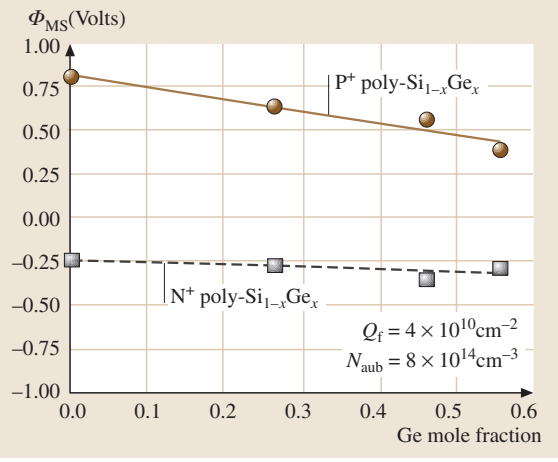


Fig. 22.28 Work-function difference between a polySi$_{1-x}$Ge$_x$ gate and an n-type substrate as a function of germanium content (after *King* et al. [22.60], copyright 1994, IEEE)

crystallisation, grain growth and dopant activation will occur at a lower temperature than in silicon. Thus lower temperature processes can be used for polySiGe devices and hence it is preferable to polySi in applications with tight thermal-budget requirements.

In MOS transistors, polycrystalline silicon–germanium is attractive as a gate material for future generations of MOS transistor, since the germanium content in the silicon–germanium layer can be varied by 200–300 mV in the direction of a mid-gap gate [22.63–65]. This can be understood from Fig. 22.27, which compares the conduction- and valence-band energy levels in single-crystal silicon, silicon–germanium and germanium. Silicon and germanium have similar electron affinities (4.05 and 4.00 eV respectively), but germanium has a much smaller band gap (0.66 eV compared with 1.12 eV). The energy difference between the valence band and the vacuum level is therefore about 0.5 eV smaller in germanium than in silicon. In silicon–germanium, this energy difference can be varied by varying the germanium content. This allows the threshold voltage of p-channel MOS transistors to be tuned by varying the germanium content in the polySi$_{1-x}$Ge$_x$ gate.

Figure 22.28 shows values of work-function difference between the polySi$_{1-x}$Ge$_x$ gate and the n-type silicon substrate as a function of germanium content in a polySi$_{1-x}$Ge$_x$ gate [22.60]. The work function is defined as the difference in energy between the vacuum level and the Fermi level. In p$^+$ polySi$_{1-x}$Ge$_x$ the Fermi level is near the valence band and hence the work-function difference varies strongly with germanium content. In n$^+$ polySi$_{1-x}$Ge$_x$ the Fermi level is near the conduction band and hence the work-function difference varies little with germanium content.

In Si$_{1-x}$Ge$_x$ HBTs, polySi$_{1-x}$Ge$_x$ has potential as an emitter of a SiGe HBT [22.62]. In bipolar transistors, the breakdown voltage, BV_{CEO}, is inversely proportional to the gain [22.66] and hence transistors with a high gain have lower values of breakdown voltage. Si$_{1-x}$Ge$_x$ HBTs inherently have high values of the gain because the reduced band gap of the Si$_{1-x}$Ge$_x$ base enhances the collector current. The base current is unchanged by the Si$_{1-x}$Ge$_x$ base and hence the gain, which is the

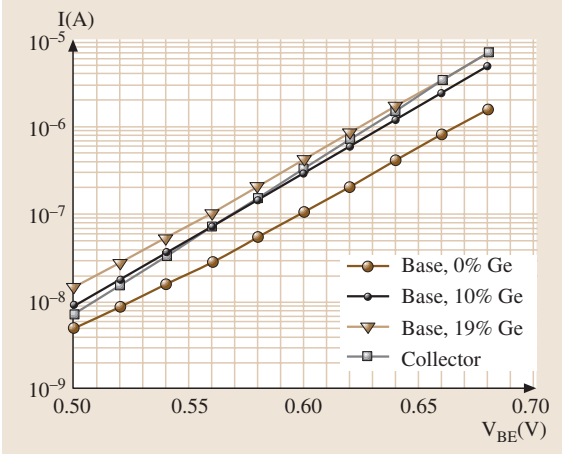


Fig. 22.29 Use of a polySi$_{1-x}$Ge$_x$ emitter to vary the base current of a Si$_{1-x}$Ge$_x$ HBT and hence give the best trade-off between gain and breakdown voltage BV_{CEO}. (after *Kunz* et al. [22.62], copyright 2003, IEEE)

ratio of collector current to base current, is increased. The use of a polySi$_{1-x}$Ge$_x$ emitter instead of a polySi emitter provides a reduced band gap in the emitter, which enhances the base current, and thereby reduces the gain. Typical measured values of base current in a polySi$_{1-x}$Ge$_x$ emitter are shown in Fig. 22.29, where it can be seen that 19% germanium gives a factor of approximately four reduction in gain. A polySi$_{1-x}$Ge$_x$ emitter therefore allows the gain to be tuned to give the best trade-off between gain and breakdown voltage BV_{CEO}.

22.4.1 Electrical Properties of Polycrystalline Si$_{1-x}$Ge$_x$

Figure 22.30 shows the sheet resistance as a function of anneal temperature for boron- and phosphorus-doped Si$_{1-x}$Ge$_x$ for different germanium contents. For boron-doped polySi$_{1-x}$Ge$_x$ the sheet resistance decreases with increasing germanium content, with the decrease being large between 0 and 25% germanium and smaller between 25 and 50% germanium. In contrast, for phosphorus-doped polySi$_{1-x}$Ge$_x$ the sheet resistance

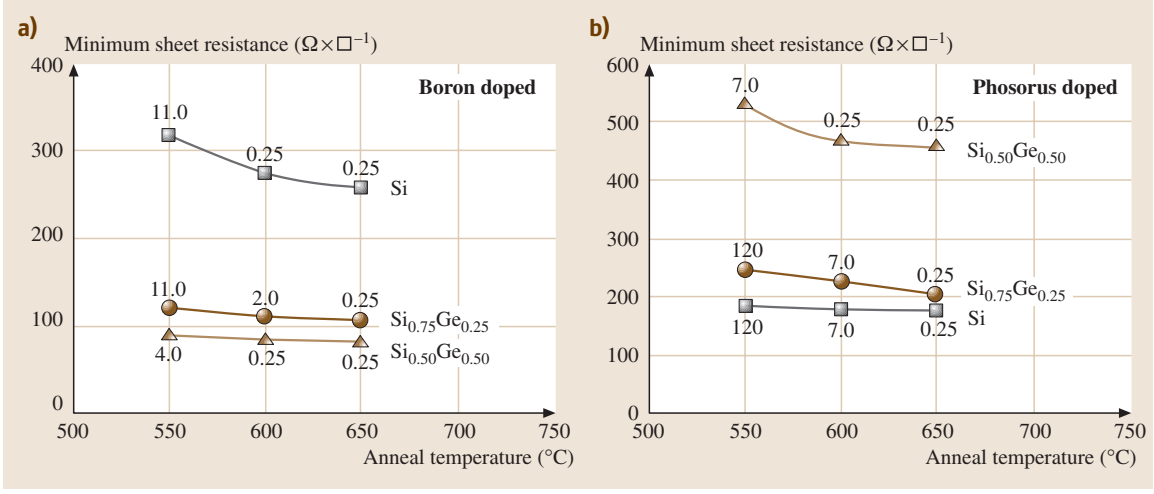


Fig. 22.30 Sheet resistance as a function of anneal temperature for boron- and phosphorus-doped polycrystalline Si$_{1-x}$Ge$_x$ with various germanium contents (after *Bang* et al. [22.67], copyright 1995, American Institute of Physics)

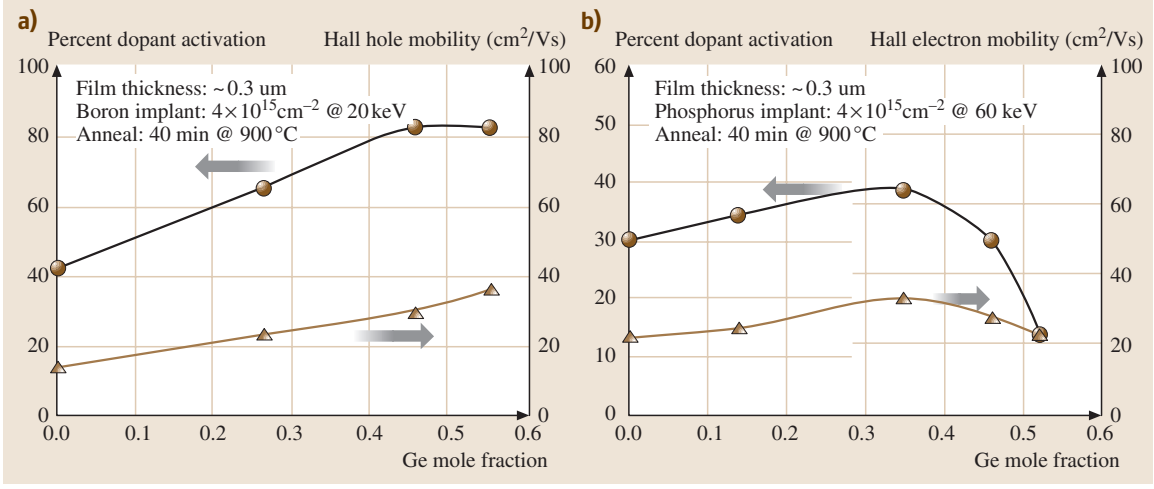


Fig. 22.31 Percentage dopant activation and Hall hole mobility as a function of germanium content for boron- and phosphorus-doped polySi$_{1-x}$Ge$_x$ (after *King* et al. [22.60], copyright 1994, IEEE)

increases with increasing germanium content, with the increase being small between 0 and 25% germanium and large between 25 and 50%. Similar behaviour is seen for arsenic-doped polySi$_{1-x}$Ge$_x$ where higher values of sheet resistance have been reported for polySi$_{1-x}$Ge$_x$ than for polySi [22.64].

The explanation for the sheet-resistance results in Fig. 22.30 can be found in Fig. 22.31, which shows the results of Hall measurements [22.60]. For boron-doped polySi$_{1-x}$Ge$_x$ both the activation and the Hall mobility increase with increasing germanium content, thereby explaining the decrease in sheet resistance with increasing germanium content. For phosphorus-doped polySi$_{1-x}$Ge$_x$ there is little change in activation and electron mobility at low germanium contents, but a sharp decrease in activation at germanium contents above 35%. This explains the sharp increase in sheet resistance seen in Fig. 22.30 for germanium contents between 25 and 50%. The decrease in activation at high germanium contents in the phosphorus-doped polySi$_{1-x}$Ge$_x$ may be due to increased segregation at grain boundaries. Boron does not generally segregate to grain boundaries [22.68], which may explain the different behaviour in boron- and phosphorus-doped polySi$_{1-x}$Ge$_x$.

References

22.1 R. Braunstein, A. R. Moore, F. Herman: Phys. Rev. **109**, 695 (1958)
22.2 S. S. Iyer, G. L. Patton, J. M. C. Stork, B. S. Meyerson, D. L. Harame: IEEE Trans. Electron. Dev. **36**, 2043 (1989)
22.3 C. A. King, J. L. Hoyt, J. F. Gibbons: IEEE Trans. Electron. Dev. **36**, 2093 (1989)
22.4 H. Miyata, T. Yamada, D. K. Ferry: Appl. Phys. Lett. **62**, 2661 (1993)
22.5 T. Vogelsang, K. R. Hofmann: Appl. Phys. Lett. **63**, 186 (1993)
22.6 J. Welser, J. L. Hoyt, J. F. Gibbons: IEEE Electron. Dev. Lett. **15**, 100 (1994)
22.7 A. Sadak, K. Ismile, M. A. Armstrong, D. A. Antoniadis, F. Stern: IEEE Trans. Electron. Dev. **43**, 1224 (1996)
22.8 B. Jagannathan, M. Khater, F. Pagette, J.-S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D. R. Greenberg, R. Groves, S. J. Jeng, J. Johnson, E. Mengistu, K. T. Schonenberger, C. M. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K. Stein, S. Subbanna: IEEE Electron Dev. Lett. **23**, 258 (2002)
22.9 Z. A. Shafi, P. Ashburn, G. J. Parker: IEEE J. Solid State Circuits **25**, 1268 (1990)
22.10 S. C. Jain, T. J. Gosling, J. R. Willis, R. Bullough, P. Balk: Solid State Electron. **35**, 1073 (1992)
22.11 J. M. Matthews, A. E. Blakeslee: J. Cryst. Growth **27**, 118 (1974)
22.12 J. M. Matthews, A. E. Blakeslee: J. Cryst. Growth **32**, 265 (1975)
22.13 R. People, J. C. Bean: Appl. Phys. Lett. **47**, 322 (1985)
22.14 S. Margalit, A. Bar-lev, A. B. Kuper, H. Aharoni, A. Neugroschel: J. Cryst. Growth **17**, 288 (1972)
22.15 O. W. Holland, C. W. White, D. Fathy: Appl. Phys. Lett. **51**, 520 (1987)
22.16 R. People: Phys. Rev. B **32**, 1405 (1985)
22.17 J. Poortmans, S. C. Jain, D. H. J. Totterdell, M. Caymax, J. F. Nijs, R. P. Mertens, R. Van Overstraeten: Solid State Electron. **36**, 1763 (1993)
22.18 T. Manku, A. Nathan: J. Appl. Phys. **69**, 8414 (1991)
22.19 T. Manku, A. Nathan: Phys. Rev. B **43**, 12634 (1991)
22.20 J. Poortmans: Low temperature epitaxial growth of silicon and strained Si$_{1-x}$Ge$_x$ layers and their application in bipolar transistors; PhD thesis, University of Leuven (1993)
22.21 J. M. McGregor, T. Manku, A. Nathan: *Measured in-plane hole drift mobility and Hall mobility in heavily doped, strained p-type* Si$_{1-x}$Ge$_x$ (Boston 1992) presented at Electronic Materials Conference
22.22 M. V. Fischetti, S. E. Laux: J. Appl. Phys. **80**, 2234 (1996)
22.23 J. Welser, J. L. Hoyt, J. F. Gibbons: IEEE Electron. Dev. Lett. **15**, 100 (1994)
22.24 C. W. Leitz, M. T. Currie, M. L. Lee, Z.-Y. Cheng, D. A. Antoniadis, E. A. Fitzgerald: J. Appl. Phys. **92**, 3745 (2002)
22.25 J. H. Bahng, K. J. Kim, H. Ihm, J. Y. Kim, H. L. Park: J. Phys.: Condens. Matter **13**, 777 (2001)
22.26 D. J. Robbins, L. T. Canham, S. J. Barnett, A. D. Pitt, P. Calcott: J. Appl. Phys. **71**, 1407 (1992)
22.27 N. L. Rowell, J.-P. Noel, D. C. Houghton, A. Wang, D. D. Perovic: J. Vac. Sci. Technol. B **11**, 1101 (1993)
22.28 D. A. Grutzmacher, T. O. Sedgwick, G. A. Northrop, A. Zaslavsky, A. R. Powell, V. P. Kesan: J. Vac. Sci. Technol. B **11**, 1083 (1993)
22.29 J. Brunner, J. Nutzel, M. Gail, U. Menczigar, G. Abstreiter: J. Vac. Sci. Technol. B **11**, 1097 (1993)
22.30 K. Terashima, M. Tajima, T. Tatsumi: J. Vac. Sci. Technol. B **11**, 1089 (1993)
22.31 H. Prestling, T. Zinke, A. Splett, H. Kibbel, M. Jaros: Appl. Phys. Lett. **69**, 2376 (1996)
22.32 L. Masarotto, J. M. Hartmann, G. Bremond, G. Rolland, A. M. Papon, M. N. Semeria: J. Cryst. Growth **255**, 8 (2003)
22.33 J. S. Park, T. L. Lin, E. W. Jones, H. M. Del Castillo, S. D. Gunapall: Appl. Phys. Lett. **64**, 2370 (1994)
22.34 S. S. Murtaza, J. C. Cambell, J. C. Bean, L. J. Peticolas: IEEE Photon. Tech. Lett. **8**, 927 (1996)

22.35 D.J. Robbins, M.B. Stanaway, W.Y. Leong, R.T. Carline, N.T. Gordon: Appl. Phys. Lett. **66**, 1512 (1995)
22.36 A. Chin, T.Y. Chang: Lightwave Technol. **9**, 321 (1991)
22.37 R. People, J.C. Bean, C.G. Bethia, S.K. Sputz, L.J. Peticolas: Appl. Phys. Lett. **61**, 1122 (1992)
22.38 P. Kruck, M. Helm, T. Fromherz, G. Bauer, J.F. Nutzel, G. Abstreiter: Appl. Phys. Lett. **69**, 3372 (1996)
22.39 R.A. Soref, L. Friedman, G. Sun: Superlattices Microstruct. **23**, 427 (1998)
22.40 G. Sun, L. Friedman, R.A. Soref: Superlattices Microstruct. **22**, 3 (1998)
22.41 J. Weber, M.I. Alonso: Phys. Rev. B **40**, 5684 (1989)
22.42 H. Landolt, R. Bornstein: *Numerical data and functional relationships in science and technology*, Vol. 111/17a, ed. by O. Madelung (Springer, Berlin Heidelberg New York 1982)
22.43 G.S. Mitchard, T.C. McGill: Phys. Rev. B **25**, 5351 (1982)
22.44 M. Meuris, S. Verhaverbeke, P.W. Mertens, M.M. Heyns, L. Hellemans, Y. Bruynseraede, A. Philipessian: Jpn. J. Appl. Phys. **31**, L1514 (1992)
22.45 A. Ishizaki, Y. Shiraki: J. Electrochem. Soc. **129**, 666 (1986)
22.46 B.S. Meyerson, F.J. Himpsel, K.J. Uram: Appl. Phys. Lett. **57**, 1034 (1990)
22.47 G.S. Higashi, Y.T. Chabal, G.W. Trucks, K. Raghavachari: Appl. Phys. Lett. **56**, 656 (1990)
22.48 F.W. Smith, G. Ghidini: J. Electrochem. Soc. **129**, 1300 (1982)
22.49 G. Ghidini, F.W. Smith: J. Electrochem. Soc. **131**, 2924 (1984)
22.50 J.L. Regolini, D. Bensahel, E. Scheid, J. Mercier: Appl. Phys. Lett. **54**, 658 (1989)
22.51 G.R. Srinivasan, B.S. Meyerson: J. Electrochem. Soc. **134**, 1518 (1987)
22.52 M. Racanelli, D.W. Greve, M.K. Hatalis, L.J. van Yzendoorn: J. Electrochem. Soc. **138**, 3783 (1991)
22.53 D.J. Robbins, J.L. Glasper, A.G. Cullis, W.Y. Leong: J. Appl. Phys. **69**, 3729 (1991)
22.54 M. Racanelli, D.W. Greve: Appl. Phys. Lett. **56**, 2524 (1990)
22.55 A. Ishitani, H. Kitajima, N. Endo, N. Kasai: Jpn. J. Appl. Phys. **28**, 841 (1989)
22.56 Y. Zhong, M.C. Ozturk, D.T. Grider, J.J. Wortman, M.A. Littlejohn: Appl. Phys. Lett. **57**, 2092 (1990)
22.57 Y. Kiyota, T. Udo, T. Hashimoto, A. Kodama, H. Shimamoto, R. Hayami, E. Ohue, K. Washio: IEEE Trans. Electron. Dev. **49**, 739 (2002)
22.58 J.M. Bonar: "Process development and characterisation of silicon and silicon–germanium grown in a novel single-wafer LPCVD system"; *PhD thesis*, University of Southampton (1996)
22.59 T.-J. King, K.C. Saraswat: IEDM Tech. Dig., 567 (1991)
22.60 T.-J. King, K.C. Saraswat: IEEE Trans. Electron. Dev. **41**, 1581 (1994)
22.61 J.A. Tsai, A.J. Tang, T. Noguchi, R. Reif: J. Electrochem. Soc. **142**, 3220 (1995)
22.62 V.D. Kunz, C.H. de Groot, S. Hall, P. Ashburn: IEEE Trans. Electron. Dev. **50**, 1480 (2003)
22.63 T.-J. King, J.R. Pfiester, K.C. Saraswat: IEEE Electron. Dev. Lett. **12**, 533 (1991)
22.64 C. Salm, D.T. van Veen, D.J. Gravesteijn, J. Holleman, P.H. Woerlee: J. Electrochem. Soc. **144**, 3665 (1997)
22.65 Y.V. Ponomarev, P.A. Stolk, C.J.J. Dachs, A.H. Montree: IEEE Trans. Electron. Dev. **47**, 1507 (2000)
22.66 P. Ashburn: *Silicon-germanium heterojunction bipolar transistors* (Wiley, Chichester 2003)
22.67 D.S. Bang, M. Cao, A. Wang, K.C. Saraswat, T.-J. King: Appl. Phys. Lett. **66**, 195 (1995)
22.68 I.R.C. Post, P. Ashburn: IEEE Trans. Electron. Dev. **38**, 2442 (1991)