Chapter 7

CIRCUIT LEVEL RF MODELING AND DESIGN

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Abstract: The compact model has been improved due to device scaling and its accuracy has been going to be acceptable for analog circuit design. However, by viewpoint of RF circuit prediction, its accuracy is still poor even if using the recent MOSFET's compact model because it is necessary to implement all parasitic components effects to obtain good accuracy of RF circuit design. Moreover, it has still some insufficient phenomena in the recent small geometry MOSFET. One is the mobility degradation due to STI stress and another one is the channel noise enhancement due to hot carrier effects. This chapter focuses on and describes these uncovered or insufficient characterizations for MOSFET and their influence on RF design, especially voltage-controlled oscillator design.

Key words: RF Model; MOSFET; STI Stress; Scalable Parasitic Components Model; Channel Noise; Voltage-Controlled Oscillator Design

1. Introduction

The downscaling of the design rule of semiconductor technology has realized many features that were unavailable in previous generations of LSIs. Logic LSIs have come to employ higher-level integration and provide high-speed functions, leading to realization of high-performance CPUs such as Pentium-IV. RF-analog LSIs [1] also employ higher-frequency operation such as 5 GHz front-end and more than 10 GHz building block of radio communications. Since the cut-off frequency of MOSFET is approximately dependent on inverse gate length, cut-off frequency of over 200 GHz has already been achieved using sub 0.1 micron design rule. Although scaling-down is thought

W. Grabinski, B. Nauwelaers and D. Schreurs (eds.),
Transistor Level Modeling for Analog/RF IC Design, 181–207.

not to pose problems, for either logic circuit or analog circuit design, there are drawbacks in the case that part of the circuit is analog. RF circuit designers are often faced with the inaccuracy and inconvenience of a compact model since the extraction of the parameter set is not perfect and sometimes the model does not express many physical phenomena even if it covers them.

The drawbacks are increased flicker noise due to introducing oxynitride in recent small geometry MOSFETs, current degradation due to shallow trench isolation (STI) stress, and increasing channel noise due to hot carrier effect in small geometry MOSFETs. Moreover, the normal MOSFET model is insufficient for RF circuit design since MOSFET's parasitic components are not introduced in the Spice model and the RF characteristics are significantly influenced by parasitic components [2].

The issue of STI stresses [3], basically, mechanical stress induced by STI, affects the carrier mobility and this influence depends on distance between edge of STI and channel. In the case of RF-analog circuit, multi-gate finger structure of MOSFET has been widely used, and MOSFET with such a structure has many channels. The mobility degradation due to STI stress differs for each channel. Therefore, drain current and transconductance of MOSFET are not precisely proportional to the number of gate fingers.

For RF design, substrate network model is one of the most important and it has often influenced circuit design accuracy, especially noise. There are some parasitic network models but there is no scalable parasitic network model. The scalable substrate model is strongly required by almost all designers.

Increases in channel noise due to scaling down of gate length is the most serious problem and has been the object of a greater deal of study [4–16] since this phenomenon had not been introduced in any Spice models although its existence has been known for over ten years.

This chapter, focuses on STI stress, parasitic component network and the channel noise enhancement of small geometry MOSFET and describe their influence on current mirror design and RF voltage-controlled oscillator design.

2. STI Stress

2.1. Origin of STI Stress

In the Si integrated circuit process, the isolation region was basically formed with thermal oxidation process. However, thermal oxidation process such as LOCOS isolation was limited so as to minimize isolation region due to bird's beak. Hence, shallow trench isolation (STI) has been utilized below $0.25\,\mu m$ process technologies. STI consists of shallow (approximately 0.3 to $0.5\,\mu m$) trench isolation etching and oxide is filled in it. These types of trench isolation had been used in BiCMOS process for over ten years. Of course, in the case

of BiCMOS process, approximately 5 μm depth deep trench isolation (DTI) or the combination of DTI and STI were used since the depth of collector buried layer is approximately 3 to 4 μm from surface. Also, mechanical stress of DTI or the combination of DTI and STI has been the object of much study [17, 18]. The determined stress in that work showed compressive stress, which was observed around trench isolations and it also depended on the distance from trench isolation. Figure 1 shows compression stress by DTI (left hand) and leakage current of pn-junction as a function of distance from trench isolation (right hand).

2.2. STI Stress on Small Geometry MOSFET

Similar to isolation in the case of BiCMOS process [19], the mechanical stress in the vicinity of active area (AA) is determined by the distance from STI edge. Thus, the mobility of electron of NMOSFET decreases as a function of inverse of the distance between them, resulting in -15% at the vicinity of STI edge. On the other hand, the mobility of hole of PMOSFET increases as a function of inverse of the distance between them, resulting in $+15\%$ at the vicinity of STI edge, vice versa.

These phenomena make it difficult to keep model scalability of MOSFET. In the conventional MOSFET's Spice model scalability of L_g and W_g is kept for both DC and CV parameters. Hence, DC characteristics depend on W_g/L_g but not on AA. However, it is necessary to add some parameter to correct this mobility dependence of distance on distance from STI. In practice, carrier mobility

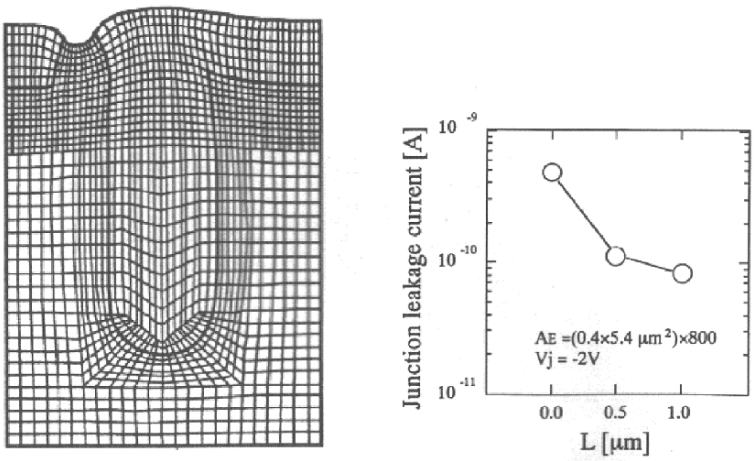

Figure 1. Displaced stress simulated mesh (left hand) and junction leakage current as a function of distance between DTI and active (right hand).

difference poses little problem for logic circuitry provided characterization for each gate (inverter, NAND, etc.) is perfect; however, it poses serious problems for analog circuitry including RF since MOSFET with multi-finger structure is often used in such circuitry. For multi-finger MOSFET, many gate fingers (channels) are available in a MOSFET and the edge of gate finger (channel) is influenced by mobility differences and the inner gate fingers (channels) are not influenced by them. Therefore, the transistor model of edge channels and that of inner channels differ. The ratio of stressed gate can be expressed as Eq. (1).

$$R_{\mathrm{STRESS}} = \frac{2nW_f}{W_g} = \frac{2nW_f}{W_f \cdot M_g} = \frac{2n}{M_g} \tag{1}$$

where, W_f is gate width for finger, M_g is number of gate fingers, W_g is total gate width, $W_g = W_f \times M_g$, and n is number of stressed gate for each side. Therefore, when number of gate finger is large, stressed gate ratio is small in other words, when gate finger width is large, stressed gate ratio is large in the case of constant total gate width.

Figure 2 shows NMOSFET transconductance dependence on gate finger width for 90 nm process with $L_g = 70\,\mathrm{nm}$, and $0.13\,\mu\mathrm{m}$ process with $L_g = 0.11\,\mu\mathrm{m}$ in the case that total gate width $= 100\,\mu\mathrm{m}$. As gate finger width is larger, STI stress appears.

To prevent this phenomenon, multi-finger MOSFET with dummy gate in both edges will be sufficient as shown in Figure 3. The upper figure of Figure 3

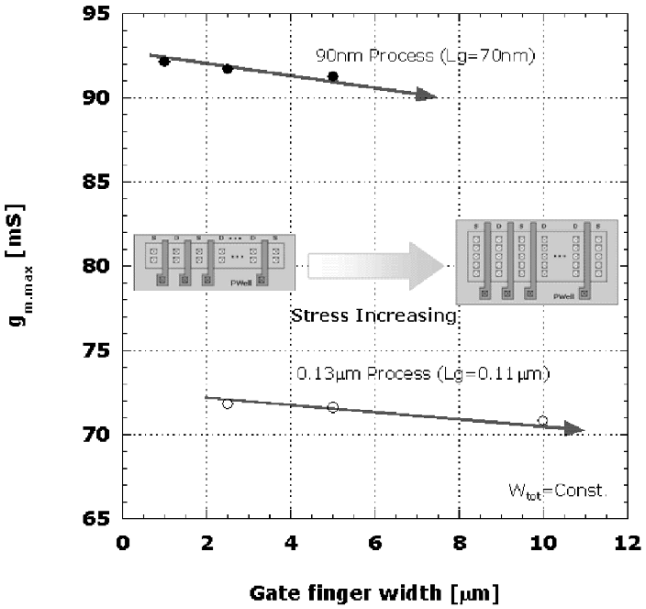

Figure 2. Transconductance degradation as a function of gate finger width.

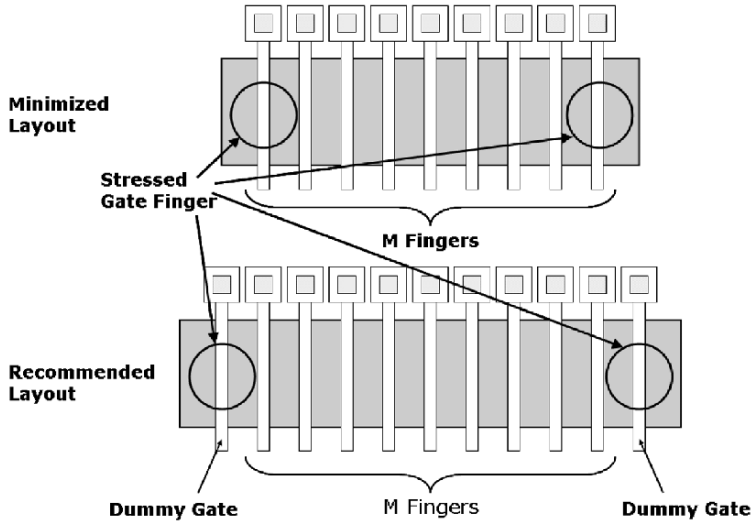

Figure 3. Stressed layout (upper) and stress-free layout (lower).

shows multi-finger MOSFET without dummy gate. This MOSFET layout makes it possible to minimize the layout but accuracy of transistor current is poor due to stressed channel. On the other hand, the lower figure of Figure 3 shows multi-finger MOSFET with dummy gate. This MOSFET layout makes it possible to obtain accurate transistor current but the layout is larger than in the case depicted in the upper figure. Since MOSFET with dummy gate may be necessary for analog circuit, the layout depicted in the lower figure is preferable for analog circuit.

2.3. Current Mirror Circuit Characteristics

The influence of STI stress was studied by using current mirror circuitry. Usually, a current mirror circuit consists of a pair of MOSFETs, one having a small number of gate fingers and the other having a large number of gate fingers and their mirror ratio is determined by only the ratio of the numbers of gate fingers. The mirror ratio is always constant except in the lower early voltage region. However, when STI stress exists, the mirror ratio is different from ideal gate finger ratio and it may depend on the difference of R_{STRESS} as represented by Eq. (1). The calculated mirror ratio as a function of R_{STRESS} is shown in Figure 4.

The designed mirror ratio of this circuitry is ten but when the stressed gate ratio increases, the accuracy of mirror ratio of current mirror circuit degrades.

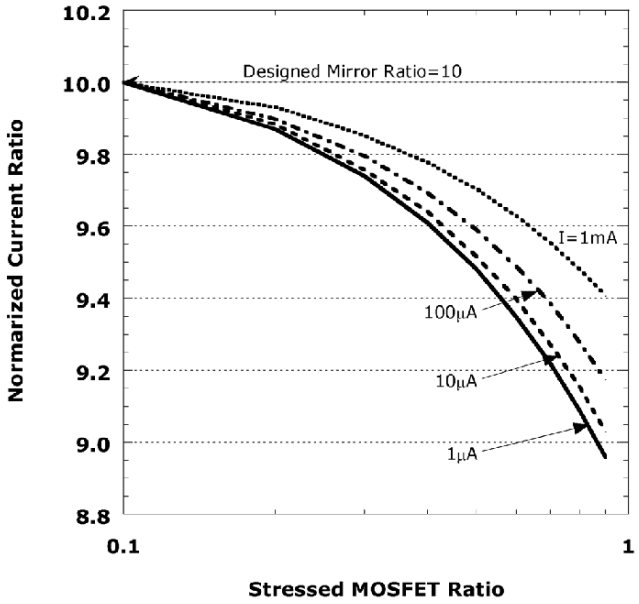

Figure 4. Mirror ratio as a function of stressed finger ratio (R_{STRESS}).

There may be a 10% difference from the designed mirror ratio in the case that R_{STRESS} is one. This difference is significantly large for analog circuit.

2.4. Summary

STI stress induced mobility degradation is on one of the most serious issues for RF circuit design and especially so in regard to transistor matching requirements with multi-finger MOSFET. Designers have to implement a dummy-gate structure or a model parameter set to cover each channel's parameter so as to prevent inaccuracy.

3. Parasitic Network Model for MOSFET

The available SPICE model of CMOS does not include parasitic components perfectly such as gate resistance, well resistance, substrate resistance, and capacitance between well and substrate. It is well known that the RF characteristic of MOSFET is strongly influenced by these parasitic components, and the influences of these components are investigated in some reports [20–24]. New types of SPICE model such as BSIM4 and/or EKV3 include the substrate network; however, the parameter values of components are set for individual

transistors even if only L_g, W_g, and M_g change. This is difficult and complicates the work of circuit designers, because many circuit designers are unfamiliar with process technology and they use a lot of MOSFETs in their circuit designs.

In this section, the scalable model of parasitic components for MOSFET is described. Each parasitic component's value can be calculated using only three basic parameters, L_g, W_f, and M_g, and the model adaptable to transistors of any size [25].

3.1. Equations for Parasitic Components

The equation for parasitic components was determined by equivalent circuit as shown in Figure 5 and target layout of MOSFET as shown in Figure 6.

The core transistor model is the normal BISM3v3 model [26] without source/drain junction capacitance (set C_j and C_{jsw} equal zero) and gate-bulk capacitance (also set C_{gbo} equal zero). The source/drain junction capacitance, gate-bulk capacitance, gate resistance, substrate resistance underlying source/drain junction, substrate resistance underlying gate-bulk capacitance, and parasitic inductance of each terminal were added to the intrinsic BSIM3v3 in this model.

Multi-finger MOSFET is commonly used in RF application to improve parasitic effects as shown in Figure 6. The present work focuses on a MOSFET that has this structure. In the case of a multi finger-MOSEFT, all finger structures are the same and the structure is repeated except at the edge part of transistors. It means some parameters, such as the distance between center of gate and back

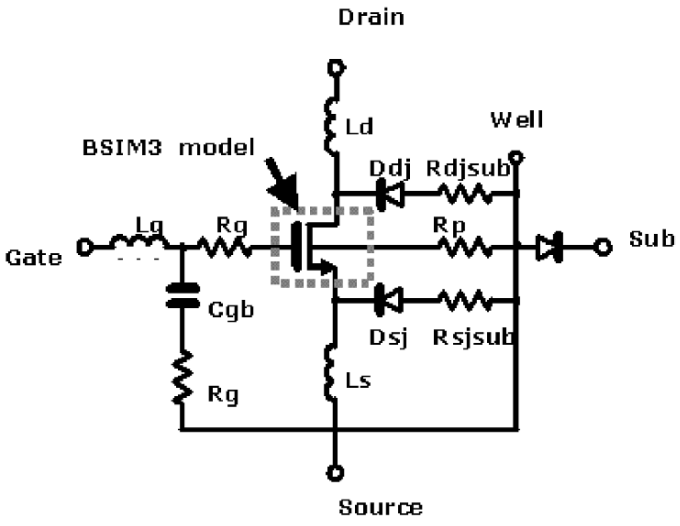

Figure 5. Equivalent circuit MOSFET for RF.

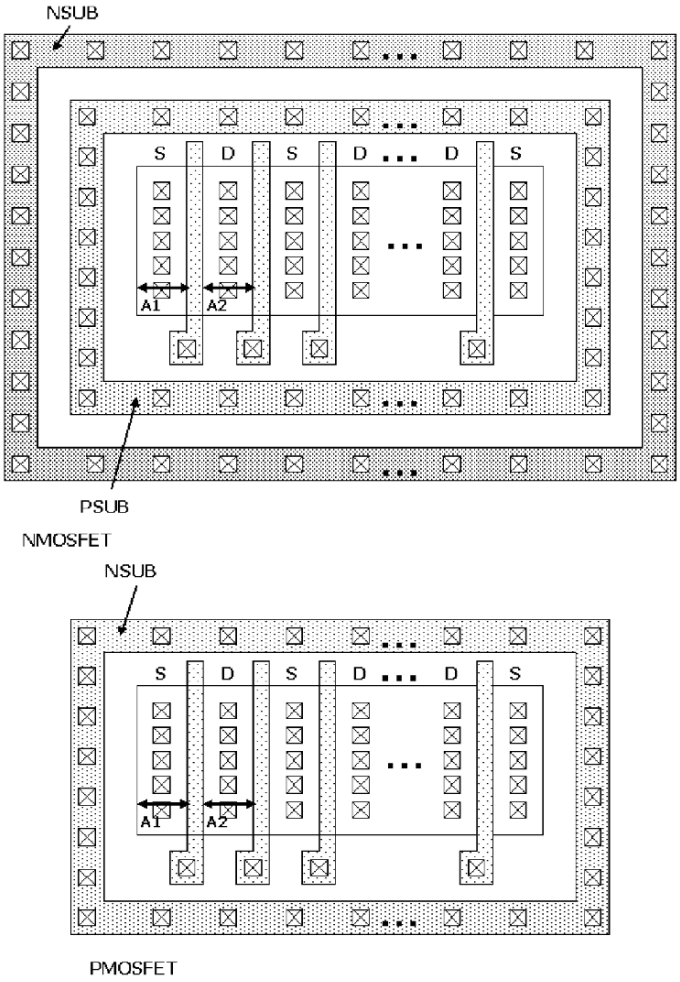

Figure 6. Target plain view of NMOS and PMOS.

gate contact and that between center of gate and substrate contact, are also the same in each fingers. Hence, the finger structure MOSFET was divided into intrinsic unit transistors for simple calculation.

3.1.1. Area and perimeter of source/drain diffusion

The source/drain diffusion of multi-finger MOSFET is common with that of the next transistor as shown in Figure 6. Thus, the number of source/drain diffusions is almost halved in this structure compared to that in a one-finger transistor. The calculated value of numbers of source/drain diffusions is shown

in Table 1, where M_s is number of source diffusion, M_d is number of drain diffusion, and M_g is number of gate fingers. In the case of an even number of gate multiples, it is possible to treat two structures of source/drain diffusion order, SDS or DSD, and the number of source/drain diffusions is different in each case. One case of the edge diffusion is source (SDS), and the other case of the edge diffusion is drain (DSD). On the other hand in the case of an odd number of gate fingers, the number of source diffusions and that of drain diffusions are the same.

The calculated equations of the area and perimeter of source/drain diffusion are shown in Table 2.

3.1.2. Gate resistance

Gate resistance, R_g, is expressed as Eq. (2).

$$R_g = R_{sg} \times \frac{(W_f + X_0)}{3 \times L_g \times M_g} + \frac{R_{cg}}{M_{cg}} \times \frac{1}{M_g} \tag{2}$$

where R_{sg} is sheet resistance of gate polysilicon, R_{cg} is contact resistance of gate polysilicon, M_{cg} is number of gate polysilicon, W_f is gate finger width, and X_o is distance between active area edge and gate polysilicon contact as shown in Figure 7 for the NMOS case. Although the layout for PMOS is not indicated here, it is almost the same as Figure 7.

3.1.3. Back gate resistance

The back gate resistance, R_n (for PMOS) and R_p (for NMOS), is dependent on length of current flow, and its length is similar to the distance between

Table 1. Number of source and drain diffusions.

# of Gate fingers	Types	M_s	M_d
EVEN	SDS	$M_g/2 + 1$	$M_g/2$
	DSD	$M_g/2$	$M_g/2 + 1$
ODD	—	$(M_g + 1)/2$	$(M_g + 1)/2$

Table 2. Area and perimeter of source and drain diffusions.

# of Gate fingers	Types	AS	PS	AD	PD
EVEN	SDS	$(M_g/2 - 1)A_2W_f + 2A_1W_f$	$(M_g - 2)(A_2 + W_f) + 4(A_1 + W_f)$	$M_gA_2W_f/2$	$M_g(A_2 + W_f)/2$
	DSD	$M_gA_2W_f/2$	$M_g(A_2 + W_f)/2$	$(M_g/2 - 1)A_2W_f + 2A_1W_f$	$(M_g - 2)(A_2 + W_f) + 4(A_1 + W_f)$
ODD	—	$(M_g - 1)A_2W_f/2 + A_1W_f$	$2(M_g - 1)(A_2 + W_f) + 2(A_1 + W_f)$	$(M_g - 1)A_2W_f/2 + A_1W_f$	$2(M_g - 1)(A_2 + W_f) + 2(A_1 + W_f)$

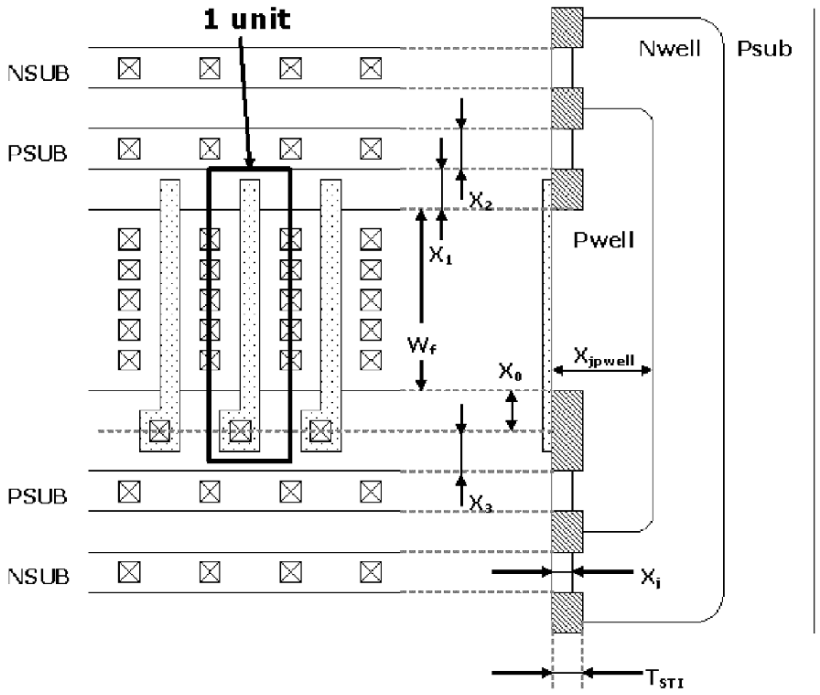

Figure 7. Details of layout view and cross section view of NMOSFET.

transistor active area and substrate contacts. To obtain accurate values of resistance, it is necessary to consider details of device structure as shown in Figure 7. Total resistance can be expressed as Eqs. (3) and (4) for NMOS and PMOS.

$$R_p = R_{spw} \times \frac{X_{\text{jpwell}}}{M_g} \times \left(\frac{X_{\text{jpwell}} + T_{\text{STI}}}{2W_f L_g} + \frac{\frac{W_f}{2} + X_1 + \frac{X_2}{2}}{(X_{\text{jpwell}} - T_{\text{STI}})^2} + \frac{X_{\text{jpwell}} - X_j}{2X_2^2} \right) \tag{3}$$

$$R_n = R_{snw} \times \frac{X_{\text{jnwell}}}{M_g} \times \left(\frac{X_{\text{jnwell}} + T_{\text{STI}}}{2W_f L_g} + \frac{\frac{W_f}{2} + X_1 + \frac{X_2}{2}}{(X_{\text{jnwell}} - T_{\text{STI}})^2} + \frac{X_{\text{jnwell}} - X_j}{2X_2^2} \right) \tag{4}$$

where $R_{spw}, R_{snw}, X_{\text{jpwell}}, X_{\text{jnwell}}, T_{\text{STI}}, X_1, X_2, X_j$ are sheet resistance of p-well, that of n-well, junction depth of p-well, that of n-well, thickness of STI, distance between gate and well contact, width of well contact, and junction depth of well contact, respectively. The first term of Eqs. (3) and (4) is resistance

of gate surface to half depth of well, the second term is resistance of gate to well contact, and the third term is resistance of half depth of well to well contact metal.

3.1.4. Well/Substrate resistance underlying source/drain diffusion

The well resistance or substrate resistance, which is underlying source/drain junction, R_{sjsub}/R_{djsub} is expressed as Eq. (5) for NMOS source, (6) for NMOS drain, (7) for PMOS source, and (8) for PMOS drain. The equation consists of components similar to those of back gate resistance.

$$R_{sjsub} = R_{spw} \times \frac{X_{\text{jpwell}}}{M_s} \times \left(\frac{X_{\text{jpwell}} - X_j}{2W_f L_{sd}} + \frac{\frac{W_f}{2} + X_1 + \frac{X_2}{2}}{(X_{\text{jpwell}} - T_{\text{STI}})^2} + \frac{X_{\text{jpwell}} - X_j}{2X_2^2} \right) \tag{5}$$

$$R_{djsub} = R_{spw} \times \frac{X_{\text{jpwell}}}{M_d} \times \left(\frac{X_{\text{jpwell}} - X_j - W_{dd}}{2W_f L_{dd}} + \frac{\frac{W_f}{2} + X_1 + \frac{X_2}{2}}{(X_{\text{jpwell}} - T_{\text{STI}})^2} + \frac{X_{\text{jpwell}} - X_j}{2X_2^2} \right) \tag{6}$$

$$R_{sjsub} = R_{snw} \times \frac{X_{\text{jnwell}}}{M_s} \times \left(\frac{X_{\text{jnwell}} - X_j}{2W_f L_{sd}} + \frac{\frac{W_f}{2} + X_1 + \frac{X_2}{2}}{(X_{\text{jnwell}} - T_{\text{STI}})^2} + \frac{X_{\text{jnwell}} - X_j}{2X_2^2} \right) \tag{7}$$

$$R_{djsub} = R_{snw} \times \frac{X_{\text{jnwell}}}{M_d} \times \left(\frac{X_{\text{jnwell}} - X_j - W_{dd}}{2W_f L_{dd}} + \frac{\frac{W_f}{2} + X_1 + \frac{X_2}{2}}{(X_{\text{jnwell}} - T_{\text{STI}})^2} + \frac{X_{\text{jnwell}} - X_j}{2X_2^2} \right) \tag{8}$$

where M_s is number of source diffusion and M_d is number of drain diffusion. Also $L_{sd} = A_s/W_f M_s$ is average value of length of source extension, $L_{dd} = A_d/W_f M_d$ is that of drain extension, and W_{dd} is depletion layer width of drain junction. Of course, W_{dd} depends on drain bias, but it is very complicated to calculate its value for each bias point. Therefore, in this work a typical biased depletion layer width was chosen (e.g. $V_{ds} = V_{gs}$).

3.1.5. Well/Substrate resistance underlying gate extension

Well/substrate resistance underlying gate extension, R_{gb}, is expressed as Eqs. (9) and (10). Equation (9) shows NMOS well/substrate resistance

underlying gate extension and Eq. (10) shows that of PMOS. The calculation methodology is also almost the same as that for back gate resistance.

$$R_{gbn} = R_{spw} \times \frac{X_{\text{jpwell}}}{M_g} \times \left(\frac{X_{\text{jpwell}} - X_j}{2A_{gf}} + \frac{X_3 + \frac{X_2}{2}}{(X_{\text{jpwell}} - T_{\text{STI}})^2} + \frac{X_{\text{jpwell}} - X_j}{2X_2^2} \right) \tag{9}$$

$$R_{gbp} = R_{snw} \times \frac{X_{\text{jnwell}}}{M_g} \times \left(\frac{X_{\text{jnwell}} - X_j}{2A_{gf}} + \frac{X_3 + \frac{X_2}{2}}{(X_{\text{jnwell}} - T_{\text{STI}})^2} + \frac{X_{\text{jnwell}} - X_j}{2X_2^2} \right) \tag{10}$$

where X_3 is distance between well/substrate contact and center of gate extension as shown in Figure 7.

3.1.6. Parasitic inductance of each terminal

Parasitic inductance of each terminal (L_s for source, L_d for drain, and L_g for gate) originates from its wire inductance. Thus, number of gate fingers is the dominant factor. The equation originated from a simple estimation of wire inductance [27] and it was optimized for adoption for some empirical results as shown in Eq. (11).

$$L_s = L_d = L_g = 1.2M_g + 18.7[\text{pH}] \tag{11}$$

All parasitic component values were calculated by Eqs. (1) to (11).

3.2. Model Confirmation

The model accuracy was confirmed by comparing between s-parameter measurement results and simulation results. MOSFET's s-parameter was measured by HP-8510 network analyzer with high frequency probe for on-wafer measurement. The parasitic capacitances in the measurement system such as pad parasitic capacitances and wire parasitic capacitances were de-embedded in an appropriate manner. Measured frequency was 0.2 to 20 GHz. Measured bias points of MOSFET were $|V_{ds}| = 1.0$ to 2.5 V, and $|V_{gs}| = 0.8$ to 1.5 V which was equivalently $|V_{th}| + 200$ mV to 900 mV. Measurement samples of MOSFET were 50 μm to 200 μm total gate width with 5 μm gate finger width, and 0.25 μm to 0.5 μm gate lengths. L_{g^-}, W_{g^-}, V_{gs^-}, and V_{ds^-} dependence were measured to compare with simulated data using this model for NMOS.

Figure 8 shows confirmation results of geometry dependence of NMOS, and Figure 9 shows that of bias dependence of NMOS, where (a) for s_{11}, (b) for s_{21}, (c) for s_{12}, and (d) for s_{22}.

Input refractions coefficient, s_{11}, differed little for different gate lengths in both simulation and measurement. Forward gain, s_{21}, shows a good agreement between simulation and measurement. Reverse gain, s_{12}, also shows good agreement between simulation and measurement, but in regions of over 10 GHz agreement is relatively poor. Output refraction coefficient, s_{22}, shows relatively poor agreement but simulated data was acceptable throughout the entire frequency range. These results indicated that this scalable parasitic model is suitable for expressing RF characteristics.

3.3. Parasitic Network Influence on RF Circuit

The influence of parasitic network on the accuracy of RF circuit simulation was confirmed. In the case of LNA, parasitic network influence on the noise figure is basically clear since the increases in noise of MOSFET results in a corresponding increase in the noise figure.

On the other hand, in the case of voltage-controlled oscillator (VCO), the parasitic network influence on the phase noise was less direct. The phase noise of VCO is influenced by several sorts of noise, including thermal noise of resonator, flicker noise of MOSFET, and also thermal noise of parasitic components of MOSFET. In this section, the phase noise differences among simulation results with substrate network, that without substrate network and measurement results are compared.

The phase noise of voltage-controlled oscillator is expressed as Eq. (12) [28].

$$L(\omega_m) = \frac{kT \cdot R_{\text{eff}}(1 + F_{GC})}{\frac{V_{\text{osc}}^2}{2}} \left(1 + \frac{\omega_{\text{osc}}}{\omega_m}\right)^2 \tag{12}$$

where, $L(\omega_m)$ is phase noise at certain hertz offset frequency ω_m from carrier, V_{osc} is oscillation amplitude of VCO, ω_{osc} is oscillation frequency, and F is noise parameter. Although the definitions of almost all the parameters in this equation are clear, a part of F is still unclear. In ideal VCO, F_{GC} consists of the resonator noise source and the gain-cell noise source.

Noise sources of resonator are fundamental phase noise contents of integrated VCO, and several papers have reported on them [27–29]. The effective resistance of resonator is expressed as Eq. (13).

$$R_{\text{eff}} = R_l + R_{vc} + \frac{1}{R_p(\omega_{\text{osc}} C_{\text{tot}})^2} \tag{13}$$

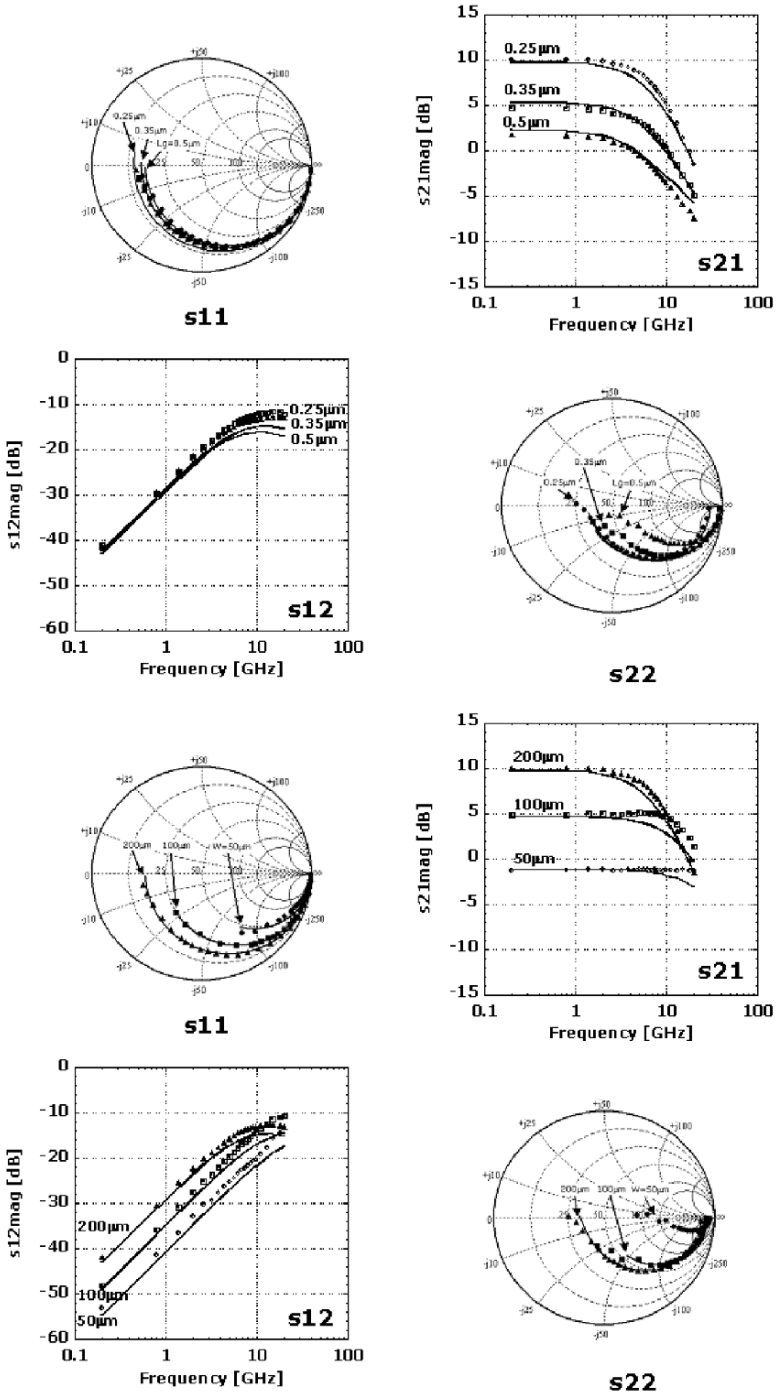

Figure 8. Measurement result and simulated one as a function of L_g and W_g.

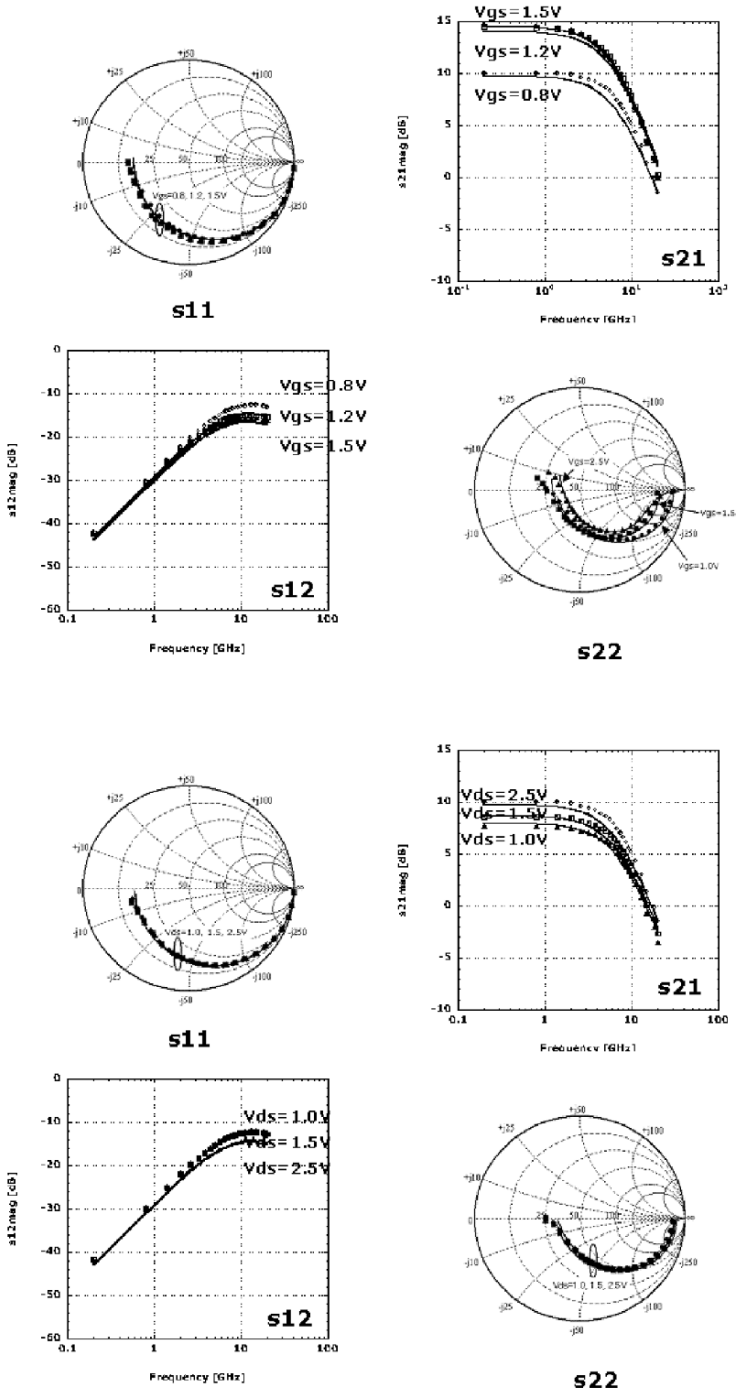

Figure 9. Measurement result and simulated one as a function of DC-bias.

where, R_l is parasitic resistance of inductor, R_{cv} is parasitic resistance of varactor, R_p is parallel resistance of resonator, and C_{tot} is total capacitance of resonator including varactor capacitance and any parasitic capacitance, where, G_m of MOS-VCO gain-cell and noise equation of MOS gain-cell is expressed as Eq. (15).

$$\overline{di}^2_{M,d} = 4kT\left(\sum \gamma g_{d0} + \sum R_i g_{d0}^2\right)\Delta f \tag{15}$$

This section focuses on parasitic resistance, hence right hand of Eq. (15) is significant. The correct noise contribution factor of MOS-VCO gain-cell from the viewpoint of parasitic resistance is expressed as Eq. (16).

$$\alpha_{\text{Noise}} = \sum R_i g_{d0} \tag{16}$$

The total noise equation of phase noise of MOS-VCO is rewritten as Eq. (17).

$$L(\omega_m) = \frac{kT \cdot R_{\text{eff}}(1 + \sum R_i g_{d0})}{\frac{V_{\text{osc}}^2}{2}}\left(1 + \frac{\omega_{\text{osc}}}{\omega_m}\right)^2 \tag{17}$$

Phase noise was calculated using Eqs. (11), (13), and (15). Figure 10 shows simulation results of MOS-VCO phase noise at 3 MHz offset from carrier with

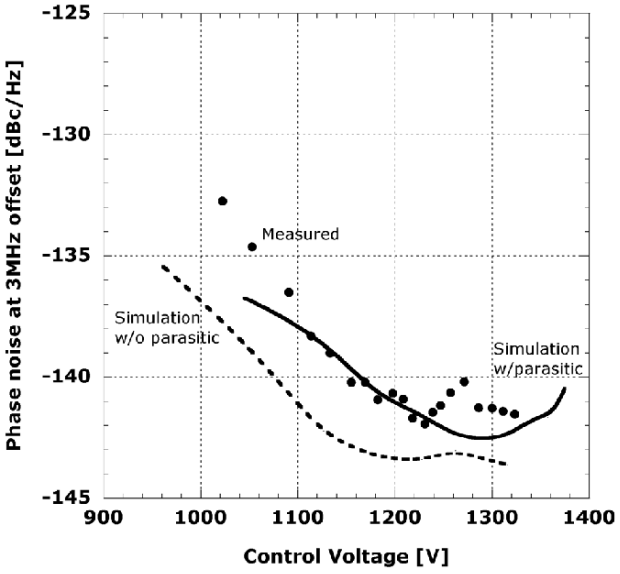

Figure 10. The difference of phase noise among measured, simulated with parasitic, and simulated without parasitic.

parasitic network model and that without parasitic network model, and measurement data. Measurement data shows good agreement with simulation data with parasitic network. On the other hand, simulation data without parasitic network shows disagreement with measurement data. The importance of the parasitic network is clarified.

3.4. Summary

The parasitic components model is very important for RF circuit design and its influence is significant as shown in this section, not only for small signal parameter accuracy but also for large signal circuit such as VCO. Introduction of a scalable parasitic model will be necessary for modern circuit design.

4. Channel Noise

4.1. Channel Noise of Small Geometry MOSFET

A simplified MOSFET equivalent circuit with noise sources is shown in Figure 11.

Noise sources of MOSFET consist of gate resistance noise, source resistance noise, drain resistance noise, flicker noise, body resistance noise, and channel thermal noise. The five noises other than channel thermal noise can be expressed

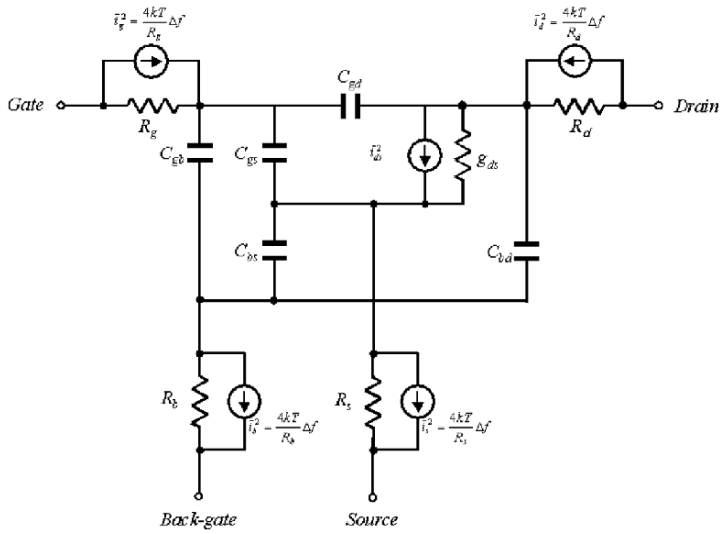

Figure 11. Noise equivalent circuit of MOSFET.

as the following equations.

$$\bar{i}_g^2 = \frac{4kT}{R_g}\Delta f \tag{18}$$

$$\bar{i}_s^2 = \frac{4kT}{R_s}\Delta f \tag{19}$$

$$\bar{i}_d^2 = \frac{4kT}{R_d}\Delta f \tag{20}$$

$$\bar{i}_{1/f}^2 = \frac{K_F I_{ds}^{A_F}}{f \cdot C_{OX} \cdot W_g \cdot L_g}\Delta f \tag{21}$$

$$\bar{i}_b^2 = \frac{4kT}{R_b}\Delta f \tag{22}$$

where, k is Boltzman's constant, T is absolute temperature, R_g is gate resistance, R_s is source resistance, R_d is drain resistance, K_F is flicker noise coefficient, A_F is noise exponential coefficient, C_{ox} is gate insulator capacitance, W_g is gate width, L_g is gate length, and R_b is total body resistance.

The channel thermal noise of recent small geometry MOSET consists of two regions as shown in Figure 12. One is gradual electron velocity region and the other is velocity saturation region. Both regions are divided at pinch-off point. Channel length of gradual electron velocity region is L_{elec} and that of velocity saturation region is ΔL in Figure 12. An applied drain to source voltage of gradual electron velocity region is $V_{d\text{sat}}$ in total drain to source voltage, V_{ds}.

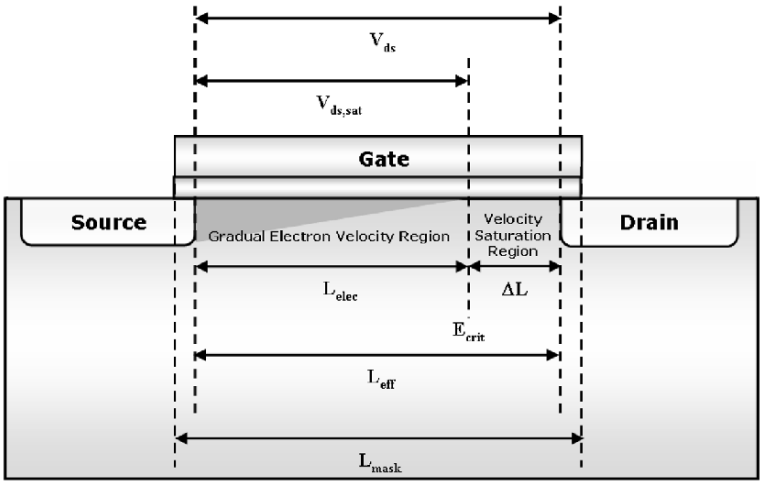

Figure 12. Cross-section view of MOSFET.

The channel thermal noise of gradual electron velocity region can be expressed as Eq. (23) [30].

$$\overline{i_{ch}^2} = 4kT\left[\gamma\frac{W_g}{L_g}\mu C_{OX}\left(V_{gs} - V_{th}\right)\right] = 4kT\gamma g_{d0}$$
$$\gamma = \frac{2}{3}\times\frac{1+\eta+\eta^2}{1+\eta} \tag{23}$$

where γ is channel thermal noise coefficient, μ is mobility of carrier, V_{gs} is gate to source voltage, V_{th} is threshold voltage of MOSFET, η is parameter of noise, and g_{d0} is zero biased drain to source conductance. When MOSFET works in linear region, η is unity and when MOSFET works in saturation region, η is zero. Hence γ is 1 and 2/3 in the case of linear region and saturation region of MOSFET, respectively. This channel thermal noise coefficient is the same as the classical one.

The channel thermal noise in velocity saturation region can be expressed as Eq. (24) [9].

$$\overline{i_{ch,vs}^2} = \delta\frac{4kT}{L_g^2}\cdot\frac{I_{ds}}{E_{\text{crit}}}\frac{1}{\alpha}\sinh\left(\alpha\Delta L\right) \tag{24}$$

where ΔL is channel length of velocity saturation region as shown in Eq. (25), E_{crit} is critical electric field along channel, and δ is a fitting parameter. The channel thermal noise of this region is defined by hot electron regime.

$$\Delta L = \frac{1}{\alpha}\ln\left[\frac{\alpha\left(V_{ds} - V_{d\text{sat}}\right) + E_D}{E_{\text{crit}}}\right] \tag{25}$$

$$E_D = E_{\text{crit}}\sqrt{1+\left[\frac{\alpha\left(V_{ds} - V_{d\text{sat}}\right)}{E_{\text{crit}}}\right]^2} \tag{26}$$

$$\alpha = \lambda\sqrt{\frac{3}{2}\cdot\frac{C_{OX}}{x_j\cdot\varepsilon_{Si}\cdot\varepsilon_0}} \tag{27}$$

where x_j is the junction depth of source/drain and λ is a fitting parameter of channel length modulation. To define enhancement of the channel thermal noise due to scaling, we measured MOSFET's noise and determined channel thermal noise with different gate length [31].

4.2. Channel Noise Measurement and Characterization

The noise figure of device was measured at frequencies of 1 to 6 GHz. The measurement configuration is shown in Figure 13. The device was measured

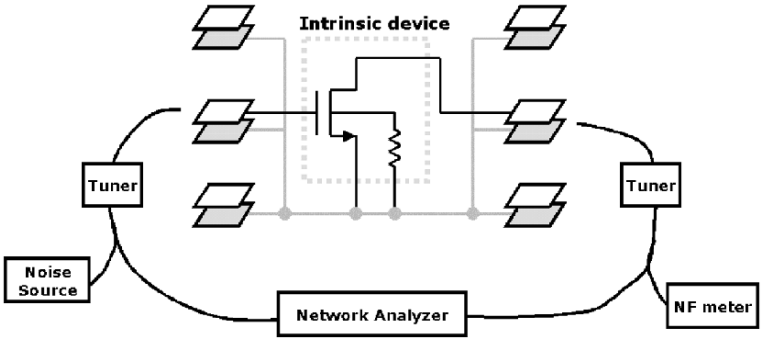

Figure 13. Set-up configuration for on-wafer RF measurement.

by common source and input and output terminals were connected to shielded GSG pads which can eliminate body noise. The parasitic capacitance, parasitic inductance and parasitic resistance were de-embedded by replica pads and wired measurement pattern. The input and output impedances were measured by vector network analyzer (NWA) and tuned by tuner of respective terminals. The noise was measured by NF meter.

Measured geometry of NMOS, L_g/W_g, were 40 nm/100 μm, 60 nm/100 μm, and 70 nm/100 μm with 90 nm process, 110 nm/100 μm with 130 nm process, and 140 nm/100 μm with 180 nm process. The gate width of each MOSFET consisted of 20 × 5 μm finger structure. This means gate width of MOSFET was very large, and therefore, parasitic resistance of source terminal and parasitic resistance of drain terminal can be negligible. Measurement conditions were $V_{ds} = 1$ V and several V_{gs}.

The $NF_{\min}$ was carried out by equivalent noise circle in smith chart. The data were determined by measurement data of several input and output matching conditions. Measured $NF_{\min}$ is dependent on drain current as shown in Figure 14. Due to scaling down of MOSFET gate length, $NF_{\min}$ decreased by 70 nm. However, $NF_{\min}$ did not improve below 70 nm gate length. It is thought that MOSFET noise originating from either gate resistance or channel resistance increases due to scaling down.

In order to extract channel thermal noise, we measured 50 Ω termination noise figures, NF50. The frequency response of NF50 is shown in Figure 15. Generally, noise figure of MOSFET shows frequency response. In the case of low frequency, the noise increases due to influence of flicker noise. On the other hand, in the case of high frequency, the noise increases, too, as a result of gain degradation due to high frequency. In order to obtain channel thermal noise correctly, it is necessary to use mid-frequency range. In Figure 15, in the frequency range above 4 GHz, NF50 increases for almost all MOSFETs regardless

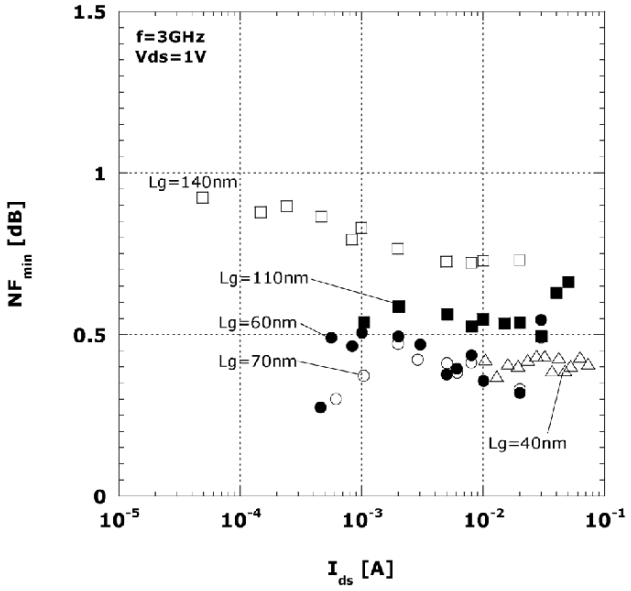

Figure 14. Drain current dependence on measured $NF_{\min}$.

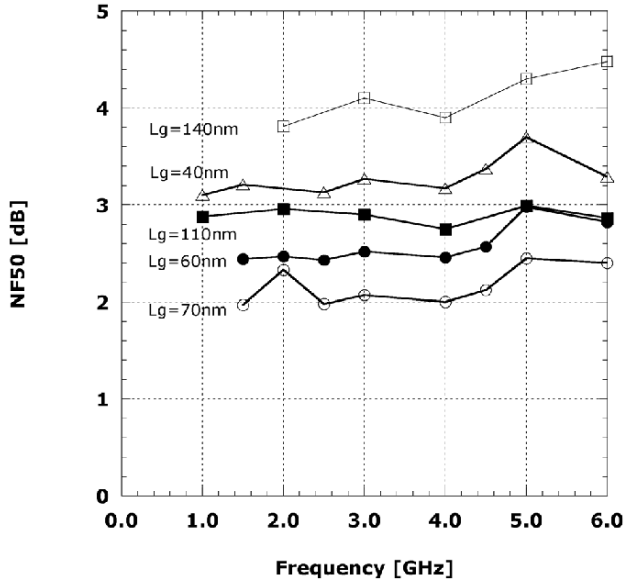

Figure 15. The operating frequency dependence on NF50.

of gate length. It was supposed that there were two reasons for these phenomena. One was MOSFET's gain degradation due to high frequency operation and another was measurement instability. Therefore, frequency range of 1 to 4 GHz was chosen to extract channel thermal noise to obtain correct channel noise performance.

Measured NF50 data for this frequency range indicated the virtual elimination of body resistance noise, source resistance noise, drain resistance noise, and flicker noise. Hence it only contains channel thermal noise and gate resistance noise. The gate resistance can be calculated by Eq. (2). The channel thermal noise was extracted by subtracting gate resistance noise from total noise which carried out NF50. The extracted channel thermal noise as a function of gate overdrive voltage, V_{gs}-V_{th}, is shown in Figure 16.

The channel thermal noise was approximately $3.0 \times 10^{-21}, 2.5 \times 10^{-21}, 2.2 \times 10^{-21}, 1.8 \times 10^{-21}, 1.6 \times 10^{-21}$, for 40 nm, 60 nm, 70 nm, 110 nm, and 140 nm gate length MOSFET at 0.3 V gate overdrive voltage. Indeed, the results indicate the channel thermal noise increased due to scaling down, and the channel thermal noise of 40 nm gate length NMOS was over two times larger than that of 140 nm gate length.

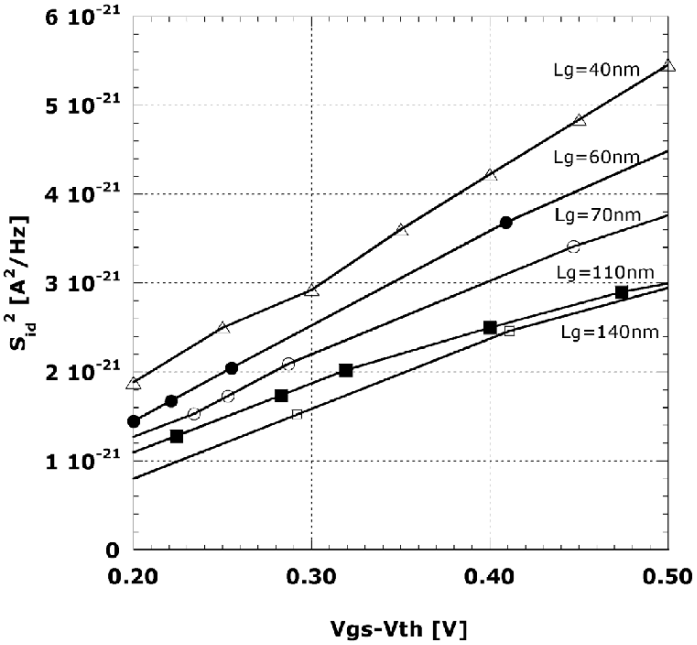

Figure 16. Gate overdrive dependence of noise current.

The total channel thermal noise in saturation region can be express as Eq. (28) using Eqs. (23) and (24).

$$\begin{aligned}\overline{i_{ch,vs}^2} &= 4kT\gamma g_{d0} + \delta\frac{4kT}{L_g^2}\cdot\frac{I_{ds}}{E_{\text{crit}}}\frac{1}{\alpha}\sinh(\alpha\Delta L)\\ &= 4kTg_{d0}\left(\gamma + \delta\frac{4kT}{L_g^2}\cdot\frac{I_{ds}}{E_{\text{crit}}}\frac{1}{\alpha}\sinh(\alpha\Delta L)\frac{1}{g_{d0}}\right)\\ &= 4kTg_{d0}\gamma_{em}\end{aligned} \tag{28}$$

where, γ_{em} is empirical notation of noise coefficient, which covers from long channel to sub 0.1 μm channel. γ_{em} can be rewritten as Eq. (29).

$$\gamma_{em} = \frac{2}{3} + \delta\frac{I_{ds}}{L_g^2\cdot E_{\text{crit}}\cdot\alpha}\sinh(\alpha\Delta L)\frac{1}{g_{do}} \tag{29}$$

The first term of Eq. (28) indicates classical channel thermal noise in [30] and the second term indicates empirical equation similar to [10]. The measured data and calculated results were compared at around $g_{m,\max}$ point for each NMOS. The calculation results of γ_{em} by Eq. (29), measured data of this work, and some published data with similar bias condition are shown in Figure 17. Figure 17 shows quite good agreement from few μm gate lengths to sub 0.1 μm gate length. The calculated channel thermal noise coefficient, γ, were 3.5, 2.2,

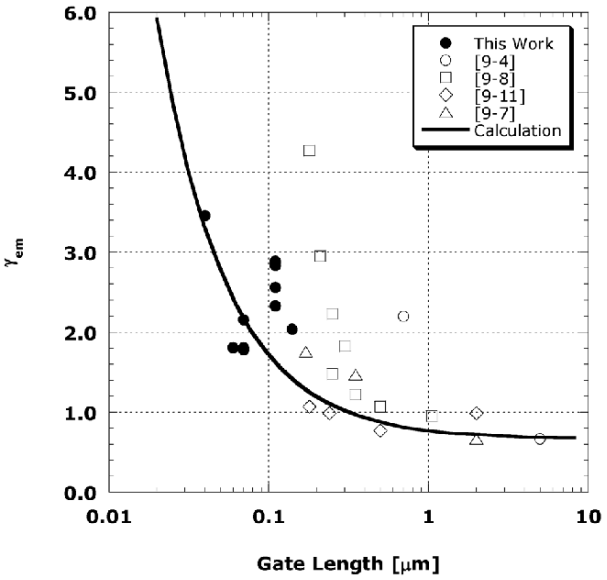

Figure 17. Channel thermal noise coefficient, γ, as a function of gate length of this work and published data. The solid line was calculated by Eq. (29).

2.0, 1.6, and 1.5 for 40 nm, 60 nm, 70 nm, 110 nm, and 140 nm gate length NMOS, respectively. The γ of 40 nm gate length NMOS was approximately five times larger than that of long channel NMOS. The calculation curve almost fit the measurement data of this work and also almost fit the published data. In this fitting curve, fitting parameters were set as $\delta \sim 10$ for Eq. (28) and $\lambda = 0.65$ to 0.95 for Eq. (27).

4.3. Influence for Phase Noise Calculation of VCO

Phase noise of integrated VCO without flicker noise contribution is expressed as Eq. (12) and noise equation of MOS gain-cell is expressed as Eq. (15).

Therefore, correct noise contribution factor of MOS-VCO gain-cell is expressed as Eq. (30) [29].

$$F_{GC} = \alpha_{\text{Noise}} A = \gamma A \tag{30}$$

The total noise equation of phase noise of MOS-VCO is rewritten as Eq. (31).

$$L(\omega_m) = \frac{kT \cdot R_{\text{eff}}(1 + \gamma A)}{\frac{V_{\text{osc}}^2}{2}} \left(1 + \frac{\omega_{\text{osc}}}{\omega_m}\right)^2 \tag{31}$$

To confirm the calculation accuracy of Eq. (12), Figure 18 shows a comparison of calculation results obtained by Eq. (13) and measured phase noise data of several VCOs using 0.25 μm to 0.5 μm gate lengths MOSFET. Compared offset frequency from carrier was 1 MHz and compared control voltage was over 1.0 V to avoid any other component influences such as flicker noise contribution and current noise contribution from current source in this work. The closed circle in Figure 18 indicates calculation using optimum γ value which was extracted by Eq. (13) and the open circle indicates calculation using constant γ as 2/3. Indeed, this figure shows the optimum γ is in better agreement with measured data than is the constant γ value of 2/3. The accuracy using optimum γ for analytical expression of VCO was within $\pm 2\,dB$ on average but that using constant γ was over $\pm 2\,dB$.

4.4. Summary

The channel thermal noise coefficient, γ, was extracted by a high frequency measurement method. It was correctly extracted, eliminating any other noise sources such as source resistance, drain resistance, flicker noise, body resistance, and gate resistance. Indeed, in the case of small gate length MOSFET,

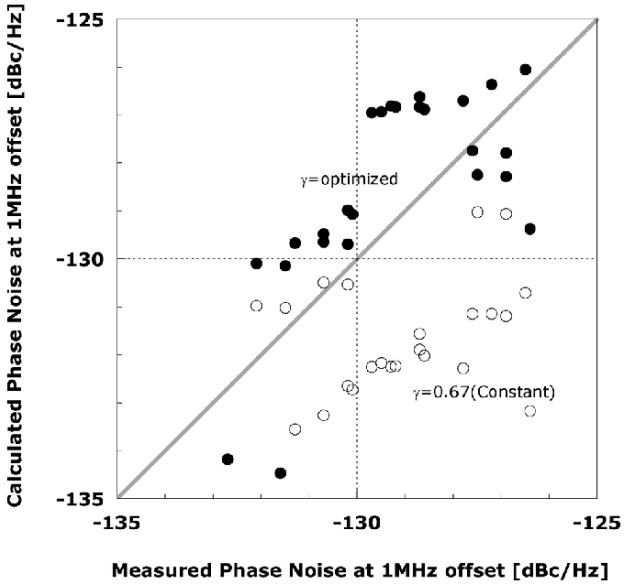

Figure 18. Comparison of measure phase noise and calculated phase noise of several fully integrated MOS-VCO with optimum γ and constant γ as 2/3. Phase noise was measured and calculated at 1 MHz offset from carrier.

γ increased due to hot carrier effect. It was approximately five times larger than classical noise coefficient value, 2/3, in the case of 40 nm MOSFET. The empirical equation of channel thermal noise was in quite good agreement with measured data.

The noise coefficient enhancement influences RF circuit performance. In this work, the influence of increased phase noise of MOS-VCO was confirmed using analytical expression of VCO phase noise. The calculation accuracy using the analytical expression of phase noise of VCO and empirical noise equation of MOS-VCO was within $\pm 2\,dB$.

5. Conclusion

In this chapter, some parameters not covered by a compact model, such as STI stress, scalable parasitic components model and channel thermal noise enhancement due to scaling were described with some circuit performances.

At least, these three issues should be solved by achieving accuracy of these models, which will shrink both the cost and design period for complicated RF circuit design.

Acknowledgement

The author is grateful to Dr. S. Yoshitomi, Mr. T. Ohguro and Mr. K. Kojima of Semiconductor Company, Toshiba Corporation, for fruitful discussion regarding this work. He also wishes to thank Mr. S. Watanabe and Mr. H. Aoki of Semiconductor Company, Toshiba Corporation, for support throughout this work.

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