Chapter 5

EMPIRICAL FET MODELS

Iltcho Angelov
U. Chalmers
E-mail: iltcho.angelov@mc2.chalmers.se

Abstract: This chapter will cover basics of the Empirical FET Models Implementation in CAD tools. First basic experimental characteristics at DC, like I_{ds} and I_{gs} bias dependence will be discussed. Experimental S-parameter, capacitance and high frequency, thermal, power and dispersion characteristics will be shown. They will be linked with the Small and Large Signal Equivalent circuit of the FET. Examples will be given with some basic FET models as they are implemented in CAD tools. It will also be shown how empirical models can be extended to incorporate physical phenomena like thermal effects and dispersion. Finally, models for MOSFET devices will be highlighted.

Key words: FET Modeling; HEMT Modeling.

1. Introduction

The RF performance of FET devices has been dramatically improved in recent years. Today, state of the art FET technology offers very high frequency of operation with high output power. A significant amount of work has been done in the field of high frequency FET transistor modelling and parameter extraction [1–64]. As the output power and operating frequency increase, we face the problem of how to model the high frequency and high power limitations in FET performance and how to implement this in software packages.

Physical modelling approach is very important to optimizing the device structure and to tailor the transistor characteristics for specific application. Nowadays, physical simulators are much faster and more accurate. In the future they will become fast enough to be used in directly for circuit design and

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better integrated in the microwave designers software tools. When the device is finally available from the processing lab quite often characteristics are different from the simulated. In addition, there are always processing tolerances even when a good and stable process is used. These tolerances can influence the accuracy of all simulations including the accuracy of prediction of the output power, but mainly the accuracy of harmonics and inter-modulation simulations. A problem with physical simulators is that they need detailed data for the material and wafer structure and manufacturing details, which are not always available from the foundries. That is why it is common practice to work with the measured device characteristics. When using experimentally measured device characteristics to extract model, there are two approaches:

2. Equivalent Circuit Approach: Evolution

Direct measurement based approach for modelling FET devices was put on track by D. Root and co-authors [17–20]. Later this approach was refined by number of researchers [56–62]. Nowadays this approach is implemented and used in the software packages. The extracted model is very accurate and provides good description of device characteristics. A problem with this approach is that the model is difficult to extend beyond the regions of measured operating voltages and frequencies. The mounting environment should be kept as in the measurements. When device (or environment) is changed, a complete set of measurements should be done and the model should be extracted again.

Years ago, modelling of semiconductor devices was started using equivalent circuit approach. The explanation is simple- software design tools started from analyzing simple lumped element circuits. When computing power and knowledge were available, it was possible to assemble simple small signal device models in the CAD tools. Figure 1 shows such a simple FET equivalent circuit. The model is a set of lumped passive components – resistors, capacitors and inductances. Their placement and values should correspond to the device physics and geometry parameters of the device. The output current source with

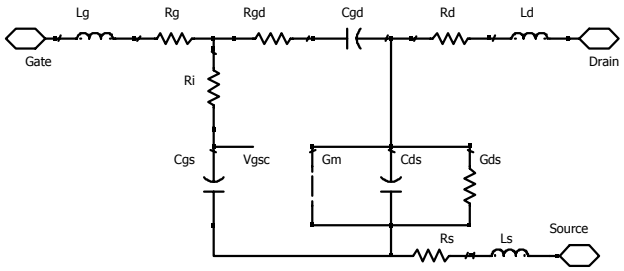


Figure 1. Small Signal Equivalent Circuit of a FET.

transconductance g_m is controlled by the voltage V_{gsc} on the input capacitor C_{gs}. The equivalent circuit approach gives a possibility to extend the model prediction well above the measurements range and when some parameter is changed it is easy to tune the model.

Approximately at the same time several very good works on the small signal FET model and extraction appeared and their extraction procedure to find parameters of the equivalent circuit (EC) is in wide use today [14–16]. This is, because their EC approach is based on the device physics, it is simple and easy to understand and very accurate. For good quality FET, the small signal (SS) model extracted in this way is accurate within 2–5% with the measurements. The extraction is rather simple and when the data are organized in a proper way, the extraction can be done automatically even using directly the software tool:

$$\begin{aligned}\left[Y^i\right] &= \begin{bmatrix} Y^i_{11} & Y^i_{12} \\ Y^i_{21} & Y^i_{22} \end{bmatrix} \\ &= \begin{bmatrix} \dfrac{jC_{gs}\omega}{1+jR_iC_{gs}\omega} + \dfrac{jC_{gd}\omega}{1+jR_{gd}C_{gd}\omega} & -\dfrac{jC_{gd}\omega}{1+jR_{gd}C_{gd}\omega} \\ \dfrac{g_m e^{-j\omega\tau}}{1+jR_iC_{gs}\omega} - \dfrac{jC_{gd}\omega}{1+jR_{gd}C_{gd}\omega} & g_d + jC_{ds}\omega + \dfrac{jC_{gd}\omega}{1+jR_{gd}C_{gd}\omega} \end{bmatrix}\end{aligned} \tag{1}$$

$$\begin{aligned} C_{gs} &= \frac{1}{\omega} \times \mathrm{Im}\left(\frac{1}{\left(Y^i_{11}+Y^i_{12}\right)}\right)^{-1} & C_{gd} &= -\frac{\mathrm{Im}\left(Y^i_{12}\right)}{\omega} \times \left[1+\left(\frac{\mathrm{Re}\left(Y^i_{12}\right)}{\mathrm{Im}\left(Y^i_{12}\right)}\right)^2\right] \\ R_i &= \mathrm{Re}\left(\frac{1}{Y^i_{11}+Y^i_{12}}\right) & R_{gd} &= -\frac{\mathrm{Re}\left(Y^i_{12}\right)}{\mathrm{Im}\left(Y^i_{12}\right)} \times \left[1+\left(\frac{\mathrm{Re}\left(Y^i_{12}\right)}{\mathrm{Im}\left(Y^i_{12}\right)}\right)^2\right]^{-1} \\ g_m &= \left|\left(\frac{Y^i_{21}-Y^i_{12}}{Y^i_{11}+Y^i_{12}}\right)\right| \times \mathrm{Im}\left(\frac{1}{Y^i_{11}+Y^i_{12}}\right)^{-1} & \tau &= -\frac{1}{\omega} \times \left[\arg\left(\frac{Y^i_{21}-Y^i_{12}}{Y^i_{22}+Y^i_{12}}\right) + \frac{\pi}{2}\right] \\ g_d &= \mathrm{Re}\left(Y^i_{22}\right) + \mathrm{Re}\left(Y^i_{12}\right) & C_{ds} &= \frac{1}{\omega} \times \mathrm{Im}\left(Y^i_{22} + Y^i_{12}\right) \end{aligned} \tag{2}$$

When the small signal model and extraction were established and implemented in the CAD tools, the next step was to integrate the small signal equivalent circuit model into the large signal model (LS). Many of the elements of the equivalent circuit are bias dependent and the extended, LS equivalent circuit approach was the simplest way to increase the complexity of the device models. With LS model is possible to include these bias dependencies of nonlinear elements. This provides a possibility to do accurately more complicated tasks like designing nonlinear circuits such as power amplifiers, mixers, oscillators multipliers etc. First, IV characteristics were added to the simulated parameters

and the Small Signal S-parameters were generated directly from the LS equivalent circuit. It is natural to expect that S-parameters generated from the LS FET model with small input power should be equal to the S-parameters generated from the SS equivalent circuit.

3. Current Models

3.1. I_{ds} Current

Extracting the current part of the model is very important part of creating the FET large signal model. Before starting any detailed measurements and modeling it is good to evaluate the quality (functionality) of the selected transistor. It is important to measure or compensate the cable and DC line losses before any extraction starts, especially with currents above 0.1 A. The reason is that, it is impossible to distinguish the influence of external resistances on the IV from the influence of intrinsic device resistances. This problem is common for every kind of device – FET or HBT, that is why, the resistances of the measurement setup should be evaluated carefully before any model extraction is started.

The drain current is measured in wide range of biases sweeping both V_{gs} and V_{ds} as Figure 2. Typically we will need at least 10 gate voltages and 5 to 10 drain voltages depending on the voltage and power range of the transistor. When measurements and extraction are done properly, we can expect that at low frequency, where the contribution from reactive components (capacitance and inductances) is small, the model will be correct. In case low-frequency dispersion phenomena are present in the device, an extended model is required (see Section 6.2). Figure 2a shows typical dependencies of $I_{ds}, G_m\, f\,(V_{gs}, V_{ds})$ for GaAs FET. Figure 2b shows typical g_m dependence vs. V_{gs} for V_{ds} above

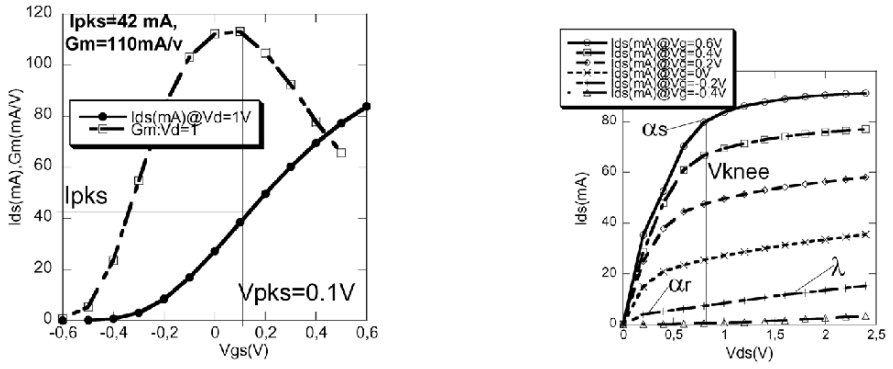


Figure 2. (a) I_{ds}, G_m vs. V_{gs}, (b) I_{ds}, vs. V_{ds}, FET $W = 200\,\mu$m.

knee voltage. The gate voltage V_{pks}, g_m and the drain current I_{pks} at which the maximum transconductance occurs can be used to link measured and modeled I_{ds}. Typically, this inflection point occurs at the gate voltage for which we have the half of the channel current I_{pks}.

For drain voltage above the knee voltage V_{knee} and gate voltage $V_{gs} \cong$ 0.6–0.8 V for GaAs FET the drain current will saturate and reach the maximum channel current. This maximum channel current depends on the material structure, doping profile etc. For GaAs FET the maximum channel current is 0.3–0.5 A/mm and for new material structures like GaN the maximum channel current can be as large as 1.6 A/mm.

When we change the drain voltage, there is a change of the gate voltage for which we have maximum of the transconductance V_{pk} as can be seen on Figure 2. At low drain voltage $V_{ds} = 0.2$ V, the peak of G_m is at $V_{gs} = -0.1$ and at high $V_{ds} > V_{\text{knee}}$ the $V_{pk} = 0.1$ V. Above V_{knee} there is some increase of the drain current, due to the channel opening from the drain voltage influence. If the drain voltage is further increased, breakdown can occur. Typically, high power devices are biased for high efficiency operation i.e., at high voltages and low currents. A properly constructed load line will keep the devices away from the breakdown area and they will be switched from high voltage and low current to high currents and low voltages (close to the V_{knee}). If this is the case, there is no sense to spend much time making very detailed and accurate breakdown model. Only if the device will be operated in the breakdown area it worth spending time to make detailed and accurate breakdown model.

Transconductance and the ratio $P_1 = G_m/I_{ds}$ also change when the drain voltage is changed. This means that the models should have a functional dependence for the peak voltage $V_{pk} = f(V_{ds})$, $P_1 = f(V_{ds})$ to describes the changes of V_{pk}, G_m due to drain voltage influence. Figure 3 shows the I_{ds} vs. V_{gs} dependence when the stepping drain voltage V_{ds} from negative to positive.

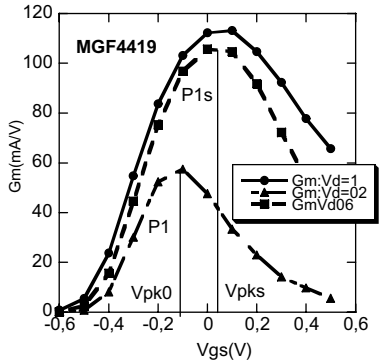


Figure 3. G_m vs. V_{gs} FET 200 μm.

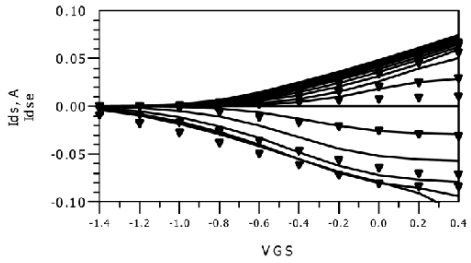


Figure 4. Measured and modeled I_{ds} vs. V_{gs} Symmetrical model.

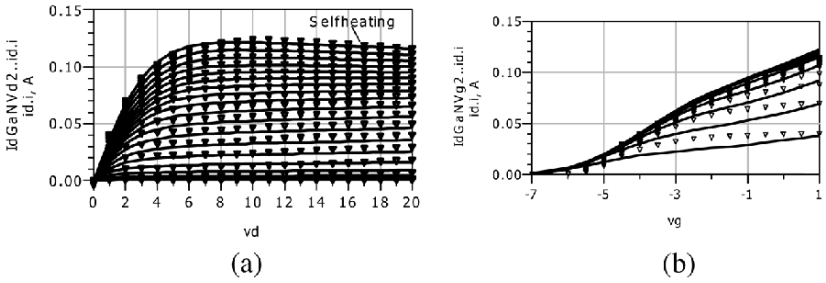


Figure 5. (a) I_{ds} vs. V_{ds} with V_{gs} as a parameter of a GaN FET; (b) I_{ds} vs. V_{gs} with V_{ds} as a parameter of a GaN FET.

As can be seen, the device is not completely symmetrical and this is in part due to the shift of V_{pk} when V_{ds} is negative.

Often due to large device size, highly dissipated power and dispersive effects, the modelled IV characteristics are far from ideal, Figures 4, 5. The self-heating will decrease the drain current at high dissipated power [64]. The decrease of I_{ds} at high dissipated power will critically depend on the thermal resistance R_{therm} and for high power devices it is important to select a proper material with a high thermal conductivity, to make a good thermal design of the transistor – i.e., using properly placed via hols thermal shunts and thin substrate. The technology for the new GaN and SiC devices is very promising, but still not settled and there is substantial activity to improve these devices. We can expect that the IV curves and all parameters for these new, high power devices will gradually become better then for devices with established technology like GaAs.

The basis for the FET operation are two dependencies- the carrier velocity and carrier concentration, Figures 6, 7. Their bias and temperature dependencies will be the main factors which will determine the transistor behavior. The I_{ds} vs. V_{gs} dependence is similar to the carrier concentration dependence vs.

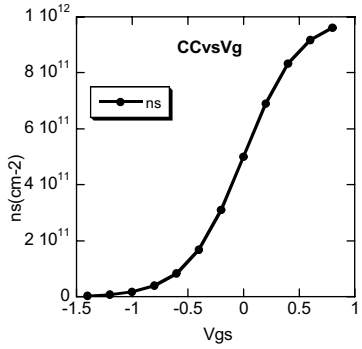


Figure 6. Variation of the 2DEG (ns) sheet densities.

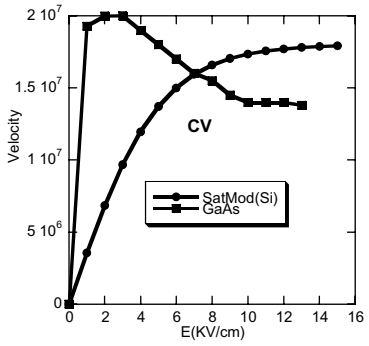


Figure 7. Velocity vs. electric field for GaAs and Si for AlGaAs. GaAs MODFET vs. V_{gs}.

gate voltage, Figure 7 and corresponding modeling function should be selected. Generally, the solution of the Schrödinger and Poisson equation are ***erf*** type of functions, but ***erf*** function is usually not available in circuit simulators. That is why, it can be replaced with other suitable, like ***tanh*** which is accurate enough for this application [7].

In GaAs FET devices at some electric field (V_{ds}, V_{gs}) we observe a maximum of the carrier velocity and transconductance. In Si we have gradual increase of the carrier velocity, which will produce quite different shape of I_{ds}, G_m, G_{ds} as in Figure 8 in comparison with the GaAs Figure 3. The g_m for the Si CMOS device increases with the drain voltage increase and will change shape I_{ds} vs. V_{gs} as well. The different shape of g_m for Si CMOS will produce different harmonic content in comparison with the GaAs FET. This means that in the FET models we should have respective parameters describing these dependences.

There are some general requirements for the selection of the modeling functions in the empirical models. In FET and HBT the device parameters can

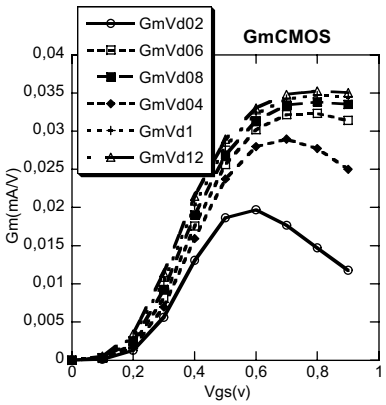


Figure 8. G_m vs. V_{gs} CMOS.

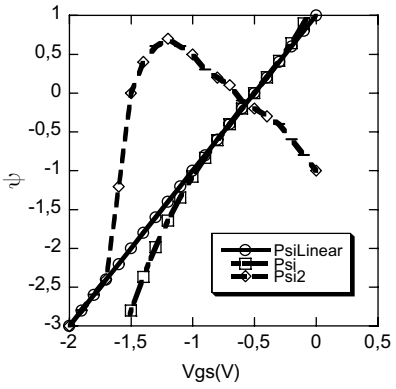


Figure 9. Extracted argument Ψ vs. V_{gs}.

be considered dependent on two voltages $I = f_1(V_{gs}) \cdot f_2(V_{ds})$ or respective V_{be}, V_{ce}. The best solution from extraction and user understanding point of view is to make both parts f_1 and f_2 completely independent – this will greatly simplify extraction. However, when follows from device physics that we have inter-coupling between the $f_1(V_{gs}) \cdot f_2(V_{ds})$ parts, this should be implemented in a proper way. Then, with very small number of additional parameters the model will describe the device behavior accurately. When proposed modeling function is correct and the device is ideal, from the measured data we should obtain a linear function for the extracted argument of f_1 *or* f_2. The derivative will be equal to the measured derivative as in Figure 9. If from the reverse extraction we can get two values of the argument, as this is shown for the *example* function P_{si2} (i.e., we have a $\partial\Psi^2/\partial V_{gs}^2 = 0$) this is an indication that our choice for modeling function is not very good. This is because the selected function

P_{si2} will work in the simulations, but will create problems in the extraction. This is valid also for the sub-functions responsible for the inter-coupling between f_1 and f_2. For example, if the function we guess is $y = Ax^2$ this will work well in the simulation. But obviously there is a problem in the reverse extraction, because the same value of y can be produced by two values of the argument $x = \pm\sqrt{y/A}$.

Often the device is not ideal and we need some flexibility to tune the model. It seems logical that a complex model is more likely to be accurate. This is correct, within limits, because we should always keep in mind that there are processing tolerances and there is no sense making model 1% accurate when process tolerances are 10%. The representation of the Argument as a Power Series (APS) will give a possibility to fit variety of devices. Fitting a polynomial function is rather simple task, but even in this case, parameters of the APS should be selected properly. For example, when we have a negative second term in APS we should always add positive 3-rd term and so on. This will exclude the possibility of a local maximum and dual argument reading and provide required trimming.

3.2. Gate Current

Sometimes we forget that FET devices have gates and ignore that the FET can exhibit significant gate current when driven with high input power. A reason users do not like gate models is that gate current I_{gs} dependence vs. V_{gs} is exponential and this creates problems with the harmonic balance convergence when large number of harmonics is considered. For this reasons the gate current model should be carefully implemented in the software package, properly extracted and used.

In the standard diode equation, $I_{gs} = I_s(\exp(V_{gs}/V_t \cdot N_e) - 1)$, I_s is extracted at $V_{gs} = -\infty$, i.e., at very small currents and very negative V_{gs} for which we do not operate the device. We can change the reference (extracting) point rearranging the diode equation. In the new definition, parameters are taken directly at the typical operating point at high gate current. This can be the knee of I_{gs} vs. V_{gs} characteristics at $V_j = 0.8\,\mathrm{V}$ which is typical GaAs device. The exponent can be limited with some limited function like in Eq. (4b):

$$\begin{aligned} I_{gs} &= I_j(\exp(P_{be}) - \exp(P_{be0})), \\ P_{be} &= P_{be1}((V_{gs} - V_j), P_{be0} = -P_{be1}(V_j), \\ P_{be1} &= q_e/K_b \cdot T_{ambK} \cdot N_{e1} = 1/V_t \cdot N_{e1} \cong 38.695/N_{e1}, \end{aligned} \tag{4a}$$

$$I_{gs} = I_j(\exp(P_{be1}\tanh(V_{gs} - V_j)) - \exp(P_{be1}\tanh(P_{be0}))) \tag{4b}$$

where q_{e^-} is the electron charge, K_{b^-} is the Boltzmann constant, N_{e1} is ideality factor, I_j is measured I_{gs} at V_j [52].

When the transistor is biased as a low noise or small signal amplifier, the gate current is small (well below 1 μA) and can be ignored.

4. Empirical FET Models: Evolution

4.1. Curtice Quadratic Model [11, 52–54]

4.1.1. Standard model

One of the first MESFET model implemented in the software packages was the Curtice FET model [11, 52–54]. The model is very simple, but includes all important transistor parameters – pinch off voltage, transconductance parameter β etc, Eqs. (1)–(5). The model describes well the transconductance and gain with the parameter β, output conductance via parameter λ etc. Due to simplicity and easy to understand and extract, the model is in wide use un general cases, because the model provides a good accuracy predicting gain, output power etc.

$$I_{ds} = \beta(V_{gst} - V_{t0})^2 * \tanh(\alpha * V_{ds}) * (1 + \lambda * V_{ds}); \quad (5)$$
$$\text{for} V_{gsi} \geq 0 \text{ and } I_{ds} = 0 \text{ for } V_{gst} < 0;$$
$$V_{gst} = V_{gsi}(t - T) - (V_{t0} + \gamma \cdot V_{dsi}); \quad (6)$$

Parameter β is transconductance parameter, α define the slope of I_{ds} vs. V_{ds} in the linear region ($V_{ds} < V_{kn}$). λ is the slope in the saturated region ($V_{ds} > V_{kn}$). V_{t0} is the pinch-off voltage. In the CAD tool implementation it is important to set the I_{ds} current equal to 0 for V_{gs} voltages less then pinch-off voltage V_{t0}. There are changes and improvements of the model equations in order to be implemented in the software packages [52–54].

4.1.2. Extended model: Curtice cubic model [52–54]

Later the model was extended with 3-rd term in the polynomial function [52–54] to improve fit for the 3-rd harmonic:

$$I_{ds} = (A_0 + A_1 \cdot V_x^2 + A_2 \cdot V_x^2 + A_3 \cdot V_1^3)\tanh(\gamma * V_{ds}); \quad (7)$$
$$V_1 = V_{gs}(t - \tau)(1 + \beta \cdot (V_{\text{out0}} - V_{ds}));$$
$$\text{for} \quad V_{gsi} - V_{t0} \geq 0 \quad \text{and} \quad I_{ds} = 0 \quad \text{for} \quad V_{gs} - V_{t0} < 0;$$

A_0, A_1, A_2 are polynomial coefficients for the I_{ds} vs. V_{gsi} dependence, V_{out0} is the drain voltage β is extracted.

4.2. Materka-Kacprzak Model [12, 52–54]

A model implemented in simulators soon after the Curtice model was Materka-Kacprzak model [12, 52–54], Eq. (10). The model addresses several important issues – ability to change the transconductance slope with the parameters E_e and K_e and change of the slope of the output conductance with the parameter S_s, K_g.

$$\begin{aligned} I_{ds} = {} & I_{dss}(1 - V_{gsi}(S_s \cdot V_{dsi}/I_{dss}) \\ & \times(1 - V_{gsi} \cdot (t - T)/V_{t0} + \gamma V_{dsi})^{(E_e + K_e \cdot V_{gsi}(t-\tau))} \\ & * \tanh(S_l * V_{dsi}/(I_{dss} \cdot (1 - K_g \cdot V_{gsi}(t - T)), \\ & \text{for} \quad V_{gsi} - V_{t0} \geq 0 \quad \text{and} \quad I_{ds} = 0 \quad \text{for} \quad V_{gst} - V_{t0} < 0; \end{aligned} \tag{10}$$

where I_{dss} is the saturation drain current, V_{t0}– threshold voltage, E_e exponent defining the dependence of saturated current, K_e description of dependence on gate voltage, K_g dependence on V_{gs} of the drain slope in linear region, S_l linear slope of $V_{gs} = 0$ drain characteristic, S_s saturation region drain slope at V_{gs}.

4.3. Triquint Model [21, 52–54]

The major companies like Triquint and Agilent also created FET models and help to extract these models.

In the Triquint model [21] controlling gate voltage is defined as ln (exp (V_{gs})) Eq. (11):

$$\begin{aligned} & I_{ds} = I_{ds0}/(1 + \Delta I_{ds0} V_{dsi}); V_{gst} = V_{gsi}(t - T) - V_{t0} + \gamma^* V_{dsi} \\ & I_{ds0} = (\beta/1 + U V_{gsi}) V_g \cdot K_{\tanh} \\ & V_g = Q V_{st} \cdot \ln(\exp(V_{gst}/Q \cdot V_{st}) + 1); \\ & V_{st} = (N_g + N_d \cdot V_{dsi}) V_t \\ & K_{\tanh} = a \cdot V_{dsi}/(1 + a \cdot V_{dsi}^2)^{0.5} \end{aligned} \tag{11}$$

where I_{ds0}, β is transconductance parameter,V_{t0} pinch-off voltage, U mobility degradation parameter, γ slope of the pinch-off voltage, Q-Power low parameter, N_g Sub-threshold drain parameter, N_d, sub-threshold drain parameter, ΔI_{ds0} Slope of drain characteristics in the saturated region, α slope of drain characteristic un the linear region, T-Channel transit time delay.

4.4. EESOF Model [52]

This is very complete model and is frequently used by foundries, it is supported by complimented extraction programs. Part of model equations is given

by Eq. (12). The model addresses different issues like changing the shape of the transconductance G_m, influence of V_{ds} on G_m and output characteristics etc:

$$\begin{aligned} V_{ts} &= V_{ch} + (V_{ts0} - V_{ch})/(1 + \gamma(V_{ds0} - V_{ds}); \\ I_{ds0} &= G_m \max\left[V_{ch} + V_x(V_{gs}) - ((V_{g0} + V_{t0})/2)\right]; \\ g_{m0} &= G_m \max\left[1 + \gamma(V_{ds0} - V_{ds})\right]; \\ g_{ds0} &= -G_m \max \gamma(V_{gs} - V_{ch}); \end{aligned} \tag{12}$$

4.5. Chalmers FET Model [27, 52–54]

The basic idea in this model is to connect and use directly measured parameters in order to simplify modeling and extraction Eq. (13a). It is supported by complimented extraction programs. The model equations are with continuous derivatives, without poles from $-\infty$ to $+\infty$, without switching or conditioning. The model is optimized to work in the saturation region for $V_{ds} > V_{\text{knee}}$ and V_{gs} for the peak of the transconductance. For saturated V_{ds} and $V_{gs} = V_{pk0}$ the function $\tanh(\alpha V_{ds})(1 + \lambda V_{ds}) \simeq$; $(\lambda \ll 1)$, and the drain current is $I_{ds} = I_{pk}$ by definition. The parameter $P_1 = g_m/I_{pk}$, will automatically define the FET transconductance g_m at this point. Parameters V_{pk0}, I_{pk}, $P_1 = g_m/I_{pk}$ are taken directly from the measurements and as result, the extraction is very simple i.e., 3 parameters $> I_{pk}, V_{pk0}, P_1$ at saturated V_{ds}. The model and derivatives are strictly defined at V_{pk0} and in the vicinity of V_{pk0} where the maximum of the transconductance occurs. For wider range of drain voltages V_{ds} two more parameters $\alpha, \boldsymbol{\lambda}$ are used:

$$\begin{aligned} I_{ds} &= I_{pk}(1 + \tanh(P_{1m}((V_{gs} - V_{pk0}))\tanh(\alpha V_{ds})(1 + \lambda V_{ds}) \\ &\simeq 1; (\lambda \ll 1) \end{aligned} \tag{13a}$$

$$I_{ds} = I_{pk} \quad \text{at} \quad V_{pk0}, G_m = I_{pk} * P_1; \tag{13b}$$

The parameter $\boldsymbol{\alpha}$ together with R_d (and all DC transmission line resistances in the measurement setup) will define the slope of I_{ds} vs. V_{ds} at small drain voltages $V_{ds} < V_{\text{knee}}$. The parameter $\boldsymbol{\lambda}$ will define the slope of I_{ds} vs. V_{ds} at high $V_{ds} > V_{\text{knee}}$ and is extracted at small currents to avoid the influence of the self-heating. These two parameters are common for many models.

For devices with complicated doping profile more sophisticated model structure can be used. The gate dependence is described as a power series using more terms in the power series as P_2, P_3 to track variety of I_{ds} vs. V_{gs} gate dependences. The parameter P_2 will introduce asymmetry of the I_{ds} vs. V_{gs} and will influence the second harmonic and parameter P_3 will trim drain current at gate voltages close to the pinch off and influence the 3-rd harmonic. Typically three terms are enough to provide accuracy better then 5%. As it follows from experimental data, some of parameters like V_{pk}, P_1 are

bias and temperature dependent and in order to have a global model, they are modeled [27], Eq. (15) as:

$$I_{ds} = I_{pk}(1 + \tanh(\Psi_p))\tanh(\alpha V_{ds})(1 + \lambda V_{ds} + \lambda_{sb} \cdot e^{V_{dg}}); \quad (14)$$

$$\psi_p = P_{1m}((V_{gs} - V_{pk0}) + P_2(V_{gs} - V_{pk0})^2 + P_3(V_{gs} - V_{pk0})^3);$$

$$P_{1m} = g_{mpk}/I_{pk};$$

$$V_{pk}(V_{ds}) = V_{pk0} + \Delta V_{pks}\tanh(\alpha_s V_{ds}) - V_{sb2}(V_{dg} - V_{tr})^2; \quad (15)$$

$$\alpha = \alpha_r + \alpha_s[1 + \tanh(\psi_p)]; \quad P_{1m} = P_{1s}(1 + B_1/\cosh(B_2 \cdot V_{ds}));$$

Parameter V_{pk} describes the change of V_{pk} due to the drain voltage, and parameters α_r and α_s change the slope of I_{ds} at small V_{ds}. A good fit in the area of small or negative drain voltages can be important for circuits working at low V_{ds} like resistive mixers, switches etc. The parameters are rather independent in adjusting I_{ds}. For example α_r will influence the drain current at small V_{ds} and small currents, and α_r will influence the drain current at small V_{ds}, and high currents, close to the knee, Figure 2b. Above knee the slope of I_{ds} vs. V_{ds} is adjusted with parameter λ. Breakdown modeling, if required, can be treated with parameters V_{tr}, L_{sb} and V_{sb2} [27, 52–54].

Many of these parameters are typical for all FET. For example, transconductance parameter P_1 for MESFET's is typically $P_1 = 1.2$–1.5, $P_1 = 2 > 4$ for the HEMT, $P_1 = 0.3$ for GaN, $P_1 =$ for 2 for LDMOS etc. High value of P_1 will produce higher gain for the same current, which is good for low noise and high gain applications. But if P_1 is very large, the gate voltage swing (input power) can be limited and this will influence the linearity and inter-modulation characteristics. Transistors with low P_1 like MESFET's, GaAs HEMT's specially designed for linear applications, SiC and GaN FET will have better inter-modulation properties, but lower gain. This means that some compromise should be made if we want to have high efficiency high power and linear amplifier. Depending on the application we can select the best P_1 for our application. Nowadays the physical simulators are fast enough and can help to optimize the device structure for specific application. In Table 1 are given some basic data for different FET devices.

Normally we operate the devices at positive drain voltages and it seems obvious that there is no need to look at negative V_{ds}. When drive level is small this is correct, but when the device is used as power amplifier, switch or mixer, the instantaneous drain voltage is swinging into the negative V_{ds} region. i.e., the drain current model should describe properly the I_{ds} at negative V_{ds} even if the device is biased with positive V_{ds}. Usually, in the circuit simulators the model switching at negative V_{ds} is arranged in a simple way. When the drain voltage V_{ds} is positive the gate voltage V_{gs} controls the drain current. When V_{ds} is negative, the control voltage is switched to V_{gd} and I_{ds} current is calculated from the same equation with reversed sign (I_{ds} is negative). If the device is symmetrical, this is correct. But at the switching point $V_{ds} = 0$ will be a singularity and the

Table 1.

Parameter	MESFET	HEMT	HighGain HEMT	Linear HEMT	SiC	GaN	LDMOS
Ichan [A/mm]	0.3−0.6	0.3−0.6	0.17−0.25	0.3−0.6	0.35	1.5	0.75
P_1	1.1−1.5	2−3	4.5−5.5	1.5	0.1	0.3	2
V_{pk}	−0.5	−0.2	+0.05	−1.4	−9	−3	3.5
V_{knee}	0.75	0.75	0.75	0.75	9	4	3
α_s	1.3−1.5	2−2.5	3.7	1.5	0.14	0.4	1.5
Cap [pF/mm]	1	1	1.0	1.3	0.8	0.7	0.6

derivative of I_{ds} is not defined. As a consequence, it will be more difficult for the HB to converge and the results of the simulations can be wrong in the vicinity of $V_{ds} = 0$. A solution to this is a continuous, single model equation for I_{ds} valid for all control voltages from $-\infty$ to $+\infty$.

For cases like switches and resistive mixers applications, operating at low and negative V_{ds} (as in Figure 4) the drain current equation Eq. (16) is composed from two sources I_{dsp} and I_{dsn}, and which are controlled respectively by V_{gs} and V_{gd} [52]:

$$
\begin{aligned}
I_{ds} &= 0.5(I_{dsp} - I_{dsn}); \qquad (16)\\
I_{dsp} &= I_{pk}(1 + \tanh(\Psi p))(1 + \tanh(\alpha V_{ds})) \cdot (1 + \lambda V_{ds} + \lambda_{sb}.e^{V_{dg}-V_{tr}}),\\
I_{dsn} &= I_{pk}(1 + \tanh(\Psi n))(1 - \tanh(\alpha V_{ds}))(1 - \lambda V_{ds}),\\
\psi_p &= P_{1m}((V_{gs} - V_{pk0}) + P_2(V_{gs} - V_{pk0}) + P_3(V_{gs} - V_{pk0})^3),\\
\psi_n &= P_{1m}((V_{gd} - V_{pk0}) + P_2(V_{gd} - V_{pk0}) + P_3(V_{gd} - V_{pk0})).
\end{aligned}
$$

When V_{ds} is 0 the currents $I_{dsp} = I_{dsn}$ and the drain current $I_{ds} = 0$.

There are cases with when the device has very complicated I_{ds} vs. V_{gs}, V_{ds} dependencies and it is very difficult to obtain a good correspondence between the model and measurements. In this case the power series can be replaced with a data set calculated from measured data [28] i.e. combining both the empirical equivalent circuit models with table based models [17–20] or using the Table Based Model. Using mixed Empirical-Table Approach is possible to combine and extract the best from both. The Empirical Model is serving as envelope for the Table Based Model and the problem with spline function selection, out of the measurement region extension and convergence are solved. This is because, a correct spline functions i.e., FET model equations are used as a spline. The derivatives are continuous and correct and the model will converge well. The linear extrapolation out of the measured data range will be adequate, because the empirical model will limit the solution. The model will be limited

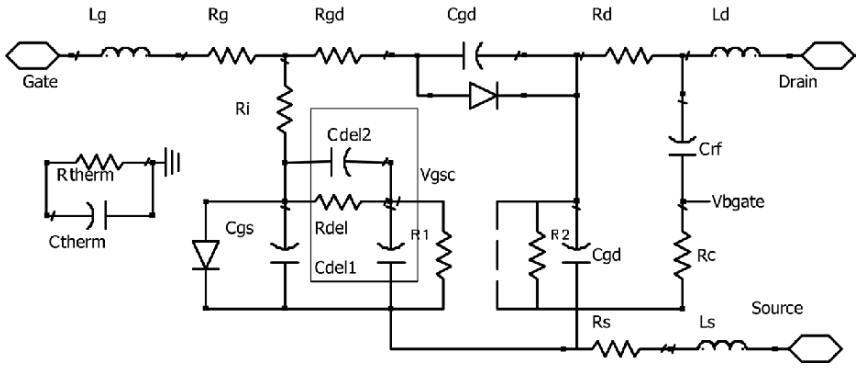


Figure 10. Large Signal Equivalent circuit of the transistor.

and valid out of the measured range, because the data set is naturally limited by using the measured data for the extraction.

Quite often there is spread of parameters and it is important to give the users some flexibility to tune basic model parameters in the Empirical or mixed Empirical – Table Based Model. For example there are always some tolerances in gm, pinch-off voltage, thermal resistance etc. and the model can be arranged in such a way that the user, without making complete measurement and extraction set can change only the required parameter. This can be done with a proper arrangement of the Mixed Empirical – Table Based Model. The Mixed Empirical Table Based Model can be arranged to access the basic parameters $I_{pk}, V_{pk}, P_1, \lambda$, capacitances combining benefits of the Empirical and the Table-Based models. The LS Model is extracted for a typical device, but later it should be possible to trace the process tolerances etc.

The FET large signal equivalent circuit with reactive components included is rather standard, Figure 10. Linear are considered most of the elements and nonlinear (bias dependent) are considered I_{gs}, I_{ds} and capacitances C_{gs} and C_{gd}. The difference between the simple small signal equivalent circuit Figure 1 and LS equivalent circuit are diodes at the gate drain current source, thermal and delay sub-circuit. They are described in more detail in the following sections.

5. Capacitance Models

5.1. Charge Conservation

In multiple extraction and physical simulations on different FET structures was evaluated that the main device capacitances are bias dependent on both voltages $C_{gs} = f(V_{gs}, V_{ds})$ and $C_{gd} = f(V_{gd}, V_{ds})$, Figures 11, 12. This is normal

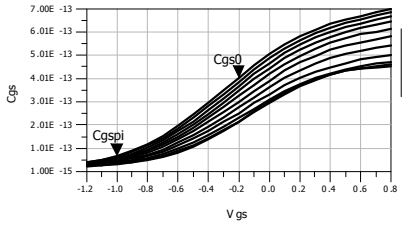


Figure 11. C_{gs} vs. V_{gs}, V_{ds} parameter.

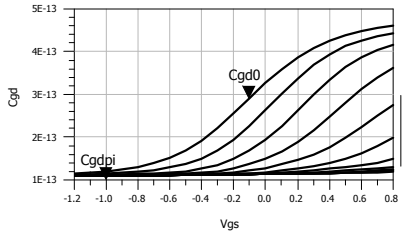


Figure 12. C_{gd} vs. V_{gs}, V_{ds} parameter.

to expect, the problem is how to implement this in the circuit simulators. The charge implementation and conservation problem is very old, several good works are devoted on the topic and propose solutions [4, 45–47]. Traditionally FET total gate charge has been model by two nonlinear charges: gate-source Q_{gs} and gate-drain charge Q_{gd}. A consequence of the dependence of the capacitances on the remote voltage is that we need additional charge control element which D. Root called transcapacitances [17–20].

There are several ways to implement the gate charges into two individual components: Division by capacitances, division by Charge [4].

As FET devices have both gate to source capacitance C_{gs} and gate to drain C_{gd}, it seems natural to use them directly. In this case:

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}}; \quad C_{gd} = \frac{\partial Q_g}{\partial V_{gd}} \tag{19}$$

In the case we use capacitances in the implementation, the currents I_s and I_d depend only on the time derivative of their own terminal voltage and not on the changes in any remote voltage. The resulting small signal equivalent circuit is completely consistent with the large signal equivalent circuit and requires no transcapacitances.

Another option is to divide the gate charge Q_g into two independent charges. Then:

$$Q_g = Q_{gs} + Q_{gd} \tag{20}$$

where both Q_{gs} and Q_{gd} are functions of V_{gs} and V_{gd}. Differentiating Q_g with respect to time gives:

$$\begin{aligned} I_g &= I_s + I_d \\ I_s &= \frac{\partial Q_{gs}}{\partial t} = \frac{\partial Q_{gs}}{\partial V_{gs}}\frac{\mathrm{d}V_{gs}}{\mathrm{d}t} + \frac{\partial Q_{gs}}{\partial V_{gd}}\frac{\mathrm{d}V_{gd}}{\mathrm{d}t}; \\ I_d &= \frac{\partial Q_{gd}}{\partial t} = \frac{\partial Q_{gd}}{\partial V_{gs}}\frac{\mathrm{d}V_{gs}}{\mathrm{d}t} + \frac{\partial Q_{gd}}{\partial V_{gd}}\frac{\mathrm{d}V_{gd}}{\mathrm{d}t} \end{aligned} \tag{21}$$

In this case the reactive source and drain currents result from both capacitances and transcapacitances and both definitions charge and capacitance are not equivalent.

A common approach to implement the charge part of every transistor model is to use directly the charge approach. In this case the current of the capacitance is easy to calculate by taking the time derivative of the charge – i.e., multiplying by $j\omega$. This operation is very reliable, because making the derivative will always produce only one solution. This works very well with capacitance which depends only on their own terminal voltage. The problem with all FET transistors is that the gate capacitance depends on the two controlling voltages. When we multiply by $j\omega$ we are making in fact the full derivative of the charge and the end result is not correct if the charge is obtained as integrating the capacitance equation by the terminal voltage. It is obvious that partial (considering the remote part constant) and full derivatives are different. This can be shown with the case of the capacitance model using Eqs. (22–25). Integrating the C_{gs} capacitance by the terminal voltage V_{gs} we obtain Eq. (26). It is assumed that V_{ds} part is constant. If ordinary charge approach is used, multiplying by $j\omega$ will bring obviously different results. i.e. we need to compensate the difference due to the partial derivative – we need an extra term the transcapacitance [4, 17–20, 45–47].

In some advance simulators, for the compiled models, the derivatives of the charges are calculated analytically using the selected terminal voltage. Then the problem is solved in a better way in the sense that the CAD tool is making the derivative vs. respective terminal voltage, considering the remote voltage constant. In this case we will have the capacitance described as a derivative of the charge at the terminal voltage and the capacitances calculated by both methods should be similar.

In the first case we need a correct description of the charge which will compensate for the difference between the partial and full derivative otherwise the model will not be charge conservative. The consequence that the model is not charge conservative is that this difference will create additional current, solution will become path dependent and the HB of the simulator will have difficulties to converge [4, 17–20, 45–47].

5.2. Capacitance Expressions

Figure 11 shows the typical shape of the C_{gs} and C_{gd} capacitances. When the device is symmetrical, for $V_{ds} = 0$ capacitances C_{gs} and C_{gd} are equal. For gate voltage voltages close to pinch off capacitances C_{gs} and C_{gd} have their minimum values C_{gspi} and C_{gdpi} and this should be used in the capacitance models to define the capacitance at the pinch-off. Increasing V_{gs} will increase C_{gs} and C_{gd}. Generally, when V_{ds} increase C_{gs} will increase and saturate at voltages around $V_{ds} = 2\,\mathrm{V}$. In general, the shape of capacitance dependencies will depend on the doping profile and material and in some specific cases a special capacitance model can be developed.

A reasonably good description of the capacitance shape for FET can be obtained using Eqs. (22)–(25) [28, 52–54]:

$$\psi_1 = P_{10} + P_{11} * V_{gs} + P_{111} * V_{ds}; \quad \psi_2 = P_{20} + P_{21} * V_d \tag{22}$$

$$\psi_3 = P_{30} - P_{31} * V_{ds}; \psi_4 = P_{40} + P_{41} * V_{gd} - P_{111} * V_{ds} \tag{23}$$

$$C_{gd} = C_{gdp} + C_{gd0} * (1 - P_{111} + \tanh[\psi_3]) * (1 + \tanh[\psi_4] + 2 * P_{111}) \tag{24}$$

Independently of the implementation (Capacitance or Charge) and the type of model, in order to have the capacitance model charge conservative it is **mandatory** to fulfil following basic requirement:

$$\frac{\partial C_{gs}}{\partial V_{gd}} = \frac{\partial C_{gd}}{\partial V_{gs}} \tag{25}$$

This means that the equations for the capacitances C_{gs} and C_{gd} should be symmetrical and model coefficients should be selected properly. In the case of Eqs. (22)–(24) this means that $P_{11} = P_{41}$ and $P_{22} = P_{33}$. The consequences can be non-convergence in the HB. A good test for the consistency of the capacitance models is to simulate the S-parameters in the small signal case and S-parameters simulated in the LS case with HB, but with very small input power. If this difference is small, this means that the capacitance model is correct and implemented properly. For capacitances described with Eqs. (19), (20) the charges are:

$$\begin{aligned} Q_{gs} &= \int C_{gs} * \partial V_{gs} = C_{gsp} * V_{gs} + C_{gs0} * (\Psi_1 + Lc1 - Q_{gs0}) * (1 + \tanh[\Psi_2]))/P_{11} \\ Lc1 &= \log[\cosh(\psi_1)]; \quad Lc10 = \log[\cosh(P_{10} + P_{111} * V_{ds})] \\ Q_{gs0} &= P_{10} + P_{111} * V_{ds} + Lc10 \end{aligned} \tag{26}$$

$$
\begin{aligned}
Q_{gd} &= \int C_{gd} * \partial V_{gd} = C_{gdp} * V_{gd} + C_{gd0} \\
&\quad * (\Psi_4 + Lc4 - Q_{gd0}) * (1 - P_{111} + \tanh[\Psi_3]))/P_{41} \\
Lc4 &= \log[\cosh(\psi_4)]; \quad Lc40 = \log[\cosh(P_{40} + P_{111} * V_{ds})] \\
Q_{gd0} &= P_{40} + P_{111} * V_{ds} + Lc40
\end{aligned}
\tag{27}
$$

The functions for capacitances, charges and their derivatives are symmetrical and defined from $-\infty < V_{gs}, V_{gd}, V_{ds} < +\infty$. A problem that should be accounted is the boundary condition problem. – i.e., what will be with the capacitances (charges) when the capacitance terminal is shorted and there is a voltage on the remote terminal as in Figures 13, 14. For example, when the gate source junction is shorted ($V_{gs} = 0$) the capacitance C_{gs} will continue to exist and the charge Q_{gs} should be $Q_{gs} = 0$ independent from remote voltage V_{ds}. This puts additional constraints on the boundary conditions for the charge definition. For these reasons some circuit simulators use separate Q_{gs}, Q_{gd}, but taking into account the boundary condition with charges Q_{gs0} and Q_{gd0}. As it can be seen from Figures 13, 14, when $V_{gs} = 0$ the charge $Q_{gs} = 0$ and when $V_{gd} = 0$ the charge $Q_{gd} = 0$ independently from the remote voltage V_{ds}.

Generally the most circuit simulators use either standard charge approach or direct capacitance approach.

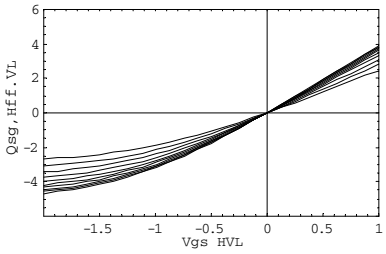


Figure 13. Charge Q_{gs} vs. V_{gs}.

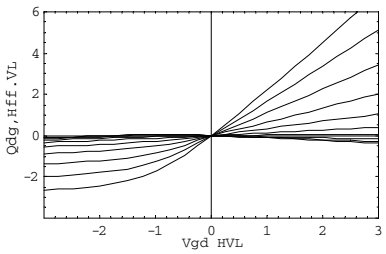


Figure 14. Charge Q_{gd} vs. V_{gd}, V_{ds} parameter.

It is important to know that **always should be some small difference** in the calculated S(Y)-parameters depending on the implementation type- capacitance or charge, even if the same model parameters for the capacitances are used. The origin of this difference in the calculated S-parameters depending on the implementations is very well described by S. Maas [4]. As a consequence, it is important to keep the same tape of the model in extraction and later in the circuit simulations, because this small difference can be accounted fitting the S-parameters with the selected capacitance model and fulfilling necessary condition Eq. (25c).

Possible solution to the problem is to use a single gate charge Q_g definition. The total gate charge Q_g is function of V_{gs} and $V_{gd}(V_{ds})$ [28, 49]. When some of these voltages changes, Q_g change as well-the gate current is $\mathrm{d}Q_g/\mathrm{dt}$. In this case, the total gate charge $Q_g = Q_{gs} + Q_{gd}$ and I_g composed by derivatives of the two charges Q_{gs} and Q_{gd}. It follows from this that $I_g = I_s + I_d$.

Where

$$\begin{aligned} I_s &= \frac{\mathrm{d}Q_{gs}}{\mathrm{d}t} = \frac{\partial Q_{gs}}{\partial V_{gs}}\frac{\mathrm{d}V_{gs}}{\mathrm{d}t} + \frac{\partial Q_{gs}}{\partial V_{gd}}\frac{\mathrm{d}V_{gd}}{\mathrm{d}t} \\ I_d &= \frac{\mathrm{d}Q_{gd}}{\mathrm{d}t} = \frac{\partial Q_{gd}}{\partial V_{gs}}\frac{\mathrm{d}V_{gs}}{\mathrm{d}t} + \frac{\partial Q_{gd}}{\partial V_{gd}}\frac{\mathrm{d}V_{gd}}{\mathrm{d}t} \end{aligned} \tag{28}$$

This will work well and the only problem is that we cannot extract charges directly and we need to derive them via capacitances and S-parameters. Because of these complications with the charge definitions and difficulties with implementation in the CAD tools, many circuit simulators use capacitance formulation. As explained, when capacitance approach is used the resulting small-signal equivalent circuit consists of the small signal capacitances evaluated at the corresponding DC voltage.

The first step in the Cap implementation is to calculate the time derivatives $\mathrm{d}V_{gs}/\mathrm{d}t$ and $\mathrm{d}V_{gd}/\mathrm{d}t$ of the respective terminal voltage. i.e. the simulator should calculate the time derivative in reliable way. When the CAD tool is able to make the transient analysis (as most modern CAD tools do), the capacitance type of implementation can be done reliably. The respective current is obtained by multiplying the time derivative with the capacitance equation:

$$I_{gsc} = C_{gs} * \frac{\partial V_{gs}}{\partial t}; \quad I_{gdc} = C_{gd} * \frac{\partial V_{gd}}{\partial t} \tag{29}$$

It is important to arrange the DC component of the time derivative to be equal to 0 within the accuracy of the HB simulations (typ. less then $I_{dc} < 10^{-15}$ A). If implemented in a proper way, this will result in consistent small- and large-signal models and we don't need any trans-capacitances. This because, the time derivatives depend only on their terminal voltage. A problem that can arise using this approach is the convergence in the HB simulations. This can happened, in the first step of calculating the time derivatives if the functions for

the C_{gs}, C_{gd} are not continuous with well-defined derivatives. Using smooth functions with infinite numbers of derivatives without singularities from $-\infty$ to $+\infty$ helps to solve the problem. Another important moment is to implement these operations Eq. (29) in a proper way.

Generally, the convergence problems are caused by poor numerical conditioning of the Jacobian matrix, caused by a combination of very large and very small numerical values. In nearly all new circuit simulators the Krylov solvers are much less robust, when dealing with ill-conditioned matrices, than some of the older solvers without Krylov solvers. So, in the past, some of these things were not a problem, but suddenly now they are.

In the capacitance implementation, problems can be caused by poor numerical conditioning of the Jacobian matrix, due to a combination of very large and very small numerical values.

For example, in the FET model with capacitance formulation we need to generate $\mathrm{d}V/\mathrm{d}T$ and $C(V)$. The derivative $\mathrm{d}V/\mathrm{d}T$ is very large, but $C(V)$ is very small, and when these are put in the Jacobian, the $\mathrm{d}V/\mathrm{d}T$ entries are much larger than other entries, so the matrix solution is poor.

The simplest solution proposed by S. Maas [4] and implemented in Microwave office, AWR is to multiply $\mathrm{d}V/\mathrm{d}T$ by a small number (for example 1e–9) before passing it to the capacitance expression. Then, C(V) is multiplied by the inverse of that number (1e9 in this case). It seems simple, but it will make a lot of difference. It is a good idea to arrange this scaled factor to be accessed in easy way by the user, because the best performance depends on the circuit (derivatives of the charge) and the user can find what is best for his application.

If this is done properly, the FET model with the capacitance implementation can converge better, specially if we keep the DC current via capacitance $I_{\mathrm{cap}} = 0$ in the HB simulations.

6. Recent Extensions

6.1. Thermal Effects

It is known that solid-state devices are temperature sensitive. There two main reasons for the change of the transistor parameters vs. the temperature. The first is the change of carrier concentration vs. the temperature and the second-change of mobility. Both are reduced when the temperature is increased. The reduction of the carrier concentration will reduce the channel current and reduced mobility will produce smaller transconductance at higher temperature for the FET devices, i.e. negative T_{cIpk}, T_{cP1}. The change of the mobility will also influence the speed of the device and in turn change (increase) the device capacitances (positive $T_c C_{gs0}$). This effect is beneficial when the device is used as a small

signal, low noise amplifier – cooling the amplifier will drastically improve the gain and noise performance of the FET amplifier. This is due to increased g_m (gain) and reduced channel noise which are strongly dependent on the channel temperature. The thermal effects are very negative for high power FET devices. The result is significant reduction of the drain current and gain at high operating temperatures and when dissipated power is high. In addition to the effects directly observed (reduction of the current and the transconductance) the RF and dispersion characteristics are also influenced. This is due to the increased influence of the traps at higher temperature. To account for the temperature changes the equations for the currents and charges should be extended with the terms describing the temperature dependencies vs. junction temperature $T_j = R_{\text{therm}} \cdot P_d + T_{\text{amb}}$ where P_d is dissipated power T_{amb} is the ambient temperature. The thermal resistance is generally nonlinear but for simplicity can be considered constant In this case the temperature increase can be modelled as a thermo-electrical circuit consisting of the thermal resistance R_{therm} and the thermal capacitance C_{therm}. The thermal capacitance models the thermal storage of the structure and the thermal constant is $R_{\text{therm}} * C_{\text{therm}}$. When thermal equivalent circuit is used, $T_j = V_{\text{therm}}$ can be treated like any other control voltage and can be found interactively in the HB simulations. i.e., $T_j = T_{\text{amb}} + V_{\text{therm}}$; $P_d = P_{dc} + P_{rf}$. Because the dissipated power contain the RF power P_{rf} the junction temperature will be time dependent. The thermal mass of the chip will filter out the RF temperature variations, but it will not filter the low frequency modulation signal and we can experience so called memory effects.

To account for the basic effects of self-heating we need to make temperature dependent at least several parameters like: I_{pk}, which are connected with the channel current (approximately $I_{\text{chan}}/2$), transconductance *connected* with mobility (parameter $P_1 = g_m/I_{pk}$), and device junction capacitances C_{gs0} and C_{gd0}. In addition to these parameters, for high power devices the delay parameters R_{del}, C_{del} and breakdown parameters should be considered temperature dependent.

If low frequency modulation of the signal is to be considered, dispersion parameters can be made temperature dependent. The temperature dependencies of all these parameters are rather linear in the temperature range $\pm 100^\circ$ C and temperature coefficients are very small. Typically for GaAs FET $T_c I_{pk}$ and $T_{cP1} = -0.025$. Because of this, they can be modeled as linear functions:

$$K = K_0(1 + T_{CK}(T_j - T_{\text{ref}})) \tag{30}$$

where $K = I_{pk}, P_1, C_{gs0}$ and C_{gd0}. T_{CK} is the temperature coefficient of parameter K. The temperature T_j is determined from the total dissipated power and the thermal resistance.

The change of device parasitic resistances is very small vs. temperature and it is usually considered that the resistors temperature should be equal to the device operating temperature.

6.2. Dispersion Modelling

Years ago when first FET were made, the researchers were unsatisfied to find that transconductance gm and output resistance (conductance) R_{ds} are quite different at high frequency in comparison to the DC values. Figure 15 show typical shape of the g_m and g_{ds} vs. frequency. It should be noticed that the effect is concentrated at rather low frequency, typically below 1 kHz and all the changes are usually settled at frequency 5–10 MHz. The interesting thing is that in some HEMT devices is possible find even a small increase of the extracted g_m vs. frequency.

It was found that the reasons for these effects are basically the material and surface defects which are always present. As long as material and device surface have some defects – we will always have dispersive effects.

From the first glance these changes look rather small and seem that they can be ignored. This is correct in some cases, but when the device is working as an oscillator, RF switch, RF modulated high power amplifier these small changes in the output conductance and transconductance will produce significant effects. The oscillator will become noisy, the slope of the switched RF power will be changed and in high power amplifiers memory effects will be visible – i.e., the output will depend in some way on the modulating signal. As usually, these effects are becoming more critical at high temperatures – i.e., will be more critical for high power and high temperature of operation.

Devices which can deliver high power should have high operating current and high breakdown voltage i.e., rather large device size. Due to this, the dispersive effects become more significant, because they are directly proportional to the surface area [29-41]. Dispersive effects will become more significant for devices with new material systems like GaN, SiC, but even for GaAs these effects can be significant. For this reason, a proper implementation of more accurate dispersion models in circuit simulators is becoming important. An additional effect of highly dissipated power is that as the device is operating at

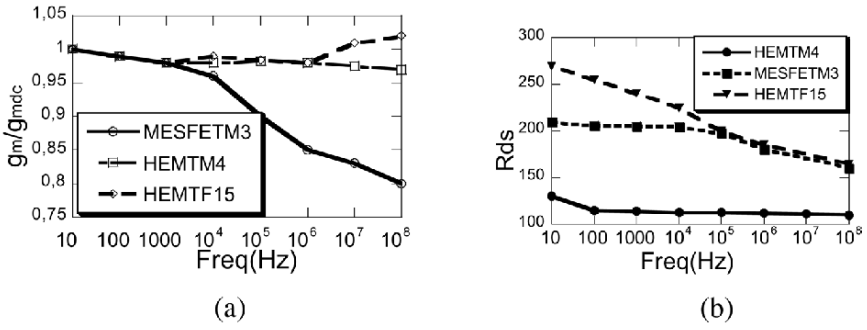


Figure 15. (a) Transconductance gm and (b) R_{ds} vs. frequency.

higher junction temperatures the thermal problems will become more severe, because power is dissipated in a comparably small volume that can be locally overheated. Finally, for large devices the intrinsic delay can cause additional problems. Due to all these effects, at high frequency the high power devices do not deliver the power their DC and small signal S-parameters predict. This can be seen when comparing the maximum tuned output power at different operating frequencies. It is known that this decrease of the maximum tuned power is not due only to the higher losses in the matching circuit and higher resistive losses in the transistor, but largely to the more pronounced physical effects as listed above.

On the topic of correct modeling of the g_m and R_{ds} dispersion are devoted many papers [29-41] and this issue is probably even more important with the new devices like CMOS, GaN. The best is to use an EC based on the physical approach as [29] or back gate approach [30–33], but usually in circuit simulators the simple EC approach is used [34], as shown in Figure 10. In this case a simple R, C branch is used to model the R_{ds} dispersion. The R_c should be bias dependent; otherwise the simulator will not produce correct results for I_{ds}, and Power Added Efficiency at RF. The network with constant R_c will give additional RF current $I_{rf} = V_{ds}/R_c$ and this will produce an extra DC current in the simulations. A correction to the problem can be made making R_c bias dependent and this is the simplest solution implemented in CAD tools:

$$R_{c\min} + R_{c\max}/(1 + \tanh[\psi]) \tag{31}$$

Quite often we forget that the device is symmetrical and dispersion effects existing on the drain side (G_{ds}) exist on the gate side (g_m). Using a similar network at the input R_{cin}, C_{rfin} we can model g_m dispersion, as shown Figure 10.

The best is to organize the model structure in such a way that four terminals are available. The fourth terminal can be used to account for dispersion using the back-gate approach. [30–33]. It is known that this will produce a proper SS description of the g_m and g_{ds} dispersion. If implemented in a proper way in the LS model, this approach works well in both the LS and SS case. This can be done by injecting the feedback RF signal V_{bgate}, shown in Figure 10, directly into the I_{ds} equations, Eq. (15b). From the parasitic coupling, the output RF voltage via C_{rf} and R_c, the backgate voltage V_{bgate} is fed to the gate and controls the drain current at RF. Using this approach, the parameters R_c and C_{rf} will have values close to values we can expect from the device physics.

The modified current equation including the backgate part is [63, 64]:

$$V_{pk}(V_{ds}) = V_{pks} - \Delta V_{pks} + \Delta V_{pks} * \tanh(\alpha_s V_{ds} + K_{BG} * V_{\text{bgate}}); \tag{15b}$$

$$P_{1m} = P_1 * [(1 + \Delta P_1)(1 + \tanh(\alpha_s V_{ds}))]; \tag{32a}$$

$$P_{2m} = P_2 * [(1 + \Delta P_2)(1 + \tanh(\alpha_s V_{ds}))]; \tag{32b}$$

$$P_{3m} = P_3 * [(1 + \Delta P3)(1 + \tanh(\alpha_s V_{ds}))]; \tag{32c}$$

where ψ_p is a power series function centered at V_{pk}. A new term K_{bg} is introduced which controls the intrinsic gate voltage at RF. As it was mention parameters, like V_{pk} and $P_1, P_2, P_3, \ldots$ exhibit bias dependence and this has been accounted by Eq. (32) for the general use.

For high voltage devices, or when very accurate fit for I_{ds} and the harmonics is important, the equations Eq. (32) can provide improved fit, like was already demonstrated in Figure 5 [63]. This is because Eq. (32) gives the possibility to handle both positive and negative changes of the harmonic content. The basic parameters are determined directly from measurements and secondary parameters like P_{2m}, P_{3m}, K_{bg} are optimized with the CAD tool. Such modeling approach allows to use a simple extraction procedure and extracted parameters are trimmed using the CAD tool optimizers.

When dissipated power is small (less then 200 mW) then all the measurements can be done in one sequence, sweeping V_{gs} and stepping V_{ds} and measuring the currents and S-parameters. It is rather important to start measurements from low frequency in order to track the dispersion effects and to improve the accuracy of modelling of the current source.

For high power devices, multiple bias S-parameter measurements should be performed splitting the measurements in two voltage ranges $\rightarrow V_{ds} < V_{\text{knee}}$ and high currents and $V_{ds} V_{\text{knee}} - 30\,\text{V}$ and small currents as in the example in Figure 16. This is needed, because the high power devices operating in class B, C, D, E, F, are usually biased at high voltage and small current, but during the voltage swing they reach very high currents for V_{ds} around the knee voltage. That is why, it is important to evaluate the device along the typical load line. Such a detailed S-parameter evaluation will also provide information on whether the capacitances and their models are behaving properly, because most of the capacitance changes are below and around the knee voltage.

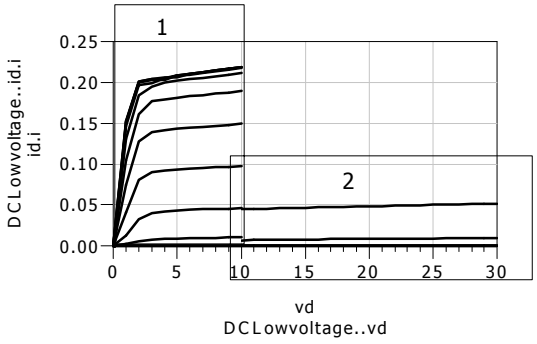


Figure 16. Dual region DC measurements: Region1 High I_{ds}, Low V_{ds}, Region2 Low I_{ds}, High V_{ds}.

6.3. Model Evaluation

It is commonly considered that performing a DC and S-parameter measurements is enough to extract a good quality transistor model. If the goal is to have a model which will predict the gain S-parameters and output power this is correct. Pulsed IV and S-parameter measurements can provide additional info, especially for high power or dispersive devices, but even these data is not enough. If we want to have a model which will predict properly harmonics, then some kind of LS measurements evaluating the harmonic content should be used to trim the model. Only in this case we can be confident that the model will describe the harmonics properly, because the DC and S-parameter evaluation is not enough. We can make very simple simulation experiment with the current source. Usually we are satisfied when the modelling accuracy for the current is better then 5%. We start with a model parameter $P_1 = 2$, $P_2 = 0$, $P_3 = 1.5$. If we change the parameter P_3 which is responsible for I_{ds} characteristics close to the pinch-off and influencing the 3 harmonic to $P_3 = 0.5$, we will see very small change – only 3–4% in the drain current. The same small change DI_{ds} will produce nearly 15 dB difference in the simulated 3-rd harmonic Figure 17. These results are common for every model and every transistor that is why it is important to evaluate the ability of models to describe harmonics with additional measurements.

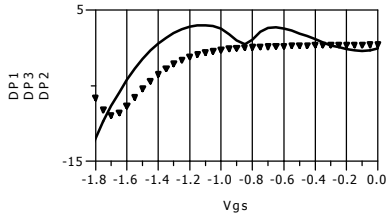


Figure 17. Change of the harmonic output.

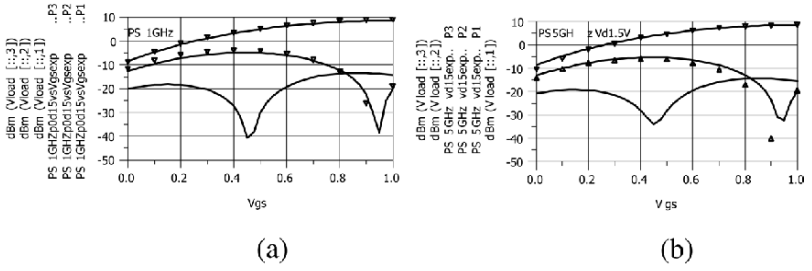


Figure 18. (a) PS measurement results 1 GHz (b) PS measurement results 5 GHz for CMOS device.

The simplest way to evaluate the harmonic contents generated from the device is the direct way to measure harmonics. It is good to evaluate the device at 2 fundamental frequencies – one low frequency – 0.1–1 Ghz depending on the device size to evaluate the nonlinearity of the current source and at high frequency close to the frequency we will operate the device. The masurements should be made sweeping V_{gs} and having as a parameter V_{ds}. Quite often we see that the people are showing P_{out} and harmonics vs input power. It can be shown that nearly every model can be adjusted to give reaonable correspondence, but later they will be surprised to see that the model is not describing harmonics accurately. Typically we need 10 measurements of V_{gs} and several V_{ds}. Figure 18 show some typical results.

6.4. Delay Modelling

The initial hope of researchers that a better model of the dispersion would solve the problem and provide an accurate prediction of the output power at high frequency for high power devices turned out to be false. It was found that even the good fit for the S-parameters does not provide the proper prediction of the output power at high frequency, i.e., it is not able to predict the significant drop of the tuned output power vs. frequency.

By using Large Signal Network Analyzer (LSNA) measurements [63] is possible to observe that the waveforms at high frequency are not efficient any more. The LSNA data provide very important information about the generated waveforms at the tuned condition directly at the device terminal. The model is supposed to reproduce accurately these waveforms.

At low frequency 2 GHz, the waveforms are quite normal, as shown in Figure 19 and Figure 20, and the device delivers 26 dBm at 10 dBm input power. At high frequency, the device is not able to swing to the DC values of the currents, refer to Figure 20b, this phenomenon is called current slump.

For example, at 18 GHz the minimum drain voltage that can be reached at 10 dBm power is 6.3 v, see Figure 20b, in comparison with 0.8 V at 1 GHz, and

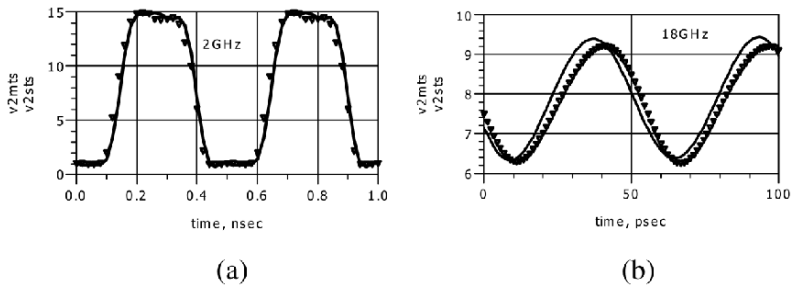
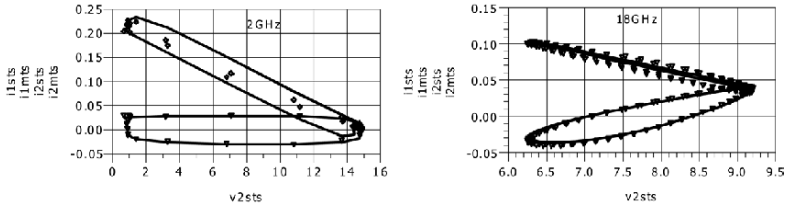


Figure 19. Time waveforms: (a) 2 GHz, (b) 18 GHz.



(a) (b)

Figure 20. Time waveforms I_{gs} (i1), I_{ds} (i2) vs. V_{ds} (v2) (a) 2 GHz, $V_{\text{dmin}} = 0.8$ V (b) 18 GHz $V_{\text{dmin}} = 6.3$ V.

see Figure 20a. The fit for the input current is good, which is a sign that the capacitance are not responsible for this and the capacitance models for C_{gs}, C_{gd} are correct. i.e. the capacitances are not responsible for the loss of power in tuned condition at high frequency.

It can be determined that the voltage V_{gsc} controlling the output current I_{ds} is reduced and delayed thus causing the output waveforms to not be able to follow the input. This was found to be one of the reasons for the low output power (respective low efficiency) at high frequency for high power FET devices.

It is known that in HB simulators is assumed that the model is quasi-static, nonlinear devices are evaluated in time domain and time (frequency) dependent equations for the currents will not behave properly [4, 17]. This means that time-delayed response, explicit frequency dependences of current equations should be avoided. From device physics, the only elements we can use to model the intrinsic part of the devices in circuit simulators are capacitances, resistances and equations connecting the currents and charges. Inductances and layout parameters can be associated with extrinsic part of the device and de-embedded.

In addition, the frequency dependence of the maximum output power is rather complicated and a simple RC network will not provide an adequate fit. After some trials it was found that a delay network (elements C_{del1}, C_{del2}, R_{del}), connected at the input (see Figure 10) provides a good description of these effects [63, 64]. At high frequency, the capacitor C_{del1} shunts the input and directly decreases the magnitude of the control voltage V_{gsc} and introduces the observed delay. The value of the delay capacitance was found by fitting the S-parameters and turned out to be very low, in the order of 2–3 fF. This is so low, that it can be the capacitance of the gate footprint. A possible reason for the delay resistance can be the charging resistance between the 2 Deg. layers and the buffer. The time constant $C_{\text{del}} - R_{\text{del1}}$ will determine the frequency at which the high frequency and high power limitations start to work. The frequency dependence of the output power can be fine tuned using the capacitance C_{del2}. Both delay capacitors C_{del1} and C_{del2} are quite similar, that is why, for simplicity they can be considered equal. The delay network is shunting the

input capacitance C_{gs}, but the values of $C_{\text{del1}}, C_{\text{del2}}$ are so small that they do not significantly influence the input. This means that the ordinary methods to extract bias dependencies of capacitances C_{gs} and C_{gd} can be used.

Thus, the LS model with a back-gate dispersion model and delay and gate control network will work well for small dissipated power and will describe the frequency dependence of the tuned maximum power and large signal gain accurately. Even a simple linear temperature-dependent model for R_c, R_{del} and C_{del} improves the fit, but a better fit can be obtained if more complicated thermal resistance model is arranged from 2 thermal resistors R_{therm1} and R_{therm2} connected in series. In this case R_{therm1} will describe the overheating occurring in a narrow volume, and R_{therm2} will describe the thermal resistance between the volume in which the power is generated and the heat sink.

The output capacitance C_{ds} will critically influence the output power at high frequency. That is why the reduction of all parasitic capacitances is important if the goal is to create a broadband high power amplifier.

7. Empirical CMOS Model

Similar approach can be used to model CMOS devices, taking into account the specific effects for the CMOS device. For example, the I_{ds} current close to pinch-off gate voltages (i.e., very small currents) is very close to exponential as can be seen from logarithmic plot Figure 21. This means that a corresponding term should be available in the current equation Eqs. (28),(29).

The CMOS devices are inherently symmetric and this means that the symmetric I_{ds} model should be used, but modified for CMOS [55]. If it is very important to have a very good accuracy at small V_{ds}, then it is recommended to use V_{ds} bias dependent P_2 and P_3 as in Eq. (32).

Usually for RF application is not required very high accuracy at small V_{ds} and small currents. If this is important, then the special attention should be paid for the fit at small currents, using the parameter for the exponent λ_1. The number of parameters for I_{ds} is low and most of them can be determined directly from

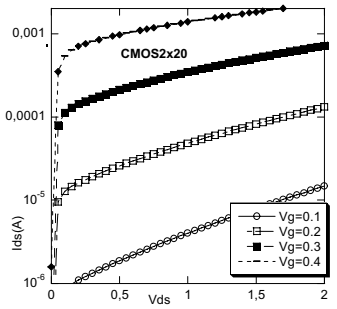


Figure 21. I_{ds} vs. V_{ds} - small current V_{gs} bias.

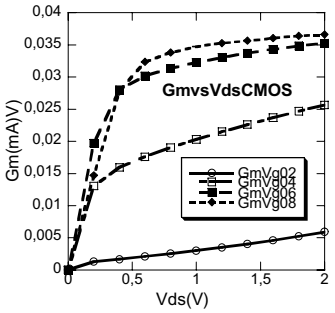


Figure 22. G_m vs. V_{ds} CMOS.

measurements and the remaining parameters are extracted using optimization default CAD tool optimizers.

$$I_{ds} = 0.5(I_{dsp} - I_{dsn})\ldots \tag{12}$$

$$I_{dsp} = I_{pk}(1 + \tanh(\psi_p))(1 + \tanh(\alpha_p V_{ds})) \times (1 + \lambda_p V_{ds} + \lambda_{1p}\exp(((V_{ds}/V_{kn}) - 1))) \tag{33}$$

$$I_{dsn} = I_{pk}(1 + \tanh(\psi_n))(1 + \tanh(\alpha_n V_{ds})) \times (1 - \lambda_n V_{ds} - \lambda_{1n}\exp(((V_{ds}/V_{kn}) - 1))) \tag{34}$$

where $\psi_{p,n}$ are power series functions centered at V_{pk}.

Typically three terms of the power series are enough to produce I_{ds} model accuracy of 2–5%. In a similar way V_{pk} and I_{pk} are the gate voltage and the drain current at which the maximum of the trans-conductance occurs, α_r, α_s are the saturation parameters, and the parameter λ accounts for channel length modulation. Drain voltage dependence of parameters, like V_{pk} and λ is described by Eqs. (15), (33).

The equivalent circuit of the CMOS transistor is much more complicated in comparison with ordinary FET, due to the influence of the bulk. In the small signal EQ Circuit there are multiple parasitic coupling pairs $C_{\text{gbulk}}, R_{\text{gbulk}}, R_{\text{sbulk}}, C_{\text{sbulk}}, R_{\text{dbulk}}$, and C_{dbulk} [55]. These parasitic couplings will affect the FET behavior mainly at RF frequency. The bulk influence at DC and low RF is handled using the backgate approach with parameter K_{bg} in the equation for V_{pk}.

The CMOS capacitances are different from the MESFET and HEMT capacitances. For this reasons the CMOS capacitance model was proposed which track closer the measured dependencies [55], Eqs. (35)–(36):

$$C_{gs} = C_{gsp} + C_{gs0}(1 + V_{gs} + P_{10})/((P_{11} + (V_{gs} - P_{10})^2))^{0.5})(1 + \tanh[P_{20} + P_{21}V_{ds}]) \tag{35}$$

$$C_{gd} = C_{gdp} + C_{gd0}(1 + V_{gd} + P_{40})/((P_{41} + (V_{gd} - P_{40})^2))^{0.5})(1 + \tanh[P_{30} - P_{31}V_{ds}]), \tag{36}$$

The selected functions for C_{gs}, C_{gd} are symmetric with well-defined derivatives. This results in good fit in the S-parameters, and very good convergence behaviour in HB.

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Table of abbreviations

CMOS	complementary MOS
MOS(FET)	metal oxide semiconductor (field effect transistor)
RF	radio frequency
DC	direct current
CAD	computer aided design
MMIC	Monolithic microwave integrated circuit
LSNA	Large signal network analyzer
HB	Harmonic Balance
I-V	current-voltage

Table of symbols

V_{gs}, V_{ds}, V_{gd}	gate-to-source voltage, drain-to-source voltage, gate-to-drain voltage
I_{ds}	drain-to-source current
V_{gsi}, V_{dsi}	intrinsic gate-to-source and drain-to-source voltages
g_m, g_{ds}	transconductance, output conductance
C_{gs}, C_{gd}, C_{ds}	gate-to-source, gate-to-drain, and drain-to-source capacitances
C_{pd}, C_{pg}	access capacitances at the drain and gate, resp.
R_g	gate resistance
R_i, R_{gd}	resistances for the NQS modeling
R_g, R_s, R_d	resistances at the gate, source and drain, resp.
L_g, L_s, L_d	inductances at the gate, source and drain, resp.
Q_g	total gate charge

Q_{gs}	gate-source charge
Q_{gd}	gate-drain charge
$I_{pk}, V_{pk}, \mathrm{Pi}, \alpha_i, \lambda_i,$	drain current fitting parameters

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