Chapter 3

EKV3.0: AN ADVANCED CHARGE BASED MOS TRANSISTOR MODEL

A Design-oriented MOS Transistor Compact Model for Next Generation CMOS

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Abstract: The EKV3.0 MOS transistor compact model addresses the design and circuit simulation of analog, digital and RF integrated circuits using advanced sub-100 nm CMOS technologies. This chapter presents the physical foundation of the charge model, as well as its extensions to account for geometrical effects, gate current, noise etc. The model is compared to data ranging from 0.25 um to 90 nm CMOS generations. A parameter extraction procedure is outlined. EKV3.0 has been developed in the Verilog-A behavioral language for reasons of portability among simulators.

Key words: MOS transistor; compact model; next generation; nanoscale CMOS; weak inversion; moderate inversion; analog/RF circuit design; EKV model; Verilog-A.

1. Introduction

For circuit-level design of CMOS analog and radio frequency integrated circuits (RFICs), the compact MOS transistor (MOST) model is the key “workhorse” enabling the designer to efficiently achieve design goals. Recently, the demand from the circuit design community for highly consistent,

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physics-based and full-featured compact models has increased particularly in view of using sub-100 nm CMOS technologies.

A primary concern for advanced MOST models is its physical basis. The charge-based model approach taken within the EKV model is itself based on a surface-potential analysis. The basic charge modelling approach [3–12] allows physically consistent and accurate modelling of current, terminal charges and noise, without introducing artificial parameters besides the physical parameters of surface potential modeling (e.g. [13, 14]). Besides supporting full circuit simulation, the compact model should however also have an efficient counterpart for circuit design. The development of the EKV model always was driven by the needs of analog IC design [1, 2]. For many circuit applications, even at RF frequencies, operation in weak and particularly moderate inversion may offer a favorable trade-off among power consumption, linearity, matching, noise and bandwidth. The charge-based approach offers suitable expressions for hand-calculation, which a surface-potential only model cannot offer.

For advanced CMOS generations, new effects have appeared which have a significant impact on circuit design, such as undesirable gate tunneling currents, layout-dependent stress effects affecting each device as well as geometrical scaling and many more. Analog circuit design requires particular attention for accurate modelling of transconductances over all bias ranges and geometries [36, 37]. For applications at radio-frequencies (RF), multi-finger device layout is commonly used [27, 30, 33, 35], which combines the above-mentioned effects with the complexity of non-quasistatic (NQS) behavior of the MOS channel [28, 29, 31]: the traditional quasistatic approach for handling the MOS channel is insufficient to accurately account for high-frequency effects. Thermal noise in short-channel transistors is enhanced [34], while at high frequencies, channel thermal noise is capacitively coupled into gate and substrate (induced gate and substrate noise) [32].

The present chapter presents the basic approach taken in the context of the EKV MOST model to implement the above effects. The full-featured EKV3.0 compact MOST model [41–47] for circuit simulation is presented together with its basic list of parameters. Application examples range from 0.25 um to 90 nm CMOS. A parameter extraction procedure is outlined [38–41], and implementation in Verilog-A language [48, 49] is shortly discussed.

2. Ideal Charge-Based Model of the MOS Transistor

2.1. Surface Potential and Inversion Charge Modelling

The total channel charge density Q'_C in an infinitesimal piece of the channel is found by applying Gauss' law,

$$Q'_C = -C'_{OX} \cdot (V_G - V_{FB} - \Psi_S) \quad (1)$$

where Ψ_S is the surface potential, $C'_{OX} = \varepsilon_{OX}/T_{OX}$ the oxide capacitance per unit area, and V_{FB} the flat-band voltage. The bulk depletion charge Q'_B is given by,

$$Q'_B = -\sqrt{2q\varepsilon_{si}N_{\text{sub}}\Psi_S} \tag{2}$$

and ε_{OX} and ε_{si} are the permittivities of silicon and silicon dioxide, respectively. The gate oxide thickness T_{OX} and the substrate doping concentration N_{sub}, together with V_{FB} are the main actual physical parameters describing the MOS technology.

Inversion charge is then expressed as,

$$Q'_I = Q'_C - Q'_B = -C'_{OX} \cdot \left(V_G - V_{FB} - \Psi_S - \gamma\sqrt{\Psi_S}\right) \tag{3}$$

where $\gamma = \sqrt{2q\varepsilon_{si}N_{\text{sub}}}/C'_{OX}$ is the substrate effect parameter. As can be seen in Figure 1, the relation among inversion charge and surface potential at fixed gate voltage is approximately linear. Linearizing the inversion charge versus surface potential provides the inversion charge linearization factor n_q,

$$n_q \equiv \frac{\partial\left(Q'_I/C'_{OX}\right)}{\partial\Psi_S} = 1 + \frac{\gamma}{2\sqrt{\Psi_S}} \tag{4}$$

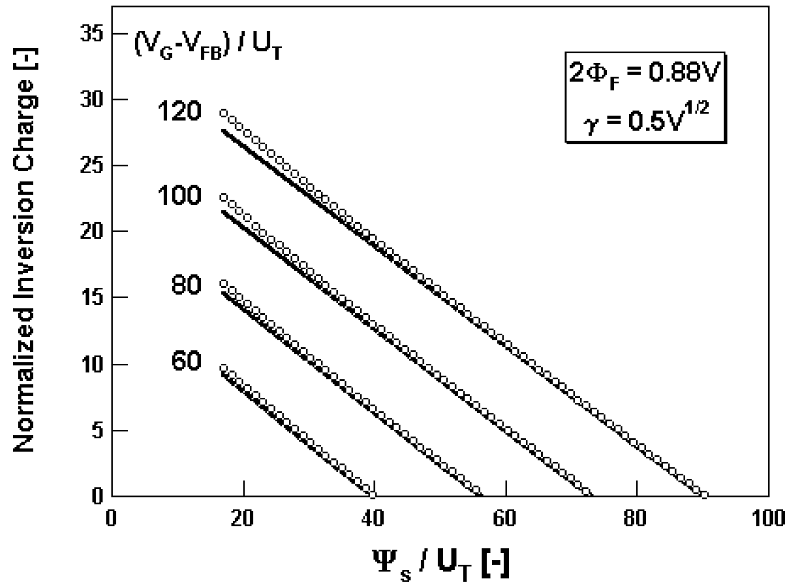

Figure 1. Normalized inversion charge versus surface potential Ψ_S for varied, fixed values of gate voltage V_G. Numerically calculated (markers) and approximation by linearization (lines).

Neglecting, on the other hand, inversion charge density in (3) provides the pinch-off surface potential Ψ_P [5, 10, 12, 15],

$$\Psi_P \equiv \Psi_S|_{Q_I=0} = V_G - V_{FB} + \gamma \cdot \left[\frac{\gamma}{2} - \sqrt{\frac{\gamma^2}{4} + V_G - V_{FB}}\right] \tag{5}$$

We can therefore express the inversion charge as,

$$Q'_I \cong n_q \cdot C'_{OX} \cdot (\Psi_S - \Psi_P) \tag{6}$$

We then define the pinch-off voltage V_P as [12],

$$V_P \equiv \Psi_P - \Psi_0 \quad \text{where} \quad \Psi_0 \cong 2\Phi_F = 2U_T \ln\left(\frac{n_i}{N_{\text{sub}}}\right) \tag{7}$$

where Φ_F is the quasi-Fermi potential and n_i the intrinsic carrier concentration.

A convenient approximation of the pinch-off voltage is [5],

$$V_P \cong \frac{V_G - V_{TO}}{n} \quad \text{where} \quad V_{TO} = V_{FB} + \Psi_0 + \gamma\sqrt{\Psi_0} \tag{8}$$

where n is the slope factor,

$$n \equiv \left[\frac{\partial \Psi_P}{\partial V_G}\right]^{-1} = 1 + \frac{\gamma}{2\sqrt{\Psi_P}} \tag{9}$$

An illustration of pinch-off voltage and slope factor is given in Figure 2.

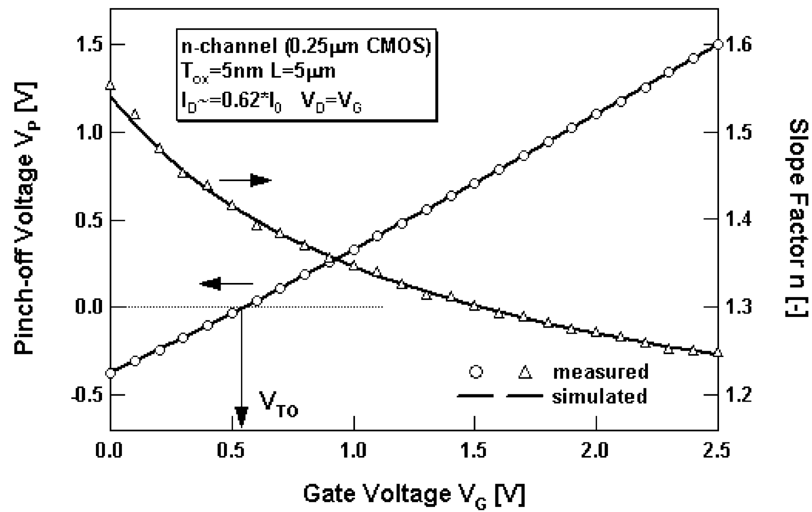

Figure 2. Pinch-off voltage (left axis) and slope factor (right axis) versus gate voltage, measurement and EKV3.0 model.

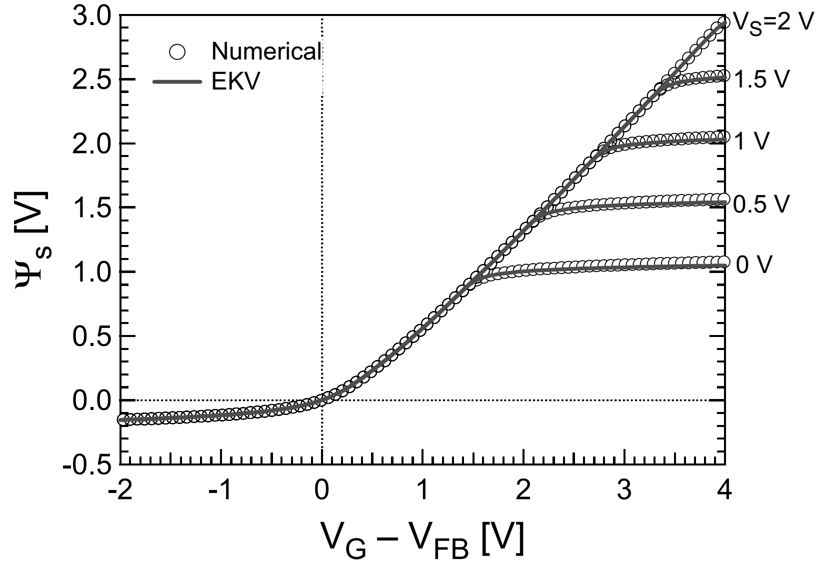

Figure 3. Surface potential Ψ_S versus gate voltage V_G and various values of V_S. The EKV model provides an accurate and continuous approximation to numerically calculated surface potential from accumulation through depletion and inversion.

Note that formally the inversion slope factor n_q and the slope factor n are very close. More detail on the interpretation of both can be found in []. While n_q appears in the normalization quantities for charges and current, the slope factor n is related to the substrate effect and hence they have a different role which needs to be kept separate in the model code for computer simulation. For approximate use in terms of hand calculation, both may be assumed the same.

The surface potential is not used explicitly in the model, but can be recalculated from the charge expressions. Anticipating the further model expressions for accumulation-, depletion- and inversion charge (see next section), Figure 3 shows the result of EKV3.0 modelling of surface potential versus gate voltage and different channel voltages. The model compares well with the numerical solution for the surface potential, and provides continuity through all modes of operation.

2.2. Model for Drain Current

The current transport equation in MOS transistors is written,

$$I_D = \mu \cdot W \cdot \left(-Q_I' \cdot \frac{\partial \Psi_S}{\partial x} + U_T \cdot \frac{\partial Q_I'}{\partial x} \right) \tag{10}$$

where μ is the carrier mobility. Using the charge linearization scheme [3–8, 10],

$$\frac{\partial \Psi_s}{\partial x} \cong \frac{1}{n_q} \frac{\partial Q_i'}{\partial x} \tag{11}$$

allows us to integrate the channel current I_D from source to drain in terms of source and drain inversion charge densities q_s and q_d, respectively [10, 12],

$$I_D = 2 \cdot n_q \cdot U_T^2 \cdot \mu \cdot C_{OX}' \frac{W}{L} \left[q_s^2 + q_s - q_d^2 - q_d \right] \tag{12}$$

Note in the above that the drain current can now be written in symmetric forward and reverse normalized currents i_f and i_r, [5] respectively,

$$I_D = I_{\text{Spec}} \cdot \left[i_f - i_r \right] \begin{cases} i_f = q_s^2 + q_s \\ i_r = q_d^2 + q_d \end{cases} \tag{13}$$

where I_{Spec} is the specific current [5],

$$I_{\text{Spec}} = 2 \cdot n_q \cdot \beta \cdot U_T^2 \quad \text{where} \quad \beta = \mu \cdot C_{OX}' \frac{W}{L} \tag{14}$$

The only missing relationship is the one linking charge to applied voltages. It can be shown that the following relationship among pinch-off voltage, inversion charge density and channel voltage v_{ch} holds throughout the channel [8, 10, 12],

$$v_P - v_{ch} = 2q_i + \ln(q_i) \begin{cases} v_P - v_S = 2q_s + \ln(q_s) \\ v_P - v_D = 2q_d + \ln(q_d) \end{cases} \tag{15}$$

This relationship clarifies the linear relationship among charge and voltage corresponding to strong inversion ($v_P - v_{S,D} > 0$), while the logarithmic relationship results in weak inversion ($v_P - v_{S,D} < 0$). From these relationships, it is easy to derive tables of approximate relationships for drain current and transconductances holding in weak/strong inversion, as well as saturation/non-saturation according to the relations among v_D and v_S.

Note that the above relationship is not analytically invertible to express charge in terms of voltage. This inversion is achieved by an approximation yielding high accuracy and continuity.

2.3. Transconductances

The relationship among transconductance and inversion charge densities at source and drain is immediate [5, 10],

$$\begin{aligned} g_{ms} &= Y_{\text{Spec}} \cdot q_s \\ g_{md} &= Y_{\text{Spec}} \cdot q_d \end{aligned} \quad \text{where} \quad Y_{\text{Spec}} = 2 \cdot n_q \cdot \beta \cdot U_T \tag{16}$$

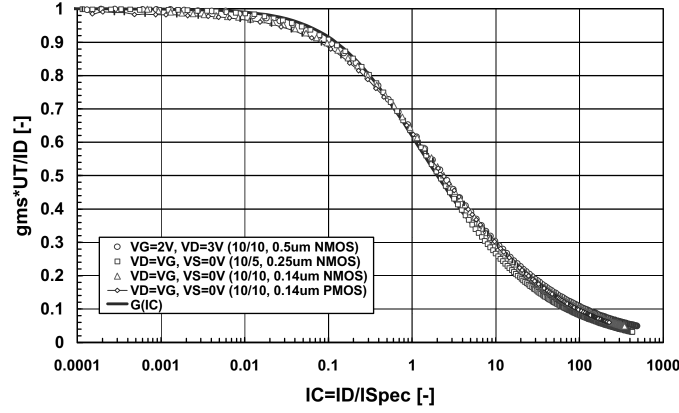

Figure 4. Normalized transconductance versus normalized current, from different NMOS and PMOS transistors from various CMOS technologies.

Noting the relationships among normalized current and charge, the important relationship among transconductance and normalized current is established [7],

$$\frac{g_{ms} \cdot U_T}{I_D} = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_f}} \qquad \frac{g_{md} \cdot U_T}{I_D} = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_r}} \tag{17}$$

Figure 4 shows normalized source transconductance of various transistors versus normalized current in saturation operation, compared to the above theoretical expression. Measurements coincide with the theory for a wide range of different CMOS technologies.

Further interesting relationships among different transconductances can be established [37],

$$g_m = \frac{g_{ms} - g_{md}}{n} \quad \text{and} \quad g_{mb} = \frac{n-1}{n}(g_{ms} - g_{md}) \tag{18}$$

2.4. Integral Charges and Transcapacitances

Integration of local charge densities along the MOS channel provides a means to express the total inversion and depletion charge. Ward's charge partitioning scheme [18] is applied to attribute a part of each channel charge to

either source or drain,

$$Q_I = W \cdot \int_0^L Q'_I(x) \cdot \mathrm{d}x \tag{19}$$

$$Q_D = W \cdot \int_0^L \frac{x}{L} Q'_I(x) \cdot \mathrm{d}x \tag{20}$$

$$Q_S = W \cdot \int_0^L \left(1 - \frac{x}{L}\right) Q'_I(x) \cdot \mathrm{d}x \tag{21}$$

where we note that $Q_I = Q_S + Q_D$. The transcapacitances are then obtained using partial differentiation,

$$C_{XY} \equiv \pm\delta \frac{\partial Q_X}{\partial V_Y} \quad \text{where} \quad \delta = \begin{cases} +1 & X = Y \\ -1 & else \end{cases} \tag{22}$$

An illustration of total gate capacitance, including polydepletion effect (see next section) is shown in Figure 5 versus gate and drain voltage. A notable difficulty is achieving continuous charge and transcapacitance expressions across the flat-band voltage. Further details can be found in [10, 19].

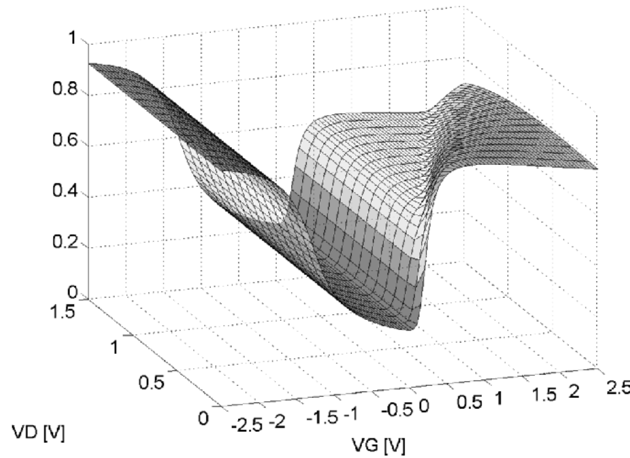

Figure 5. Normalized total gate transcapacitance C_{GG}.versus gate and drain voltages V_G.and V_D, where $V_S = 0$ V. The operating regions cover accumulation (left) to depletion and inversion (right), and linear operation (front) to saturation (back).

2.5. High-Frequency Model

A general model for high-frequency small-signal operation [28, 31]is shown in Figure 6. The three voltage controlled current sources (VCCS) are defined as,

$$\begin{aligned} I_m &= Y_m \cdot (V(gi) - V(bi)) \\ I_{ms} &= Y_{ms} \cdot (V(si) - V(bi)) \\ I_{md} &= Y_{md} \cdot (V(di) - V(bi)) \end{aligned} \tag{23}$$

General relationships hold in all operating regions among transadmittances and admittances,

$$\begin{aligned} Y_m &= \frac{Y_{ms} - Y_{md}}{n} \\ Y_{gbi} &= \frac{n-1}{n}(j\omega \cdot WLC'_{ox} - Y_{gsi} - Y_{gdi}) \\ Y_{bsi} &= (n-1) \cdot Y_{gsi} \\ Y_{bdi} &= (n-1) \cdot Y_{gdi} \end{aligned} \tag{24}$$

The above transadmittances are governed by a bias-dependent critical normalized frequency $\Omega_{\text{crit}} = \omega_{\text{crit}}/\omega_{\text{spec}}$ defined as [28, 31],

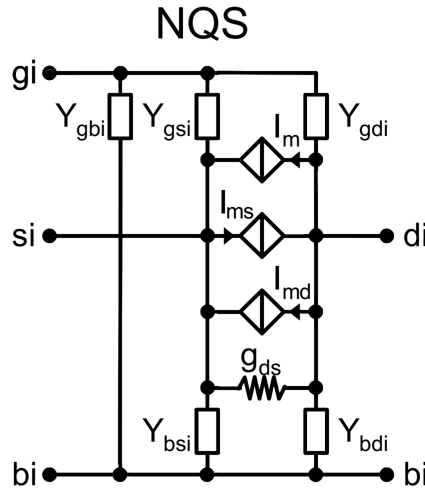

Figure 6. Small-signal equivalent circuit for HF application.

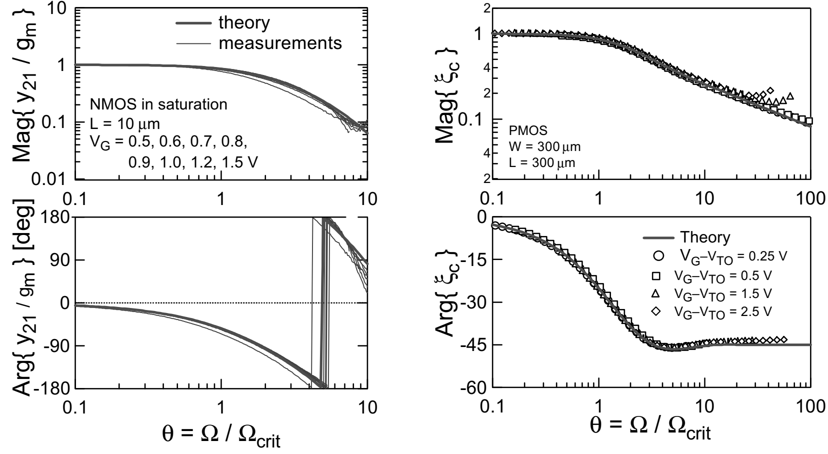

Figure 7. Magnitude and phase of normalized NQS small signal auxiliary functions versus normalized frequency, compared to measurement.

$$\Omega_{\text{crit}} = \frac{30 \cdot (q_s + q_d + 1)^3}{4q_s^2 + 4q_d^2 + 12q_s q_d + 10q_s + 10q_d + 5}$$
$$\Omega_{\text{crit}} = \begin{cases} \frac{15}{2} q_s & SI(sat.) \\ 6 & WI(sat.) \end{cases} \tag{25}$$

where $\omega_{\text{spec}} = \mu U_T / L^2$. The non-quasistatic model reduces to the quasistatic counterpart at lower frequencies, essentially depending on inversion conditions, besides mobility and channel length.

The 3 transadmittances and the 5 admittances depend on two general auxiliary functions, ξ_m and ξ_c, respectively. These are detailed in [28, 31] and further illustrated in Figure 7.

3. Extensions of Charge-Based Modelling Approach

The ideal MOS transistor model framework as presented in the previous section needs to be complemented to account for all imperfections related to high-field effects, high doping concentrations, thin gate dielectric, parasitic capacitances and leakage, series resistance etc. These effects are summarized in Table 1. Several among these will be further presented throughout the following subsections.

Table 1. Effects covered in the EKV3.0 compact MOS transistor model.

"Long-channel"	**"Short-/Narrow channel"**
Polydepletion (PD) effect	Reverse short-channel effect (RSCE)
Quantum mechanical (QM) effect	Inverse narrow width effect (INWE)
PD effect in accumulation in MOS varactors	Source/drain charge sharing
Continuous depletion/accumulation charge/transcapacitances	Drain induced barrier lowering (DIBL)
	Weak inversion slope degradation
Vertical/lateral non-uniform doping	Velocity saturation (variable order) channel length modulation
Vertical field dependent mobility based on effective field including Coulomb, phonon- and surface roughness scattering	Hot-carrier effects on short-channel thermal noise
Output conductance degradation due to pocket/halo implants	2nd order scaling effects
	Matching
NQS effects, consistent large- and small signal approach	**Parasitic effects**
Thermal noise, flicker noise	Bias-dependent series resistance
Induced gate- and substrate noise at NQS conditions.	Bias-dependent overlap & inner fringing charge/capacitance
	Gate tunnelling current
	Gate induced source/drain leakage
	Edge conduction effect

3.1. Polydepletion and Quantum Effects

Depletion in the polysilicon gate and energy quantization of the mobile carriers in the channel drastically reduce the performance of deep submicron CMOS technology. Quantum mechanical (QM) and polydepletion (PD) effects delay the formation of either accumulation or inversion charge with applied gate bias. The most immediately observed changes in device characteristics are increased threshold voltage and decreased gate capacitance, resulting in reduced drain current. Implementation of both these effects has been presented in [15–17].

Polydepletion, resulting from insufficient doping of the polysilicon gate, usually occurs when the MOS channel is inversion for usual type of gate doping, i.e. opposite to the type of channel doping. The EKV3.0 model provides however also the possibility of choosing the same doping type for the gate as for the channel. For further discussion of this point the reader is referred also to the section on overlap charge/capacitance as well as parameter extraction.

3.2. Mobility, Velocity Saturation and Channel Length Modulation

Various scattering mechanisms reduce carrier mobility depending on the field strength, either vertical field, or longitudinal field in the MOS channel. In long-channel MOSTs operating in inversion, the mobility of the carriers is dominated by Coulomb scattering at low vertical field, while phonon scattering dominates at intermediate and surface roughness scattering at high vertical field strength. A convenient way to combine these effects is via the Matthiessen rule,

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{26}$$

where μ_C, μ_{ph} and μ_{sr} correspond to the three respective mobility effects.

Coulomb scattering increases at lower temperatures and higher doping densities, and is therefore important at low-temperature operation and/or with highly doped substrates as in advanced CMOS. Phonon-scattering has a well-known temperature dependence reducing mobility at higher temperatures also in less highly doped MOS channels and intermediate vertical field strength, while surface roughness scattering is only slightly temperature dependent.

Due to the field-dependence of the scattering mechanisms, mobility in the MOS channel is position dependent due to the change in charge density along the channel. An integration along the channel provides the integral mobility of the MOS transistor,

$$\bar{\mu} = \frac{1}{\frac{1}{L}\int_0^L \left[\frac{1}{\mu_C} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}\right] \cdot \mathrm{d}x} \tag{27}$$

where the Coulomb, phonon- and surface roughness scattering limited mobility terms depend on local charges or vertical field $E_{\perp} = \left|Q'_B + \eta Q'_I\right| / \varepsilon_{si}$, respectively, as,

$$\frac{1}{\mu_C} \propto \left[\frac{1}{2} + \frac{\left|Q'_I\right|}{\varepsilon_{si}}\right]^{(-1 \geq \alpha_C \geq -2)} \quad \frac{1}{\mu_{ph}} \propto [E_{\perp}]^{1/3} \quad \frac{1}{\mu_{sr}} \propto [E_{\perp}]^2 \tag{28}$$

The above integration can be carried out resulting in an expression notably depending on inversion charge densities at source and drain. The integral mobility is then used in the drain current expression. As a result, vertical field mobility is naturally dependent not only on gate, but also source and drain voltages, without introducing artificial dependences or parameters. An illustration of the resulting mobility for a long-channel transistor is shown in Figure 8.

In short-channel transistors, velocity saturation is the main effect limiting mobility and therefore available drain current, which is sensible mostly in strong

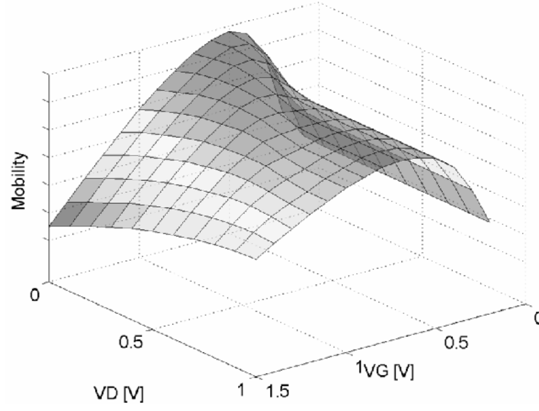

Figure 8. Integral mobility (arbitrary units) versus gate and drain voltage in a long-channel MOST, showing the influence of Coulomb- (low V_G), phonon- and surface roughness (high V_G) scattering, as well as dependence on drain voltage from linear to saturation operation, at $V_S = 0\,\text{V}$.

inversion for velocity saturated conditions. Mobility of the channel carriers is related to drift velocity v_d as,

$$\mu = v_d / E_{II} \tag{29}$$

where $E_{II} = \partial\Psi_s/\partial x$ is the longitudinal field along the channel. The inversion charge linearization vs. surface potential is again conveniently used, $\partial\Psi_s \cong \partial Q_i'/n_q$. A common approach to relate velocity saturation to mobility is the well-known 1st-order hyperbolic model

$$v_d = v_{sat} \frac{E_{II}/E_C}{1 + E_{II}/E_C} \tag{30}$$

where $E_C \cong v_{sat}/\mu_0$ is the critical field for velocity saturation usually considered as a temperature dependent parameter.

The above mobility relationship is easy to handle analytically and is therefore often preferred for simplicity. Theoretically, a 2nd-order velocity-field relationship should be used for electrons. In EKV3.0, a variable-order velocity-field relationship is used as follows,

$$v_d = v_{sat} \frac{E_{II}/E_C}{\sqrt{1 + \frac{[2(2-\delta)\cdot(E_{II}/E_C)]^2}{G + |2(2-\delta)\cdot(E_{II}/E_C)|} + (E_{II}/E_C)^2}} \tag{31}$$

where $1 \le \delta \le 2$ is an adjustable parameter defining the order of the velocity-field-relationship and G is a constant. In Figure 9, the variable-order velocity-field relationship is compared with 1st- and 2nd-order relationships.

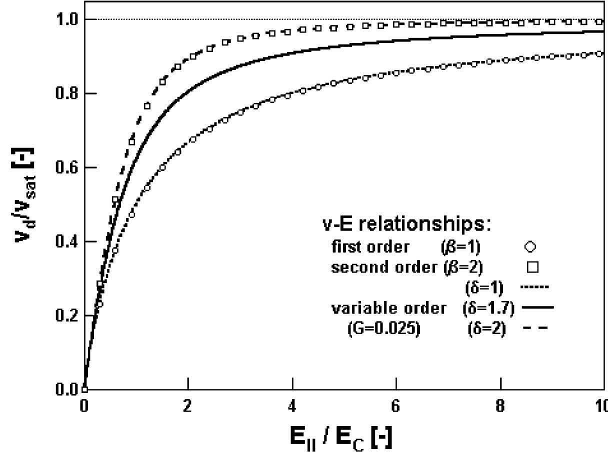

Figure 9. Variable-order velocity-field relationships compared with 1st- and 2nd-order relationships.

The final drain current expression including vertical field and velocity saturation is then,

$$I_D = \frac{2n_q U_T^2 \cdot \bar{\mu}_\perp C'_{OX} \dfrac{W}{L} \left[q_s^2 + q_s - q_d^2 - q_d\right]}{\sqrt{1 + \dfrac{\left[4\varepsilon(2-\delta)\cdot(q_s - q_d)\right]^2}{G + |4\varepsilon(2-\delta)\cdot(q_s - q_d)|} + \left(2\varepsilon\left(q_s - q_d\right)\right)^2}} \tag{32}$$

where $\varepsilon = U_T / L \cdot E_C$. Note that this formulation not only introduces a flexible handling of the degree of velocity saturation, it also responds to the need of correctly handling source-drain symmetry at the point $V_D = V_S$.

Output conductance in short-channel transistors in saturation is dominated by channel length modulation mostly in strong inversion. A quasi-two-dimensional approach is used to model the modulation of the channel length ΔL,

$$\Delta L \cong \lambda \cdot \ln\left(1 + \frac{V_{DS} - V_{DSsat}}{L_C \cdot E_C}\right) \quad \text{where} \quad L_C = \sqrt{\frac{\varepsilon_{si} \cdot X_J}{C'_{OX}}} \tag{33}$$

where X_J is the junction depth and λ the adjustable parameter for channel length modulation. The saturation voltage is related to inversion charge densities,

$$V_{DSsat} = U_T \left[2\left(q_s - q'_d\right) + \ln\left(\frac{q_s}{q'_d}\right)\right] \tag{34}$$

$$q'_d \cong q_s + \frac{1}{2}\left(\frac{1}{\varepsilon} + 1 - \sqrt{\frac{1}{4} + \frac{1}{2\varepsilon}\left(\frac{1}{2\varepsilon} + 1 + 2q_s\right)}\right) \tag{35}$$

Further details of handling CLM in the context of EKV3.0 may be found in [10]. Note that mobility expressions are valid for the part of the channel that is not velocity saturated. In the following, the actual channel length is expressed as $L \rightarrow L - \Delta L$, and in the previous evaluations, the inversion charge density at the saturation point is considered instead of the at the drain as $q_d \rightarrow q_d'$. Precautions are again needed so that no discontinuities are created at $V_D = V_S$.

3.3. Series Resistance

Source and drain series resistance, if handled as distinct elements, cause additional internal nodes and therefore increase simulation time of large circuits. An simple and efficient approach to handle series resistances is to consider their approximate effect on drain current,

$$I_D \cong \frac{I_{D0}}{1 + g_{ms0} \cdot R_S + g_{md0} \cdot R_D} \tag{36}$$

where R_S and R_D are the source and drain resistances, respectively. In the above expression, I_D, g_{ms0} and g_{md0} denote the drain current and source- and drain transconductances evaluated assuming no series resistances are present. The direct relation among transconductances and inversion charge densities $g_{ms} = Y_{\text{Spec}} \cdot q_s$ and $g_{md} = Y_{\text{Spec}} \cdot q_d$ can be conveniently used. Furthermore, since $R \propto \rho_{sh} \cdot L_{\text{dif}}/W$, we obtain,

$$I_D \cong \frac{I_{D0}}{1 + r \cdot q_{s0} + r \cdot q_{d0}} \quad \text{where} \quad r = 2nU_T \mu \rho_{sh} \frac{L_{\text{dif}}}{L} \tag{37}$$

where L_{dif} is the length of the LDD diffusion and ρ_{sh} the sheet resistance.

Besides this simple approach to account internally for series resistance, the model also offers the possibility to add external series resistances, requiring however two additional nodes. The model user has therefore the choice among the more efficient, although less accurate, approach of internally accounting for series resistance, or the external one incurring increased computational effort in large circuits, however providing higher accuracy.

3.4. Short-Channel Effects: DIBL, Charge Sharing, RSCE

In order to control short-channel effects in ultra-deep submicron CMOS, halo or pocket implants are commonly used, as is illustrated schematically in Figure 10. Commonly used techniques are Shallow trench isolation, halo or pocket implants near source and drain to control short-channel effects, salicided gate and junction areas and possibly nitrided oxides to reduce gate current.

Drain induced barrier lowering (DIBL), charge sharing and reverse short-channel effect (RSCE) are the main effects dominating weak inversion operation. In Figure 11 the effect of an increasing longitudinal field on the surface

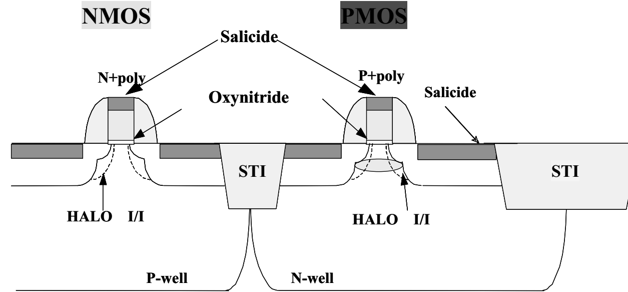

Figure 10. Schematic cross-section of short-channel NMOS and PMOS transistors in an advanced CMOS technology using shallow trench isolation (STI), oxynitride gate oxide, halo implantation near source/drain, and salicided gate and junction areas.

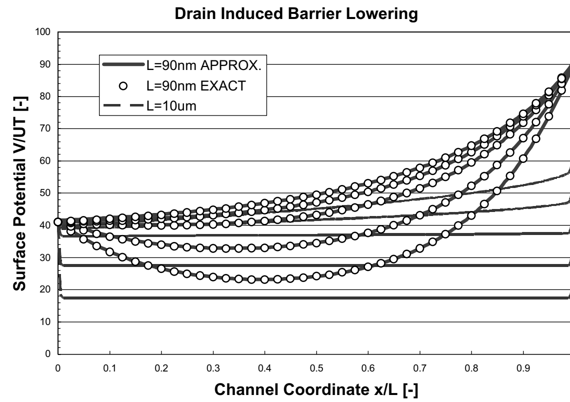

Figure 11. Drain induced barrier lowering effect on surface potential, along the channel, for a long- (lines) and a short-channel (markers and lines) transistors, for fixed V_S and V_D and increasing values of V_P.

potential distribution along the channel can be observed. While the drain voltage has practically no incidence on the surface potential for a long transistor, a short channel transistor is affected significantly by the drain. A quasi-two-dimensional solution of the field distribution near the drain leads to the expression used in EKV3.0.

The DIBL effect is governed by a characteristic length, L_0,

$$L_0 = \eta_D \cdot \sqrt{\frac{\varepsilon_{si} \cdot \gamma}{q \cdot N_{\text{sub}}} \sqrt{\Psi_0}} \tag{38}$$

where $\eta_D \cong 1$ is the main parameter for DIBL. Note the other implicit dependences of L_0 on N_{sub} and C'_{ox}, as well as temperature via Ψ_0 – since the latter

decreases with increased temperature, DIBL tends to have less influence at higher temperature and vice versa.

The estimated difference $\Delta\Psi_S$ of minimum surface potential in the short-channel case, due to DIBL, with respect to the long-channel case, is proportional to,

$$\Delta\Psi_S \propto e^{\left(-\frac{1}{2}\frac{L}{L_0}\right)} \tag{39}$$

and is therefore exponentially dependent on channel length. Note that the exponential is bias-independent and therefore can be evaluated once for each channel length. The $\Delta\Psi_S$ shift is itself approximated by an equivalent shift of the pinch-off voltage $\Delta V_P \approx \Delta\Psi_S$.

The combination of DIBL, charge-sharing and reverse short-channel effect in EKV3.0 gives good results for threshold voltage modelling over channel lengths, as can be seen in Figure 12. Results of threshold voltage modelling

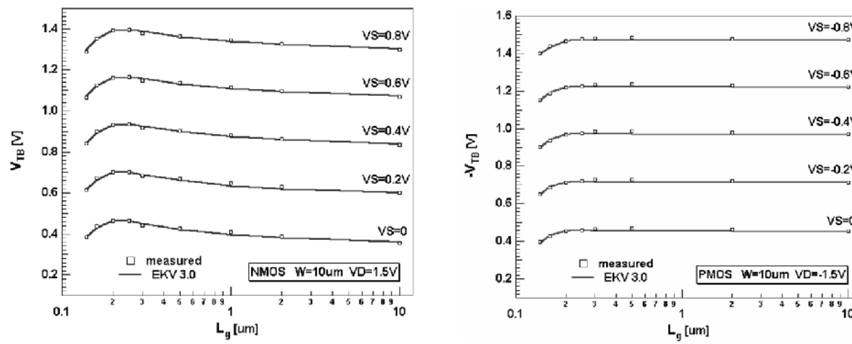

Figure 12. Combined DIBL, charge-sharing and reverse short-channel effect modelling of threshold voltage in 0.14 um CMOS.

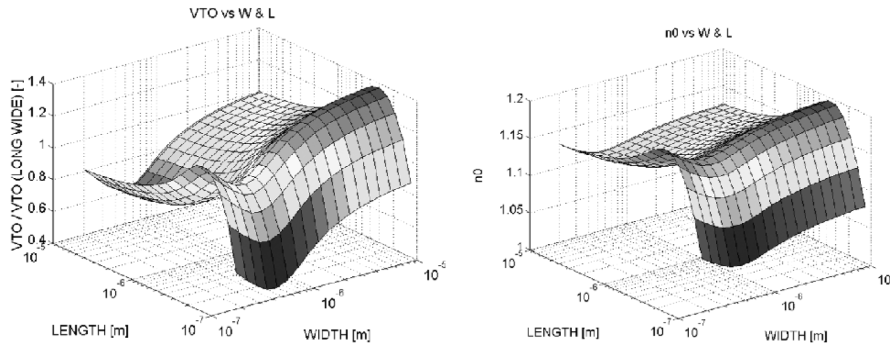

Figure 13. Threshold voltage – relative to long/wide channel – and slope factor n versus channel length and width. Parameter values are realistic for NMOS transistors of an 0.12 um technology.

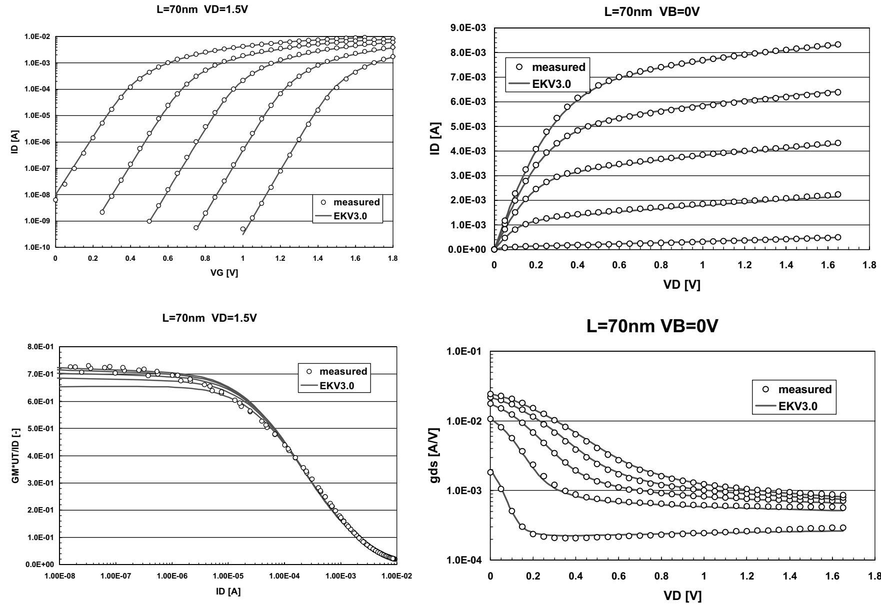

Figure 14. Weak inversion characteristics (left) of a 70 nm n-channel transistor in saturation. The EKV3.0 model provides accurate modelling of weak inversion slope, and transconductance-to-current ratio *versus* normalized drain current. Output characteristics (right) for the same transistor, measurements and modeled with EKV3.0.

for NMOS and PMOS transistors over channel length of an 0.14 um CMOS technology is shown.

The combined short-and narrow-channel effects on threshold voltage and slope factor n are further illustrated in Figure 13. Both characteristics are notably influenced by RSCE and short-channel roll-off mainly due to DIBL and charge sharing. In the width dimension, note the influence of INWE.

In the following, drain current characteristics and related transconductance and output conductance are presented in Figure 14 for an NMOS transistor with effective channel length of 70 nm. These characteristics are all very strongly dependent on DIBL, most notably in weak-moderate inversion.

In order to illustrate these short-channel effects further, Figure 15 shows normalized gate and source transconductance for long- and short-channel transistors of an 0.14 um CMOS technology. Overall the EKV3.0 model represents all characteristics very well. Note that the gate transconductance-to-current ratio in weak/moderate inversion is almost unaffected by channel length, due to a compensating effect among charge sharing (reducing the substrate effect and hence improving weak inversion slope) and DIBL (deteriorating the weak inversion slope).

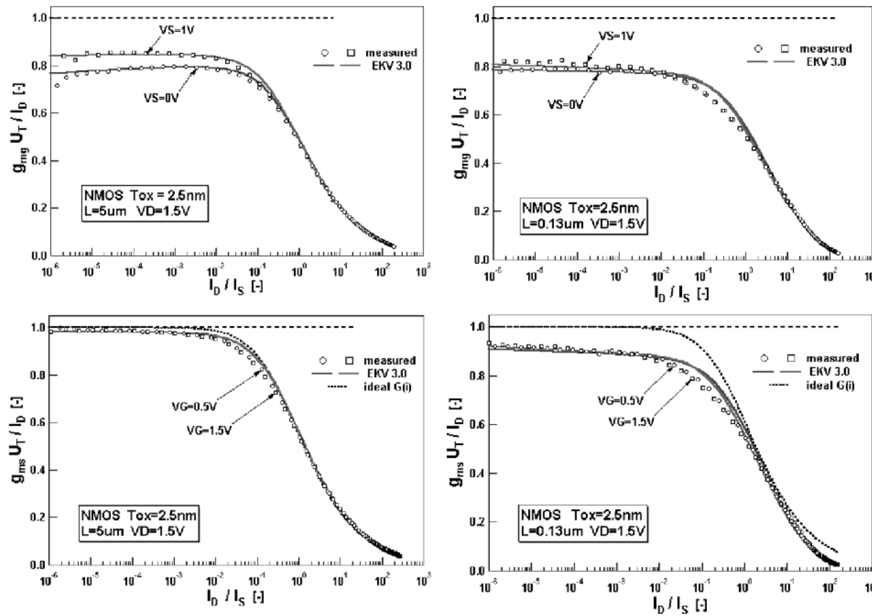

Figure 15. Gate (top) and source (bottom) transconductance to current ratio *versus* normalized drain current, for long-channel (left) and short-channel (right) transistors in 0.14 um CMOS. DIBL effect is responsible for a reduction of g_{ms} in weak inversion for the short-channel transistor.

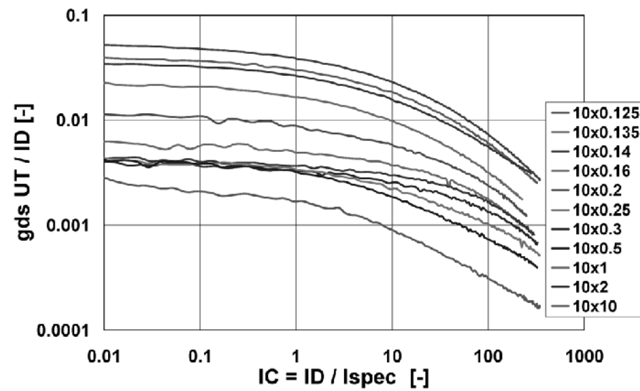

Figure 16. Normalized output conductance-to-current ratio in 0.14 um CMOS. Note that normalized output conductance, instead of improving with longer channels, remains stable or even deteriorates with longer channel lengths (0.3–2 um) in moderate/weak inversion.

Finally, Figure 16 shows normalized output conductance to current ratio versus normalized current for the same technology. It would be expected that normalized output conductance should improve steadily with longer channel lengths. This can be seen not to hold for some intermediate channel lengths,

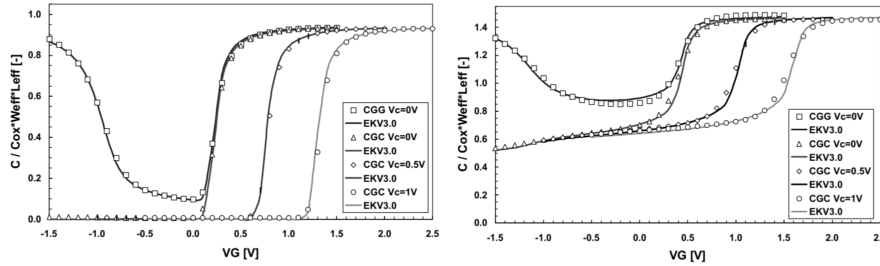

Figure 17. Long- and short-channel NMOS CV characteristics from 0.12 um CMOS, normalized to $C'_{ox}WL$, versus gate voltage, for different channel voltages.

where normalized output conduction to current ratio even deteriorates. This is attributed to the presence of pocket or halo doping implants, degrading output conductance at longer channel lengths.

3.5. Overlap and Fringing Capacitances in Advanced CMOS

Long- and short-channel CV characteristics of an 0.12 um CMOS process are illustrated in Figure 17. Note the correct fitting of all capacitances simultaneously, as well as good fitting of the crucial overlap capacitances in the short-channel characteristics. The latter contribute close to 45% of the total capacitance in (strong) inversion. Overlap and inner fringing capacitances are formulated as charges – preferred over capacitances [25], which are added to the intrinsic channel charges. Note that the overlap capacitances may themselves be affected by polydepletion – just as for MOS varactors in accumulation – when the channel is inverted.

For fringing charge/capacitances, an approach similar to [26] is used. This allows to improve inversion related capacitances in moderate inversion and at the onset of strong inversion significantly as illustrated in Figure 17.

3.6. High-Frequency Application of EKV3.0

One requirement for high-frequency circuit simulation is the consistency among small-signal AC and large-signal transient simulation. While the NQS model presented in the previous section is attractive for its analytical simplicity and its capacity to provide insight in the physics of high-frequency operation of a MOST, it does not provide a solution for transient large-signal simulation.

A convenient approach to solve this problem is the dividing the intrinsic MOS channel into segments as is shown in Figure 18. A number of N channel

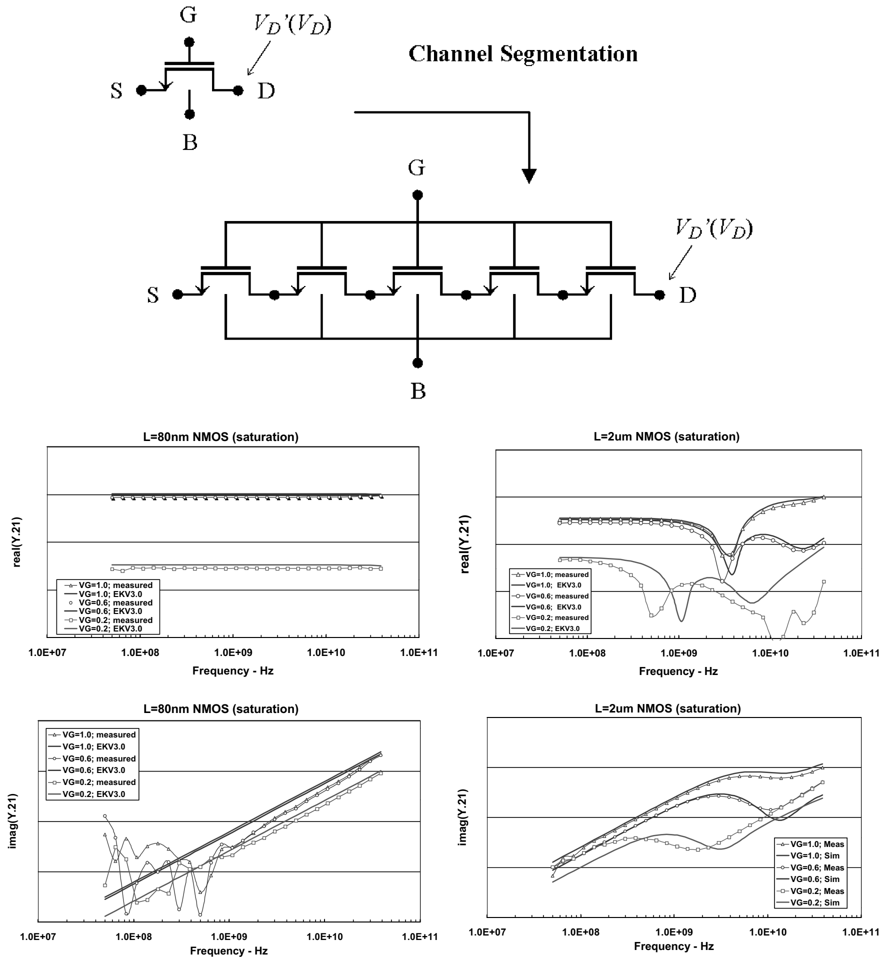

Figure 18. Principle of channel segmentation for consistently handling non-quasistatic (NQS) large-signal and small-signal effects. Real and imaginary part of Y21 for short ($L = 80$ nm, left) and long ($L = 2$ um, right) channel multifinger NMOS transistors operating in saturation and at 3 different gate voltages up to 40 GHz. A qualitatively excellent result is achieved by EKV3.0 with 5 channel segments up to very high frequencies.

segments having an individual length of L/N replace a single transistor with channel length L. This was similarly used in former Philips' models (MM11). A requirement is that the segmented-channel transistor should give the same static and quasistatic response. This can indeed be achieved in the following manner: the mobility of the MOS transistor is calculated for the entire channel, just as if no channel segments existed. Velocity saturation is applied only to the rightmost transistor at the end of the segments chain. For each intermediate

node, only the charge densities need to be evaluated to compute the total charges within each segment.

Figure 18 also presents results on using the above NQS model for small-signal RF modelling with the example of gate transadmittance Y21 in 90 nm CMOS. In the short-channel transistor NQS effects are not visible, while a 2 um transistor shows very significant influence of NQS effects. In the present case, EKV3.0 with 5 channel segments was used. The user may choose the number of segments freely from 1 to 10, according to his/her needs in terms of accuracy.

3.7. Further Aspects Accounted for in EKV3.0

It should be noted that further aspects are included in the EKV3.0 MOS compact model but were not further detailed in the present work. Among these, the following effects should be specially noted:

- Gate tunneling current. The inversion charge linearization principle is extended to account for tunneling through thin oxides. This becomes very significant in 90 nm CMOS technologies and below.
- Substrate current.
- Induced noise in gate and substrate [32].
- Hot-carrier, velocity saturation, mobility and CLM effects on short-channel thermal noise [34].
- Edge conduction effects, resulting from shallow trench isolation.
- Gate and substrate parasitics network for RF application, scaling of parasitics with number of fingers for RF-layout.
- Device matching parameters.
- Temperature effects.

Furthermore, the model is completed with complete sets of extrinsic elements equations, for gate-induced drain/source leakage, diode junction currents and capacitances, according to the BSIM4 model.

In future releases of the model, it is expected that the following effects will be made available:

- Layout-dependent stress effects.
- Matching for gate current.

3.8. Parameters and Principles of Parameter Extraction

Table 2 provides a synoptic overview of the main parameters of EKV3.0. The parameters, written in SPICE syntax, are grouped according to their role (compare with Table 1), and include indicative and/or default values, with

Table 2. List of main parameters (∼ 90) in EKV3.0 with indicative values. Parameters for 2nd order scaling (∼ 30), extrinsic elements (diodes, gate induced drain leakage, series resistance) are not included.

• Flags	• Vsat & CLM par.	• Overlap & fringing
+ SIGN = 1	+ UCRIT = 5.0E+6	+ LOV = 10.0E-9
+ TG = -1	+ DELTA = 1.5	+ GAMMAOV = 2.5
• Scale parameters	+ LAMBDA = 0.5	+ VFBOV = 0.0
+ SCALE = 1.0	+ ACLM = 0.83	+ KJF = 0.0
+ XL = 0.0	• Geometrical par.	+ CJF = 0.5
+ XW = 0.0	+ DL = 0.0	• Gate current
• Cgate parameters	+ DLC = 0.0	+ KG = 30.0E-6
+ COX = 10.0E-3	+ WDL = 0.0	+ XB = 3.1
+ GAMMAG = 6.0	+ LL = 0.0	+ EB = 29.0E+9
+ AQMA = 0.5	+ LLN = 1.0	+ LOVIG = 20.0E-9
+ AQMI = 0.4	+ DW = -10.0E-9	• Substrate current
+ ETAQM = 0.75	+ DWC = 0.0	+ IBA = 100.0E+6
• Nch. parameters	+ LDW = 0.0	+ IBB = 300.0E+6
+ VTO = 200.0E-3	• Charge sharing	+ IBN = 1.0
+ PHIF = 450.0E-3	+ LETA0 = 0.0	• Edge device cond.
+ GAMMA = 300.0E-3	+ LETA = 1.0	+ WEDGE = 10.0E-9
+ VBI = 1.0	+ LETA2 = 0.0	+ DGEDGE = 30.0E-3
+ XJ = 20.0E-9	+ WETA = 1.0	+ DPEDGE = 20.0E-3
+ NO = 1.0	+ NCS = 1.0	• Temperature par.
• Mobility	• DIBL	+ TNOM = 27.0
+ KP = 300.0E-6	+ ETAD = 1.0	+ TCV = 500.0E-6
+ E0 = 1.0E+9	+ SIGMAD = 1.0	+ BEX = -1.5
+ E1 = 400.0E+6	• RSCE	+ TE0EX = 0.0
+ ETA = 0.5	+ LR = 40.0E-9	+ TE1EX = 1.5
+ ZC = 1.0E-6	+ QLR = 2.5E-3	+ TETA = 6.0E-3
+ THC = 0.0	+ NLR = 100.0E-3	+ UCEX = 0.8
• Long-ch. gds degr.	+ FLR = 0.0	+ TLAMBDA = 0.0
+ PDITS = 0.0	• INWE	+ IBBT = 0.0
+ PDITSD = 0.0	+ WR = 60.0E-9	+ TCVL = 0.0
+ PDITSL = 0.0	+ QWR = 2.0E-3	+ TCVW = 0.0
+ FPROUT =10.0E+6	+ NWR = 50.0E-3	+ TCVWL = 0.0
+ DDITS = 0.3	• Series resistance	• Flicker noise
• Matching par.	+ RLX = 50.0E-6	+ AF = 1.0
+ AVTO = 0.0	+ LDIF = 100.0E-9	+ KF = 1.0E-24
+ AKP = 0.0		+ EF = 2.0
+ AGAMMA = 0.0		

typical values for an 0.12 um CMOS technology. The reader is cautioned that this list is not exhaustive and that parameter names might slightly differ in the actual computer simulation model.

A few comments on the parameters are in order here. NMOS and PMOS transistors have the same parameter set, with same signs of parameters except for the flag `SIGN=1` which denotes an NMOS transistor, and `SIGN=-1` a PMOS. The type of the gate can be chosen opposite to the channel as usual for

enhancement type transistors with `TG=-1` (e.g. N+ poly for p substrate), while `TG=1` denotes similar type of gate as the channel. The latter may be used e.g. for modeling of MOS varactors, which present polydepletion effect when the channel is accumulated. The scale of parameters (e.g. meter per default, or micrometer) may be chosen with `SCALE`.

In Figure 19, a flowchart for the extraction of the main parameters of EKV3.0 is presented. For simplicity, higher-order effects have been omitted. A set of less than 25 parameters is sufficient to represent current-voltage and capacitance-voltage characteristics over channel length for one type of transistor. It should be noted that such a rough hand parameter extraction can be done even by a non-expert user. Model users of former versions, e.g. EKV2.6, will find many similarities with the formerly existing model. Once a rough set of parameters is obtained including length scaling, refinements need to be done for narrow width effects, combined short/narrow channel effects and temperature. Further details of parameter extraction are described e.g. in [38–41]. If necessary, 2nd order scaling of parameters with geometry can be used to improve the overall fitting over geometry.

3.9. Implementation in Verilog-A, ADMS and Diffusion of C-code

The EKV3.0 model has been fully coded in Verilog-AMS [49] and was tested in several circuit simulators (ADS, ELDO, Spectre). Model implementation

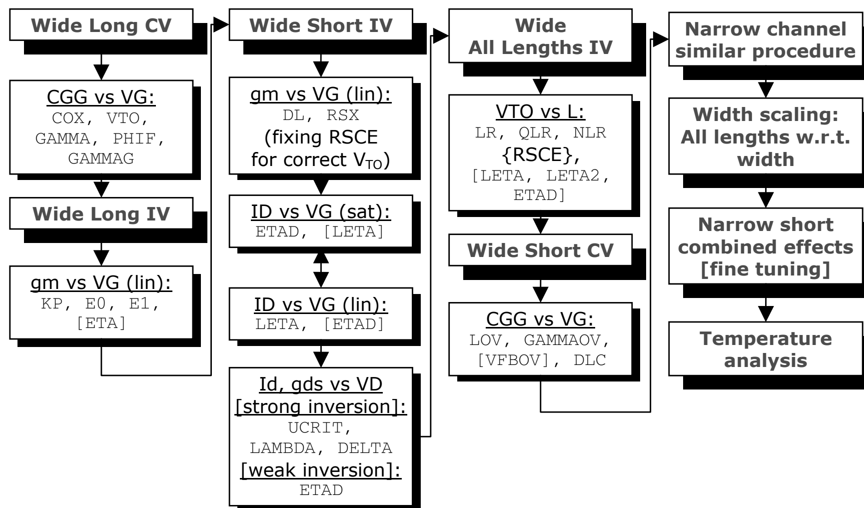

Figure 19. Extraction flowchart showing a possible sequence of basic parameter extraction for EKV3.0 model.

in a Verilog-AMS to C code converter, called ADMS [47], has been completed at the time of writing this chapter. This allows generation of executable C-code for simulators for which XML interfaces in ADMS exist. Notably, SPICE3F5 of UC Berkeley, but also commercial simulators among which Cadence's Spectre, and Synopsys' HSPICE. Further implementations, such as direct C-code implementations in Xpedion's GoldenGate and Mentor Graphics' ELDO are either completed or nearing completion at the time of writing. Therefore, the EKV3.0 code is being made widely available to the community.

4. Conclusions

In summary, this chapter presents aspects of the EKV3.0 model formulation to address modelling of sub-100 nm CMOS. Basics of model formulation, namely the charge-based approach to MOST modelling, have been presented. This provides a consistent approach to model static, quasistatic, non-quaistatic and noise properties of the ideal long-channel MOS transistor. One advantage of the inversion charge linearization model lies in its high analytic versatility. It is therefore particularly suited to advanced analog design. Model extensions to account for high-field effects in advanced CMOS have been outlined and modelling results on various CMOS technologies ranging from 0.25 um to 90 nm CMOS presented.

EKV3.0, with approximately 90 main parameters, accounts for most geometrical, bias and parasitic effects observed in sub-100 nm CMOS technologies. Moreover, the model can be used with a rather small subset of parameters and included effects while leaving others inactive. This facilitates learning as well as teaching, therefore making the model more easily accessible. EKV3.0 is being made available to a wide community for analog/RF circuit design.

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