Chapter 2

PSP: AN ADVANCED SURFACE-POTENTIAL-BASED MOSFET MODEL

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Abstract: PSP is the latest and the most advanced compact MOSFET model. It was developed by merging and enhancing the best features of the two surface-potential-based models SP (developed at The Pennsylvania State University) and MOS Model 11 (developed by Philips Research). PSP has been selected as a new industry standard for the next generation compact MOSFET model by the Compact Modeling Council. This chapter presents the main ideas enabling the development of PSP, the model structure and its general features.

Key words: compact model; MOSFET; surface potential; PSP, JUNCAP2.

1. Introduction

In computer-aided design of integrated circuits, compact models are used to reproduce electrical characteristics of semiconductor devices. These models describe the device behavior as a function of bias conditions, temperature, device geometry and process variations. For IC-design in CMOS, compact MOSFET models are a critical link in the translation of CMOS process properties into IC performance. In the IC-industry, state-of-the-art compact MOS

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models in the public domain such as BSIM3 [1], BSIM4 [1] and MOS Model 9 (MM9) [2], are widely used. With the continuous down scaling of CMOS technologies, however, the demands for compact MOS models have become more and more stringent:

- As the supply voltage is scaled down, the moderate inversion region becomes an increasingly larger fraction of the maximum voltage swing. An accurate, physical description of moderate inversion becomes essential, and it can be most easily obtained by the use of surface-potential-based models.
- Modern CMOS technologies are suitable for digital, analog as well as RF applications. The compact model should thus be accurate for digital, analog and RF circuit design. This implies that the model should, amongst others, provide Gummel drain-source symmetry and give an accurate description of distortion behavior.
- The model should accurately describe all the important physical effects of contemporary and future CMOS technologies.

State-of-the-art models such as BSIM4 and MM9 are based on threshold voltage formulations, so-called threshold-voltage-based models, and they fail to fulfil some or all of the above requirements for advanced modeling. This deficiency has presently resulted in a wide consensus in the compact modeling community that traditional threshold-voltage-based models have reached the limit of their usefulness and need to be replaced with more advanced models based on surface potential ψ_s or inversion charge density q_i formulations [3], referred to as surface-potential-based or inversion-charge-based models[1], respectively. The development of the SP model at The Pennsylvania State University [4–17] and MOS Model 11 (MM11) at Philips Research [18–26] has followed the ψ_s-based approach. This approach provides for a physics-based modeling of all regions of operation (including the moderate inversion and the accumulation region) and avoids making additional approximations beyond those already inherent in the charge-sheet models. While the constitutive equation of q_i-based models such as ACM, EKV and BSIM5 [3] can be derived differently, in the final analysis it follows from the equation for surface potential introducing several extra approximations [4]. In addition the ψ_s-based approach, as opposed to the q_i-based approach, enables the physical modeling of the source-drain overlap regions where the inversion charge is not a particularly suitable variable.

The ψ_s-based approach to modeling MOS transistors dates back to the Pao-Sah model [27]. The modern ψ_s-based models are based on the charge-sheet model (CSM) of Brews [28]. Despite the clear physics and the ability to

[1] Here we use the model classification suggested in [4].

provide a single expression for all regions of operation [29] ψ_s-based models did not become popular until the last decade due, in part, to their perceived complexity. Successful ψ_s-based models became possible only after significant progress was made in the techniques for computing the surface potential, simplification of the charge equations relative to the original formulation and the introduction of small-geometry effects. The implementation of these advances and the overall model structures of SP [4] and MM11 [22] turned out to be compatible, enabling the merger of both models into a single new model called PSP that combines and enhances the best features of SP and MM11. This chapter provides an overview of PSP.

The PSP core model contains an intrinsic and an extrinsic model. The intrinsic model describes the electrical behavior of the channel region of the MOSFET, and includes expressions for the drain-source channel current and the quasi-static (QS) terminal charges. The extrinsic model describes the electrical behavior of the gate overlap regions of the MOSFET, and contains expressions for the substrate current, the gate current and the gate overlap and fringing capacitances. PSP also includes a noise model which describes the (intrinsic and extrinsic) noise sources. In addition, PSP provides for two support modules: a new junction model named JUNCAP2 [30] and the non-quasi-static (NQS) module [8, 15, 31].

Both MM11 and SP distinguish between local and global model parameters. This approach is carried over to PSP. Global parameters include geometry dependencies and before evaluating the MOSFET output characteristics they are converted into a small number of local parameters actually used in the core model. The use of local parameters facilitates the model parameter extraction, as one can extract the local parameters for each device geometry separately and then use scaling equations to obtain the global parameters for the relevant range of geometries.

The major features of PSP include the following.

- Physical ψ_s-based formulation of both intrinsic and extrinsic models
- Physical and accurate description of the accumulation region
- Symmetrical linearization enabling accurate modeling of ratio-based circuits (e.g., R2R circuits)
- Gummel symmetry
- Coulomb scattering and non-universality in the mobility model
- Non-singular velocity-field relation enabling the accurate modeling of RF distortion
- Quantum-mechanical corrections
- Correction for polysilicon depletion effects
- Inclusion of all relevant small geometry effects
- modeling of halo implant effects, including the output conductance degradation in long devices

- GIDL/GISL model
- Surface-potential-based noise model including flicker noise, and partly correlated channel thermal noise and channel-induced gate noise.
- Advanced junction model including Shockley-Read-Hall generation/recombination, trap-assisted tunneling and band-to-band tunneling
- Spline-collocation-based NQS model including all terminal currents
- STI-induced stress model

This chapter aims at giving a derivation and physical description of the most important equations used in PSP. Limited space, however, does not allow for discussing all the features included in PSP in detail. For a complete overview of all equations and parameters, the reader is referred to the PSP documentation as can be found on the internet [32]. In Section 2, we will first discuss the intrinsic model, followed by a discussion of the extrinsic model in Section 3. Next, the noise model, the junction diode model and the non-quasi-static model will be treated separately in Sections 4, 5 and 6, respectively. Finally, we will conclude in Section 7.

2. Intrinsic Model

The intrinsic model contains expressions for the drain-source current and the terminal charges. These electrical quantities can be most easily written in terms of the surface potential, hence we start with a discussion of the surface potential in Section 2.1. Next, an approximate method to include two-dimensional effects important for small-geometry devices, the lateral field gradient factor, is treated in Section 2.2. The drain current and the intrinsic charges will be discussed in Sections 2.3 and 2.4, respectively.

2.1. Surface Potential

The surface potential ψ_s is the most natural variable for the formulation of MOS device physics. It is defined as the difference between the electrostatic potential at the SiO_2/Si interface and the potential in the neutral bulk region due to band bending, see Figure 1 (a). Assuming an ideal gate (i.e., neglecting the poly-depletion effect), ψ_s is found using the following derivation [27, 33].

In the p-type substrate, the Poisson equation for the electrostatic potential ψ (with respect to the neutral bulk) is written as:

$$\frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y^2} = -\frac{\rho(x,y)}{\epsilon_{\mathrm{Si}}} = q \cdot \frac{N_{\mathrm{SUB}} + n(x,y) - p(x,y)}{\epsilon_{\mathrm{Si}}} \tag{1}$$

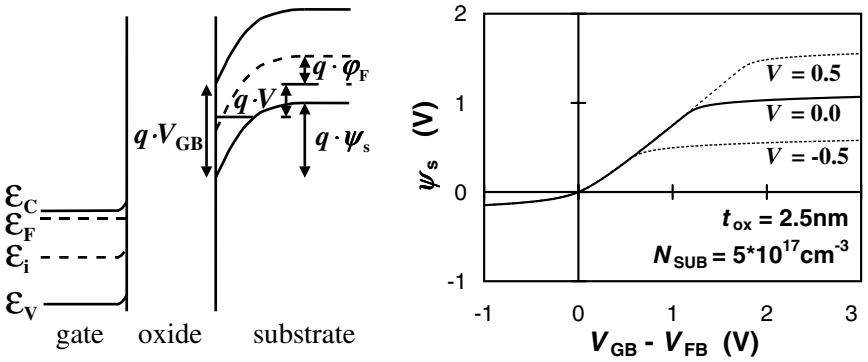

Figure 1. (a) The energy-band diagram (in transversal direction) of an n-MOSFET for $V_{GB} > V_{FB}$, where V_{FB} is the flat-band voltage, ψ_s is the surface potential, V is the difference between electron and hole quasi-Fermi potentials, and ϕ_F is the intrinsic Fermi-potential ($\phi_F = \phi_T \cdot \ln(p_b/n_b)$). (b) The surface potential as a function of gate bias for different values of quasi-Fermi potential V as calculated from (3).

where x and y are the transversal and lateral coordinates, respectively, ρ is the space charge, and N_{SUB} is the net acceptor doping concentration. The electron and hole density, n and p, are given by Maxwell-Boltzmann statistics:

$$\begin{aligned} n(x,y) &= n_b \cdot \exp\left(\frac{\psi(x,y)-V(x)}{\phi_T}\right) \\ p(x,y) &= p_b \cdot \exp\left(-\frac{\psi(x,y)}{\phi_T}\right) \end{aligned} \tag{2}$$

where n_b and p_b denote the electron and hole concentration in the neutral bulk, respectively, ϕ_T ($= k \cdot T/q$) is the thermal voltage, and $V(x)$ denotes the difference between electron and hole quasi-Fermi potentials. This so-called channel voltage $V(x)$ ranges from V_{SB} at the source side ($y = 0$) to V_{DB} at the drain side ($y = L$). Charge neutrality in the bulk sets $N_{\mathrm{SUB}} = p_b - n_b$. In order to obtain an approximate analytical solution of (1), the impact of the lateral field gradient is neglected, i.e., it is assumed that $\partial^2\psi/\partial y^2 \ll \partial^2\psi/\partial x^2$. This is commonly refered to as the gradual channel approximation (GCA). Next, the surface potential ψ_s can be obtained using the first integral of the 1-D Poisson equation and applying Gauss' theorem at the SiO_2/Si interface, where both ψ and $\partial\psi/\partial y$ are taken to be equal to zero deep in the neutral bulk. The resulting equation is the so-called surface potential equation (SPE), which provides ψ_s as an implicit function of the terminal voltage V_{GB} and

the channel voltage V:

$$\left(\frac{V_{GB} - V_{FB} - \psi_s}{\gamma \cdot \sqrt{\phi_T}}\right)^2 = \exp(-u) + u - 1 + \frac{n_b}{p_b} \cdot k_n \cdot \left[\exp(u) - m(u)\right] \tag{3}$$

Here, γ is the body factor given by $\sqrt{2 \cdot q \cdot \epsilon_{\mathrm{Si}} \cdot N_{\mathrm{SUB}}}/C_{ox}$, V_{FB} is the flat-band voltage, $u = \psi_s/\phi_T$, and $k_n = \exp(-V/\phi_T)$. Following the above derivation, the term $m(u)$ is equal to $1 + u/k_n$. Using (3), the surface potential at the source side (ψ_{ss}) and at the drain side (ψ_{sd}) are given implicitly by setting V equal to V_{SB} and V_{DB}, respectively, see Figure 1 (b). It should be pointed out here that the SPE is not only the basis of ψ_s-based models, but also forms the basis of threshold-voltage-based models [33] and inversion-charge-based models [4].

In the SPE, the term $m(u)$ merely affects the $\psi_s(V_{GB}, V)$ dependence in a narrow region near flat band. Nevertheless, the above specific form of $m(u)$ is problematic very near the flat-band voltage where it results in a negative right-hand side of (3) [34]. This has been traced in [14] to the variation of the electron carrier quasi-Fermi potential across the space charge layer[2] neglected in the original formulation [27]. Several different empirical forms of $m(u)$ have been proposed in literature [7, 14, 17, 34] to provide well-conditioned SPE in all regions of operation. In PSP, the expression for $m(u)$ developed for SP-SOI [17] is adopted:

$$m(u) = u + 1 + \frac{u^2}{u^2 + 1} \tag{4}$$

This expression has the following advantages: *(i)* in contrast to [27], it ensures that the right-hand side of (3) is always positive, *(ii)* in contrast to [34], it ensures that $\partial\psi_{ss}/\partial V_{GB} = \partial\psi_{sd}/\partial V_{GB}$ at flat-band allowing one to simply set $\psi_{ss} = \psi_{sd}$ in accumulation without encountering any discontinuities in the derivatives, and *(iii)* in contrast to [7, 14], it is valid even for very negative values of channel voltage ($V < -0.5$V). Eq. (4) produces well-behaved $\psi_s(V_{GB}, V)$ dependence without any differences in the output device characteristics relative to the original formulation. The above modification of the original $m(u)$ does not affect the output device characteristics and is, essentially, invisible to the model user.

Computation of the surface potential as a function of terminal voltages requires the solution of the implicit Eq. (3) and represents a long-standing problem of the MOS device modeling. Almost from the beginning it was addressed both through iterative computations and via analytical approximations[3]. Initially, it was thought that the need for evaluation of the surface potential would negatively affect the model performance. In today's

[2] In other words, the channel voltage V is not only a function of coordinate y but of coordinate x as well.
[3] Look-up tables were used as well.

sophisticated models [4, 25, 38] computation of ψ_s takes only 5–10% of the model execution time and is easily performed using one of several powerful algorithms [4, 25, 32].

The iterative solution of ψ_s was originally pursued in [36], and significantly improved in [25] and [37]. An iterative approach is used efficiently in some of today's surface-potential-based models [3, 25, 37, 38]. On the other hand, the analytical approximation of ψ_s initially pursued in [39] was found to be insufficient for the purpose of transcapacitance modeling (a much more demanding task than modeling of current-voltage characteristics [40]) and abandoned. This approach – based on obtaining the asymptotic approximations of the surface potential in different regions of MOSFET operation and joining them via smoothing functions – has been further developed in [41] and brought into its most successful form with about 1mV accuracy in MM11 [18] (where it was later replaced by iterative calculations [25]).

A different approach in which the surface potential is obtained by an approximate solution of the SPE was developed in [5, 4, 16]. The analytical approximation in [4] is based on a specific form of $m(u)$ [7, 14] and as such is limited to $V > -0.5\,\mathrm{V}$. In PSP we use an even more powerful analytical approximation based on (4) [17, 32] which is accurate under all bias conditions. Typical results are shown in Figure 2 for both positive and negative bias on the source-drain *pn* junction. The accuracy of this approximation is better than 1nV, which is sufficient for even the most demanding MOSFET modeling

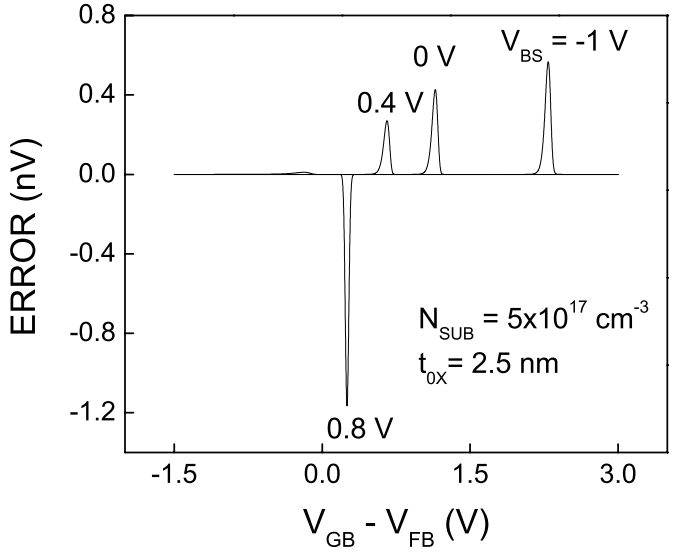

Figure 2. Absolute error of the analytical approximation for the surface potential at source side ψ_{ss} for different values of bulk-source bias V_{BS}.

applications. The approximations of this type are slightly slower than the more simple approximation in [18], but the overall effect on the model execution time is minimal (about 0.4%).

In this section we have discussed the computation of the surface potential in the active region of the device. In the source-drain overlap regions the problem is even simpler and it is addressed in Section 3.1.

2.2. Lateral Field Gradient Factor

As discussed in the previous section, the derivation of the SPE is based on the gradual channel approximation. This approximation neglects the lateral field gradient, and as a result, short-channel effects such as drain-induced barrier lowering (DIBL) and threshold-voltage roll-off are not accurately incorporated in any model based on the GCA.

To extend the model formulation beyond the gradual channel approximation PSP relies on the lateral field gradient factor f introduced in [42]. In weak inversion where $n, p \ll N_{\mathrm{SUB}}$, Eq. (1) at the SiO_2/Si interface is rewritten to:

$$\frac{\partial^2 \psi_s}{\partial x^2} = \frac{q \cdot N_{\mathrm{SUB}}}{\epsilon_{\mathrm{Si}}} \cdot \left(1 - \frac{\epsilon_{\mathrm{Si}}}{q \cdot N_{\mathrm{SUB}}} \cdot \frac{\partial^2 \psi_s}{\partial y^2}\right) = \frac{q \cdot N_{\mathrm{SUB}}}{\epsilon_{\mathrm{Si}}} \cdot f \tag{5}$$

The use of factor f allows the introduction of an effective doping concentration $N_{\mathrm{SUB}} \cdot f$. The application of this method to threshold voltage was reported in [43]. The initial application f this method to surface potential used the bias-independent approximation $f = f(L, W)$ [44], but in PSP, as in SP [4], a bias-dependent approximation is used for f.

An elementary expression for f can be obtained by the following generalization of the analysis in [43, 44]. A parabolic dependence of $\psi_s(y)$ is assumed, which is equivalent to a position-independent f. The boundary conditions are $\psi_s(0) = V_{SB} + V_{BI}$ and $\psi_s(L) = \psi_s(0) + V_{DS}$, where V_{BI} is the built-in potential of the n^+/p source-bulk and drain-bulk junctions. Linearizing the result, one finds the generic expression:

$$f = F_0 \cdot \left(1 - A_f \cdot V_{SB} - C_f \cdot V_{DS}\right) + B_f \cdot \psi_f = f_0 + B_f \cdot \psi_f \tag{6}$$

where ψ_f is the surface potential without lateral field gradient, and F_0, A_f, B_f and C_f are geometry-dependent factors. Despite its simplicity Eq. (6) contains the essential physics: a linear dependence of f on the surface potential ψ_f and a decrease of f with V_{SB} and V_{DS}. The latter can be effectively regarded as the drain-induced barrier lowering (DIBL) effect.

The above derivation serves as a motivation for the actual expression for the lateral gradient factor used in PSP. While the linear dependence of $f(\psi_f)$

has been retained, the dependence on V_{SB} and V_{DS} has been modified in order to assure $f_0 > 0$ for all terminal biases. The result is still Eq. (6) but with

$$f_0 = \frac{F_0}{1 + F_{SB}(V_{SB}) + F_{\mathrm{DIBL}}(V_{DS})} \tag{7}$$

where F_0 is a geometry dependent factor and functions F_{SB}, and F_{DIBL}, as well as the surface potential ψ_f, are selected in a manner consistent with the Gummel symmetry of the model. Complete expressions and further details can be found in [32].

2.3. Drain Current

An important objective of the PSP project is to incorporate essential device physics without a prohibitive increase in the model complexity in the framework of ψ_s-based models. To a large extent this is accomplished using the symmetric linearization technique developed in [4, 6] and similarly in [20, 24]. To simplify the exposition of this key idea we start by reformulating Brews' charge-sheet model (CSM) [28], while neglecting all short-channel effects (which, of course, are included in the complete PSP model equations, see below). There are several ways to arrive at the CSM equations. A particularly simple derivation [29] starts with equation

$$I_{DS} = \mu \cdot W \cdot \left(q_i \cdot \frac{\mathrm{d}\psi_s}{\mathrm{d}y} - \phi_T \cdot \frac{\mathrm{d}q_i}{\mathrm{d}y} \right) \tag{8}$$

where μ denotes the effective channel mobility and q_i is the inversion charge per unit area. There are numerous issues that need to be discussed in connection with the validity of this equation. References [35, 46] and those cited therein are quite useful in this regard. The bottom line is that (8) leads to the original CSM [28] that is justified by comparison with the Pao-Sah model [27]. Our task here is to further simplify (8) in order to make it conducive to the development of a compact MOSFET model.

The symmetric linearization method is based on the approximation

$$q_i = q_{im} - \alpha \cdot (\psi_s - \psi_m) \tag{9}$$

where q_{im} is the inversion charge density at the potential midpoint $\psi_s = \psi_m$:

$$\psi_m = \frac{\psi_{ss} + \psi_{sd}}{2} \tag{10}$$

In the above α denotes the linearization coefficient easily obtained using standard CSM equations [4, 6]. In the full PSP equations the expression for α is slightly more complex in order to provide smooth behavior in all modes of

operations including the region $\psi_s < 3 \cdot \phi_T$ where equations of the original CSM model do not apply. Using (9), Eq. (8) reduces to

$$I_{DS} = \mu \cdot W \cdot q_i^* \cdot \frac{\mathrm{d}\psi_s}{\mathrm{d}y} \tag{11}$$

where q_i^* is the effective inversion charge density modified to account for the diffusion current component

$$q_i^* = q_i + \alpha \cdot \phi_T \tag{12}$$

Integrating from source to drain yields [6]

$$I_{DS} = \mu \cdot \frac{W}{L} \cdot q_{im}^* \cdot \Delta\psi \tag{13}$$

where q_{im}^* is the effective inversion charge density at the surface potential midpoint ψ_m, and $\Delta\psi$ is given by:

$$\Delta\psi = \psi_{sd} - \psi_{ss} \tag{14}$$

The above equation for the drain current is numerically equivalent to the one in the original CSM [28] but is significantly simpler. In particular, fractional powers that are present in the drain current expression in [28] are eliminated, while both drift and diffusion components of the drain current are retained and simplified. Typical results are shown in Figures 3 and 4 indicating that the difference between (13) and the original CSM is less than 1–2% and is inconsequential for the purpose of compact modeling.

Note that Eq. (13) is also accurate in the subthreshold region. In this operation region where $q_{im} \ll \alpha \cdot \phi_T$ and $\Delta\psi$ is an exponential function of the gate bias [9] one can easily recover the classic subthreshold approximation [28, 29, 33].

Up till this point in the derivation of drain current, the carrier mobility in the inversion layer has been assumed constant. In reality, however, this is not true. Carriers in the channel undergo increased scattering with increasing fields, when they move under the influence of the normal electric field and the lateral electric field due to the gate bias V_{GS} and the drain bias V_{DS}, respectively. The former is referred to as mobility reduction, whereas the latter is referred to as velocity saturation.

Mobility Reduction: In a MOS structure the normal electric field restricts the channel to a sheet layer in which two-dimensional confinement effects and scattering cause the mobility to depend on bias conditions. Mobile carriers in the inversion layer can be scattered by ionized doping atoms (so-called Coulomb scattering), by vibrations of the crystal lattice (so-called phonon scattering) and

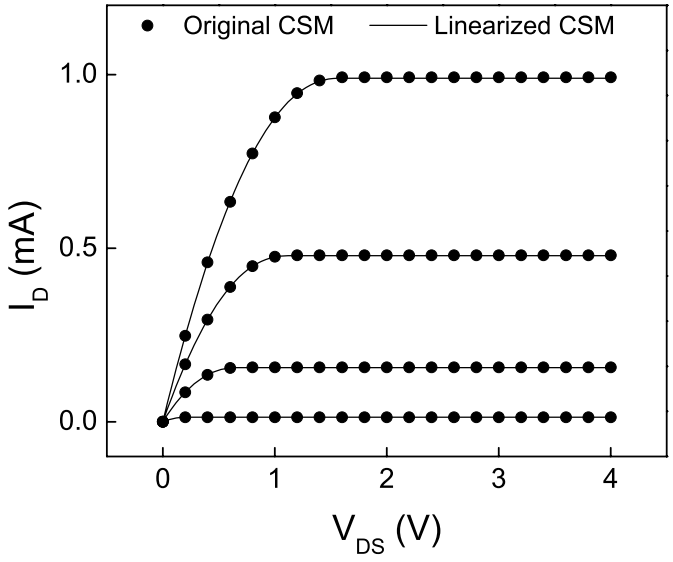

Figure 3. Comparison between the symmetrically linearized and original charge-sheet model; $N_{\mathrm{SUB}} = 5 \cdot 10^{23}\,\mathrm{m}^{-3}$, $t_{ox} = 2\,\mathrm{nm}$, $V_{BS} = 0\,\mathrm{V}$, $\mu = 5 \cdot 10^{-2}\,\mathrm{m}^2/\mathrm{Vs}$, $W/L = 1$, $V_{FB} = -0.9\,\mathrm{V}$, V_{GS} varies between 0.5 and 2 V with 0.5 V steps.

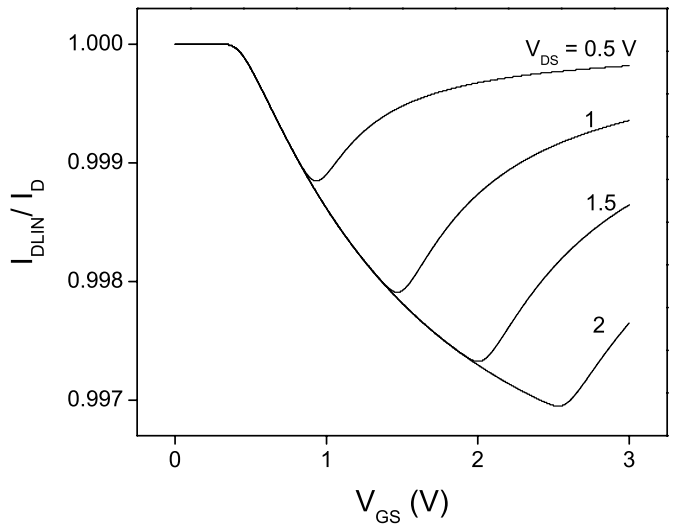

Figure 4. Ratio of the drain currents in symmetrically linearized (I_{DLIN}) and original (I_D) charge-sheet model; $N_{\mathrm{SUB}} = 5 \cdot 10^{23}\,\mathrm{m}^{-3}$, $t_{ox} = 2\,\mathrm{nm}$, $V_{BS} = 0\,\mathrm{V}$, $V_{FB} = -0.8\,\mathrm{V}$.

by the SiO_2/Si interface roughness (so-called surface roughness scattering). The mobility expression used in PSP takes all this into account and is given by:

$$\mu = \mu_{\text{eff}} = \frac{\text{MU0} \cdot \mu_x}{1 + (\text{MUE} \cdot E_{\text{eff}})^{\text{THEMU}} + \text{CS} \cdot \left(\dfrac{q_{bm}}{q_{bm} + q_{im}}\right)^2 + G_R} \tag{15}$$

where MU0 is the low-field mobility, and parameters MUE and THEMU account for the mobility degradation caused by the surface roughness and phonon scattering by the effective vertical field E_{eff}:

$$E_{\text{eff}} = \frac{q_{bm} + \eta \cdot q_{im}}{\epsilon_{\text{Si}}} \tag{16}$$

with $\eta = 1/2$ for electrons and $\eta = 1/3$ for holes. Coulomb scattering is introduced as in [47] using parameter CS, q_{bm} is the bulk charge per unit channel area at the surface potential midpoint [4] and the factor μ_x describes non-universality effects and also accounts (empirically) for doping non-uniformity. The term G_R accounts for the series resistance:

$$G_R = \text{MU0} \cdot \frac{W}{L} \cdot q_{im} \cdot \text{RS} \tag{17}$$

where RS is the source/drain series resistance. When series resistance is included externally G_R can be set to zero.

Velocity Saturation: With an increase in lateral electric field, carriers gain sufficient energy to be scattered by optical phonons, resulting in a decrease of mobility and eventually resulting in the saturation of drift velocity. Velocity saturation is critical not only for the accurate modeling of the saturation region, but also to ensure nonsingular behavior of the model at zero drain bias [45, 48]. The saturation velocity model used in PSP is that of MM11 [22], which is based on the Scharfetter-Gummel expression [49]. For n-channel devices:

$$v_d = \frac{\mu_{\text{eff}} \cdot E_y}{\sqrt{1 + \left(\dfrac{\mu_{\text{eff}}}{v_{\text{sat}}} \cdot E_y\right)^2}} \tag{18}$$

where E_y is the lateral component of the electric field and v_{sat} denotes the saturation velocity. Using (18) in the derivation of drain current leads to an implicit expression for I_{DS}, linearizing this expression leads to the following explicit expression [25]:

$$I_{DS} = \mu_{\text{eff}} \cdot \frac{W}{L} \cdot \frac{q_i^* \cdot \Delta\psi}{G_{\text{vsat}}} \tag{19}$$

where $\theta_{\text{sat}} = \mu_{\text{eff}}/(v_{\text{sat}} \cdot L)$ and:

$$G_{\text{vsat}} = \frac{1}{2} + \frac{1}{2} \cdot \sqrt{1 + 2 \cdot (\theta_{\text{sat}} \cdot \Delta\psi)^2} \tag{20}$$

For p-channel devices, the velocity saturation is accurately described by [49]:

$$v_d = \frac{\mu_{\text{eff}} \cdot E_y}{\sqrt{1 + \dfrac{(\mu_{\text{eff}} \cdot E_y/v_c)^2}{G + \mu_{\text{eff}} \cdot E_y/v_c}}} \tag{21}$$

where v_c is a parameter corresponding to the velocity of the longitudinal acoustic phonons and G is a fitting parameter. In this case, the integration along the channel is less straightforward. For simplicity's sake, we approximate the term $G + \mu_{\text{eff}} \cdot E_y/v_c$ by $G + \theta_{\text{sat}} \cdot \Delta\psi$ where $\theta_{\text{sat}} = \mu_{\text{eff}}/(v_c \cdot L)$. The parameter G has been found to be of minor influence, and is set equal to 1. In other words, all equations derived for n-channel devices can simply be re-used for p-channel devices by replacing θ_{sat} by $\theta_{\text{sat}}/\sqrt{1 + \theta_{\text{sat}} \cdot \Delta\psi}$.

The resulting expressions for n- and p-channel devices are non-singular, enabling for example the modeling of passive RF mixers [48]. As shown in [19] they also enable accurate modeling of RF distortion in the saturation region.

Long-channel surface-potential-based models automatically include the pinch-off behavior in the saturation region. Pinch-off implies that the channel at the drain end is forced into weak inversion and that the mobile charge density at the drain approaches zero. In reality, however, the description of pinch-off is not realistic, since carriers reach velocity saturation at the drain end before the pinch-off condition is fulfilled. As a result the drain-source saturation voltage V_{dsat} may differ significantly from the pinch-off voltage, and this difference needs to be taken into account in the model. This is a general problem for any compact MOSFET model based on the gradual channel approximation.

In PSP, the saturation voltage V_{dsat} is calculated from setting $\partial I_{DS}/\partial\Delta\psi = 0$. Next, the drain-source voltage V_{DS} is replaced by an effective drain-source voltage V_{dse}, which changes smoothly from V_{DS} in the linear region (i.e., for $V_{DS} \ll V_{\text{dsat}}$) to V_{dsat} in the saturation region (i.e., for $V_{DS} \geq V_{\text{dsat}}$). The smooth transition is obtained by [45]:

$$V_{\text{dse}} = \frac{V_{DS}}{\left[1 + (V_{DS}/V_{\text{dsat}})^{a_x}\right]^{1/a_x}} \tag{22}$$

where a_x (≥ 2) is a local parameter which determines the smoothness of the transition. The use of (22) ensures preservation of Gummel drain-source symmetry [45].

For an accurate description of output conductance $g_{DS} = \partial I_D/\partial V_{DS}$ PSP also includes detailed description of channel length modulation. This description is based on [50] and has been extended to include the impact of pocket implants similar to [51].

The incorporation of mobility reduction, velocity saturation, saturation voltage and channel length modulation as described above results in an accurate description of the output characteristics as shown in Figure 5. In addition, the linearization scheme adopted in PSP (as well as those in SP and MM11) enables accurate modeling of ratio-based circuits. A detailed discussion including applications to R2R circuits can be found in [26].

2.4. Intrinsic Charges

In a quasi-static approximation, charges can be attributed to the four terminals of the MOSFET: Q_G, Q_D, Q_S and Q_B. Using these charges, one can define 16 transcapacitances C_{ij} (9 of which are independent):

$$C_{ij} = \begin{cases} \dfrac{\partial q_i}{\partial V_j} & \text{for: } i = j \\ -\dfrac{\partial q_i}{\partial V_j} & \text{for: } i \neq j \end{cases} \tag{23}$$

where i and j denote the terminal S, D, G or B. The total gate charge Q_G is calculated by integrating the gate charge density q_g along the channel:

$$Q_G = W \cdot \int_0^L q_g \cdot \mathrm{d}y \tag{24}$$

where $q_g = q_i + q_b = C_{ox} \cdot (V_{GB} - V_{FB} - \psi_s)$. Note that q_g is a simple function of ψ_s, and as a result the calculation of Q_G is quite straight-forward in ψ_s-based models. In threshold-voltage-based and inversion-charge-based models, on the other hand, the surface potential is not readily available and the calculation of Q_G is more elaborate.

The total inversion-layer charge is split up into a source Q_S and a drain Q_D charge. For MOSFETs with a homogeneous doping concentration the Ward-Dutton charge partitioning scheme [52] is valid, and Q_S and Q_D are given by:

$$Q_S = -W \cdot \int_0^L (1 - y/L) \cdot q_i \cdot \mathrm{d}y \tag{25}$$

$$Q_D = -W \cdot \int_0^L y/L \cdot q_i \cdot \mathrm{d}y \tag{26}$$

This partitioning scheme results in bias-dependent or dynamic charge partitioning. Finally, since charge neutrality holds for the complete transistor, the total bulk charge Q_B is simply given by $-Q_S - Q_D - Q_G$.

Since inversion charge q_i and gate charge q_g are functions of the surface potential ψ_s, calculation of these integrals requires $y\,(\psi_s)$ dependence. For the charge-sheet model explicit expressions for the terminal charges have been

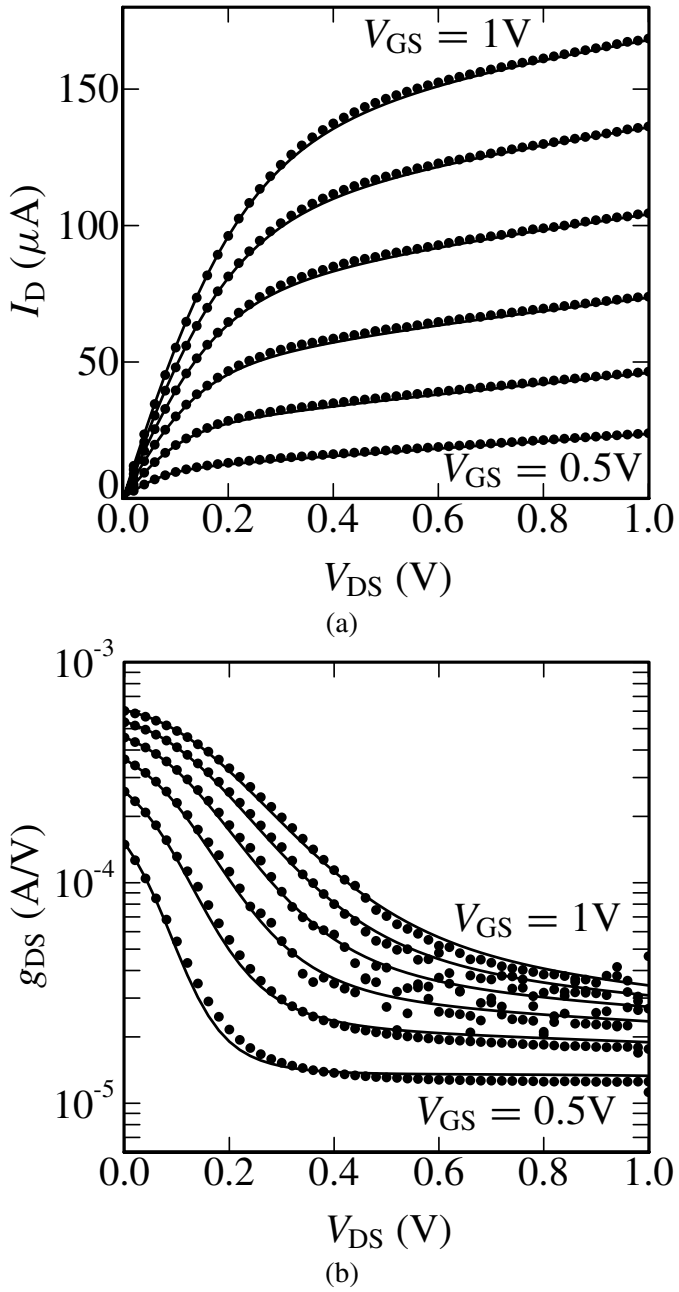

Figure 5. Drain current I_D (a) and corresponding conductance g_{DS} (b) versus drain-source bias V_{DS} for a $W/L = 360\,\text{nm}/90\,\text{nm}$ n-channel MOSFET; V_{GS} varies between 0.5 and 1 V and $V_{SB} = 0\,\text{V}$. Symbols denote measurements and lines represent modeled results using PSP.

given in [34] and, subsequently, in an equivalent but less singular form in [8]. These equations are extremely complex and hence unsuitable for compact modeling purposes. However, just as in the case of the drain current, the symmetric linearization method allows one to derive extremely simple yet accurate expressions numerically indistinguishable from the expressions given in [8, 34]. To simplify the exposition and verification of the technique we first consider the long-channel case and later indicate how the resulting equations can be modified to account for velocity saturation.

From Eqs. (9) through (12), we find:

$$\frac{\mathrm{d}y}{\mathrm{d}s} = \frac{\mu \cdot W}{I_{DS}} \cdot (H - s) \tag{27}$$

where $s = \psi_s - \psi_m$ and $H = q^*_{im}/\alpha$. Separating variables and integrating, we finds [6, 8]:

$$\psi_s(y) = \psi_m + H \cdot \left[1 - \sqrt{1 - 2 \cdot \frac{\Delta\psi}{H} \cdot \frac{y - y_m}{L}}\right] \tag{28}$$

where y_m denotes the coordinate of the surface potential midpoint ψ_m:

$$y_m = \frac{L}{2} \cdot \left(1 + \frac{\Delta\psi}{4 \cdot H}\right) \tag{29}$$

This result of the symmetric linearization method can be compared with the $y\,(\psi_s)$ dependence obtained from the charge-sheet model. Typical plots shown in Figure 6 and given in [6, 8] indicate the high accuracy of (27) and (28).

With (27) available it is a simple matter to compute the integrals for the terminal charges by changing variables from y to s. For example, Eq. (26) for Q_D results in:

$$Q_D = \frac{q_{im}}{2} + \alpha \cdot \frac{\Delta\psi}{12} \cdot \left(1 - \frac{\Delta\psi}{2 \cdot H} - \frac{\Delta\psi^2}{20 \cdot H^2}\right) \tag{30}$$

To verify the accuracy of expression (30) and similar expressions for other terminal charges, they are compared with the exact results in [8, 34]. To make this comparison particularly stringent we evaluate the transcapacitances C_{ij}.

The results shown in Figure 7 indicate that symmetric linearization is extremely accurate. Two comments can be made concerning this conclusion. Firstly, the integration along the channel is a common task in the development of a compact MOSFET model. It is involved in the evaluation of the gate current, the noise spectral densities, etc. In all cases symmetric linearization allows one to obtain manageable equations without compromising the device physics. Secondly, all compact models (even the older threshold-voltage based ones [33, 53]) include some form of linearization of the inversion charge as a function of the surface potential in order to escape complicated expressions

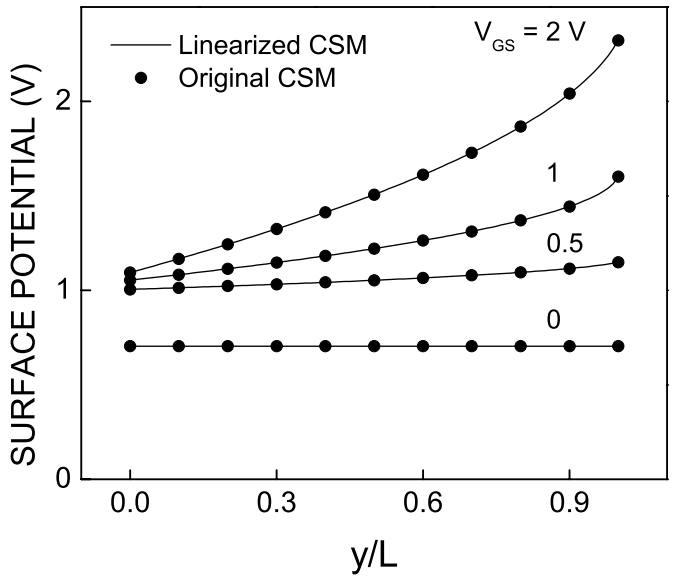

Figure 6. Comparison of the position dependence of surface potential for symmetrically linearized and original charge-sheet models; $N_{\mathrm{SUB}} = 5 \cdot 10^{23}\,\mathrm{m}^{-3}$, $t_{ox} = 2\,\mathrm{nm}$, $V_{BS} = 0\,\mathrm{V}$, $V_{FB} = -0.9\,\mathrm{V}$.

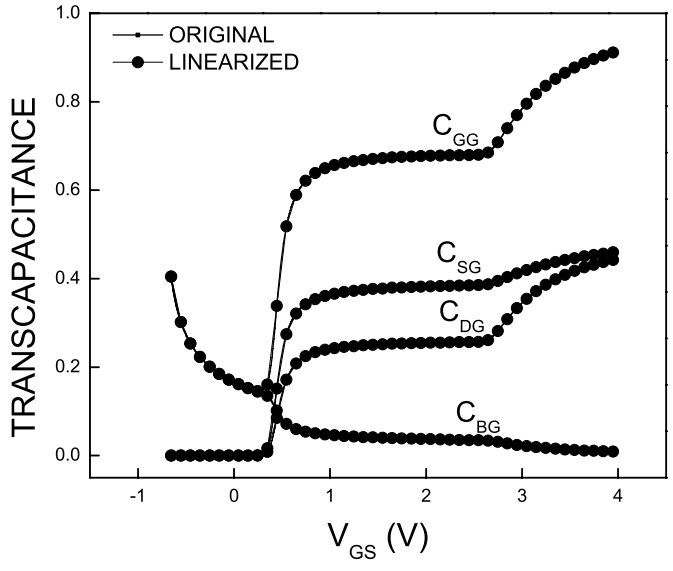

Figure 7. Comparison of transcapacitances for linearized and original charge-sheet models; $N_{\mathrm{SUB}} = 5 \cdot 10^{23}\,\mathrm{m}^{-3}$, $t_{ox} = 2.5\,\mathrm{nm}$, $V_{FB} = -0.8\,\mathrm{V}$, $V_{BS} = 0\,\mathrm{V}$, $V_{DS} = 2\,\mathrm{V}$.

for the terminal charges. In many of the traditional models this results in the loss of Gummel symmetry [26, 33, 45, 48]. In addition, the complexity of the charge expressions may necessitate decoupling the charge and the current expressions with the well-known unfortunate consequences for circuit simulations described, e.g., in [54]. The symmetric linearization method solves both of these problems without complicating the model structure. In fact, the resulting expressions are simpler than in the traditional approach.

The key to the merger of SP and MM11 is the inclusion of the different expression for the drift velocity (18) and the drain current (19) within the context of symmetric linearization. The initial version of this technique was developed for long-channel devices to verify the concept. It was later shown that the flexibility of the symmetric linearization method is such that Eqs. (27) through (30) remain unchanged when the velocity saturation model in SP is included; the only difference being the change in the expression for H [4]. This approach is carried over to PSP where the position dependence of ψ_s is still given by (28), but in order to accommodate the different expression for the drift velocity and the drain current, it can be derived that:

$$H_{\mathrm{PSP}} = \frac{q_i^*}{\alpha' \cdot G_{\mathrm{vsat}}} \tag{31}$$

where

$$\alpha' = \alpha \cdot \left[1 + \frac{1}{2} \cdot \left(\frac{\theta_{\mathrm{sat}} \cdot \Delta\psi}{G_{\mathrm{vsat}}}\right)^2\right] \tag{32}$$

With this in mind the quasi-static terminal charges can be evaluated as in [4, 6, 8], the only difference being that now $H = H_{\mathrm{PSP}}$. For example, the normalized drain charge given in the Ward-Dutton partition is still given by (30). The expressions for the current and terminal charges obtained in this manner are continuous and smooth in all regions of operation from accumulation to strong inversion.

3. Extrinsic Model

The extrinsic model includes contributions of the gate/source and gate/drain overlap regions, and the gate and bulk current. As is the case for the intrinsic model, the electrical behavior in the overlap regions can be most easily described in terms of the surface potential. Consequently, we will start with a discussion of the surface potential in the overlap regions in Section 3.1. Next, the bulk current will be discussed in Section 3.2, followed by a discussion of gate current in 3.3. Finally, the extrinsic charges and capacitances will be treated in Section 3.4.

3.1. Surface Potential in the Overlap Regions

For a quantitative description of the gate/source and gate/drain overlap regions, the overlap regions are treated as n^+-gate/oxide/n^+-bulk MOS capacitances, where the source (or drain) acts as bulk terminal. Assuming the doping profile in the n^+-source extension can be approximated by a uniform constant doping concentration N_{OV}, we can define a body factor γ_{ov} and a flat-band voltage V_{FBov} in this region. A surface potential ψ_{ov} can be calculated (both at source and drain side) using the SPE (3), which can be further simplified by neglecting the minority carrier contribution to the space charge[4]:

$$\left(\frac{V_{GX} - V_{\mathrm{FBov}} - \psi_{ov}}{\gamma_{ov} \cdot \sqrt{\phi_T}}\right)^2 = \exp(-u_{ov}) + u_{ov} - 1 \tag{33}$$

where $u_{ov} = \psi_{ov}/\phi_T$ and V_{GX} denotes either V_{GS} or V_{GD}. Note that to facilitate the comparison with (3), Eq. (33) is written for the p^+ overlap region, i.e., for the case of p-channel transistors. In n-channel devices with n^+ overlap regions one needs to make obvious sign changes in (33).

Analytical approximation for the non-iterative solution of this equation has been initially given in [12] and the final version can be found in [32]. Typical results are shown in Figure 8 for the cases of high and moderate doping, respectively. While the high doping levels are more important for the modeling of the overlap regions, this analytical approximation appears (in a totally different physical context) in the problem of dynamic varactor modeling [55] and in the development of the non-quasi-static model [15]. Hence, it is essential that the accuracy of the approximation is quite high regardless of the doping level.

The derivation of currents and charges in the overlap regions is most easily performed in terms of the oxide voltage in the overlap region V_{ov}, which is simply given by:

$$V_{ov} = V_{GX} - V_{\mathrm{FBov}} - \psi_{ov} \tag{34}$$

This quantity is extensively used in the following sections on bulk current, gate current and extrinsic charges.

3.2. Bulk Current

Up to this point, it has been assumed that the bulk current in a MOSFET is equal to zero. Bulk current may, however, be generated between drain and bulk or between source and bulk by impact ionization and gate-induced drain

[4]This approach disallows description of the inversion channel but since the source/drain extension is highly doped, the inversion channel can only be formed at unrealistically negative gate-source or gate-drain bias.

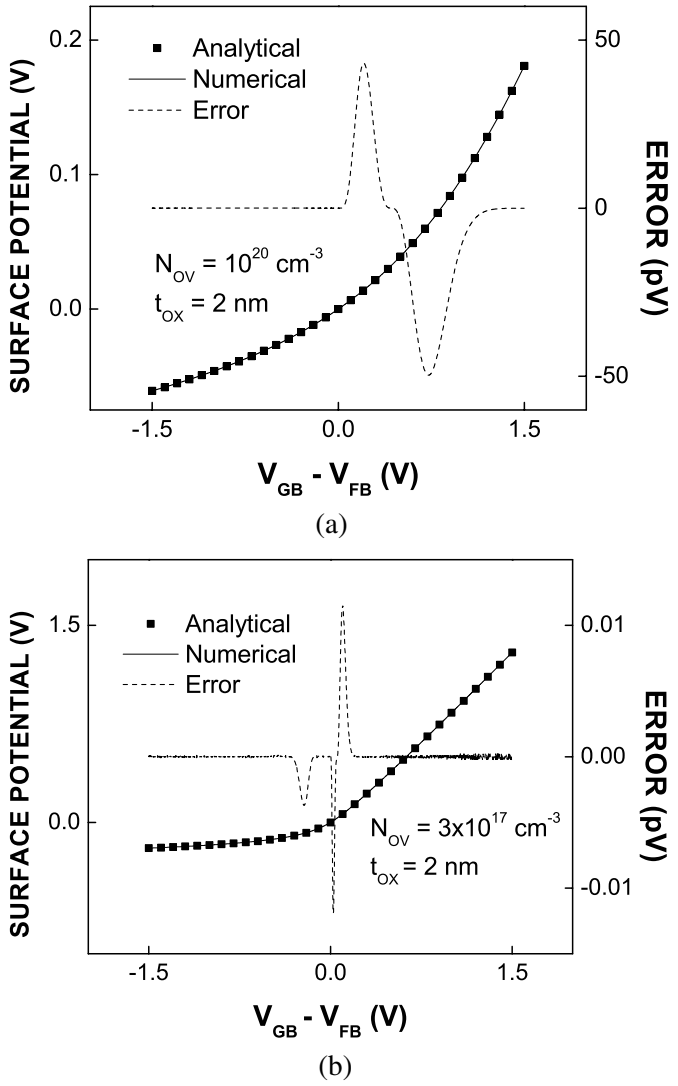

Figure 8. Absolute error of the analytical approximation for the surface potential neglecting the minority carrier contribution in (a) a highly doped the source/drain overlap region and (b) a moderately doped region.

leakage (GIDL). These effects are all included in PSP and are briefly discussed in this section.

Impact Ionization: Subjected to a high lateral electric field, electrons in the channel will accelerate traveling from source to drain and gain so much energy that they can create extra electron-hole pairs by exciting electrons from the

valence band into the conduction band. This effect is generally referred to as impact ionization, and it results in a current I_{ii} between drain and bulk. The impact-ionization current is conventionally written as [33]:

$$I_{ii} \propto I_{DS} \cdot E_m \cdot \exp\left(-b \,/\, E_m\right) \tag{35}$$

where b is a parameter and E_m is the maximum lateral field in the channel. In PSP, this conventional description has been extended with an accurate description of the subthreshold region and the impact of back bias [9].

Gate-Induced Drain Leakage: When the MOSFET is in off-state, a significant leakage current flowing from drain to bulk can be detected at a drain voltage much lower than the breakdown voltage [56]. This drain leakage current is caused by the gate-induced high electric field in the gate-to-drain overlap region, and as a result it has been named gate-induced drain leakage (GIDL). For negative gate-drain bias V_{GD}, a high transversal field is created in the depletion region formed in the gate-to-drain overlap region. Electron-hole pairs are generated by the band-to-band tunneling[5] of valence band electrons into the conduction band and collected by the drain and bulk separately. A simple expression for GIDL current based on [57] is given by:

$$J_{\mathrm{GIDL}} \propto {E_{\mathrm{tov}}}^2 \cdot \exp\left(-B^*_{\mathrm{GIDL}} / E_{\mathrm{tov}}\right) \tag{36}$$

where B^*_{GIDL} is a physical parameter and E_{tov} is the maximum electric field at the Si/SiO_2-interface in the drain overlap region. The latter consists of a (dominant) transversal component (equal to $C_{ox} \cdot V_{ov}/\epsilon_{\mathrm{Si}}$) and a lateral component empirically proportional to V_{DB}. The maximum electric field E_{tov} can be written as:

$$E_{\mathrm{tov}} = \frac{C_{ox}}{\epsilon_{\mathrm{Si}}} \cdot \sqrt{{V_{ov}}^2 + (C_{\mathrm{GIDL}} \cdot V_{DB})^2} = \frac{C_{ox}}{\epsilon_{\mathrm{Si}}} \cdot V_{\mathrm{tov}} \tag{37}$$

where C_{GIDL} is an empirical parameter. Using (36) and (37), we can write for the total GIDL current:

$$I_{\mathrm{GIDL}} = A_{\mathrm{GIDL}} \cdot V_{DB} \cdot {V_{\mathrm{tov}}}^2 \cdot \exp\left(-B_{\mathrm{GIDL}} / V_{\mathrm{tov}}\right) \tag{38}$$

where $A_{\mathrm{GIDL}} \propto W \cdot \Delta L_{ov} \cdot C_{ox}/\epsilon_{\mathrm{Si}}$ and $B_{\mathrm{GIDL}} = \epsilon_{\mathrm{Si}} \cdot B^*_{\mathrm{GIDL}}/C_{ox}$, but they are both considered as local parameters. The V_{DB} term in (38) is empirical and has been added in order to ensure that $I_{\mathrm{GIDL}} = 0$ for $V_{DB} = 0$ and that I_{GIDL} changes sign when V_{DB} changes sign.

In the above derivation we have focussed on the gate-induced drain leakage. The same phenomenon, however, can also occur at the source side, in which case it is referred to as gate-induced source leakage (GISL). The electric field

[5] Trap-assisted tunneling may also occur, but it is neglected in the calculation of GIDL.

in the overlapped source region is typically not as high as the field in the drain region, and as a result, GISL will not really impact the source leakage. Nonetheless, GISL has been incorporated in the PSP model in order to preserve Gummel drain-source symmetry.

3.3. Gate Current

From a classical point of view, gate current in a MOSFET is non-existent, since carriers in the inversion layer cannot cross the potential barrier χ_B of the gate oxide, see Figure 9 (where $\chi_B = \chi_{B_N}$ for electrons and $\chi_B = \chi_{B_P}$ for holes). From a quantum-mechanical point of view, however, carriers may tunnel through the potential barrier resulting in a non-zero gate current density J_G. The probability of tunneling increases exponentially with decreasing oxide thickness t_{ox}, resulting in an exponentially increasing J_G. With CMOS technology scaling, t_{ox} is continuously scaled down, and consequently gate current can no longer be neglected for modern and future CMOS technologies as it may start to affect circuit performance [60, 61]. PSP provides for a gate current

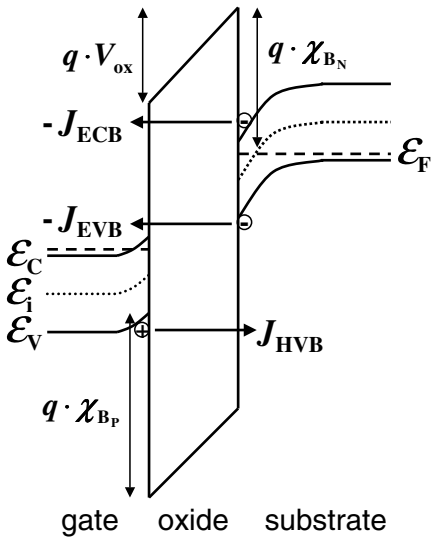

Figure 9. Energy-band diagram of an n-MOS in inversion where χ_{B_N} and χ_{B_P} are the oxide potential barriers for electrons and holes, respectively. Carriers may tunnel through the gate oxide resulting in a non-zero gate current density J_G. Three major mechanisms of gate tunneling can be distinguished: electron conduction-band tunneling (J_{ECB}), electron valence-band tunneling (J_{EVB}) and hole valence-band tunneling (J_{HVB}). ECB tunneling is important for n-MOS devices, whereas HVB tunneling is important for p-MOS devices. EVB tunneling only becomes important for high V_{ox}, and is therefore neglected in the remainder of this section.

model that accurately describes gate leakage in MOSFETs. This gate current model is a further development of the gate current model in SP [12], which in itself is an extension of the gate current model in MM11 [21].

In a typical MOSFET structure, we can distinguish two main gate current components: the gate-to-channel I_{GC} and the gate overlap component I_{Gov}. In the channel or overlap regions of an n-type MOSFET, mainly conduction band tunneling (ECB) is important[6]. The gate current density J_G due to direct tunneling is written as [12]:

$$J_G(y) = J_0 \cdot F_S(y) \cdot D(y) \tag{39}$$

where J_0 is a physical constant, $F_S(y)$ is the supply function [62] and $D(y)$ is the tunneling transmission coefficient. Based on the WKB approximation $D(y)$ is given by:

$$D(y) = \exp\left[-B \cdot f(z_g)\right] \tag{40}$$

where B is a physical constant, z_g is equal to V_{ox}/χ_B, $V_{ox} = q_g/C_{ox}$, and:

$$f(z_g) = \frac{1 - (1 - z_g)^{3/2}}{z_g} \approx -\frac{3}{2} + G_2 \cdot z_g + G_3 \cdot z_g^2 \tag{41}$$

Ideally, the coefficients $G_2 = 3/8$ and $G_3 = 1/16$ can be obtained from a second-order Taylor expansion. However, here they have been turned into adjustable parameters to absorb inaccuracies included in the derivation of (39)–(40). The supply function [62] is given by:

$$F_S(y) = \ln\left[\frac{1 + \exp\left(\dfrac{\psi_s - V - \alpha_b - \psi_t}{\phi_T}\right)}{1 + \exp\left(\dfrac{\psi_s - V_{GB} - \alpha_b - \psi_t}{\phi_T}\right)}\right] \tag{42}$$

where $q \cdot \alpha_b$ is the difference between the conduction band edge and the electron quasi-Fermi potential, and the variable ψ_t reflects the fact that there are few electrons having a kinetic energy higher than a few $k \cdot T$. Specifically, $\psi_t = 0$ for $V_{ox} \geq 0$ and $\psi_t = -V_{ox} + G_0 \cdot \phi_T$ for $V_{ox} < 0$, where G_0 is an adjustable parameter accounting for the possibility of a difference between the conduction band offset at the Si/SiO_2 and poly-Si/SiO_2 interfaces. In contrast to more empirical models, the use of the supply function F_S automatically ensures that gate current is zero for zero applied bias.

In the following we briefly discuss the gate-to-channel and the gate-overlap current components separately.

[6] In p-type MOSFETs, on the other hand, mainly valence band tunneling is important. In the following, the same derivation can be used for p-type MOSFETs but a different value for oxide potential barrier χ_B has to be used, see Figure 9.

Gate-to-Channel Current: The total contribution I_{GC} of the channel region to the gate-tunneling current is given by:

$$I_{GC} = W \cdot \int_0^L J_G(y) \cdot \mathrm{d}y \tag{43}$$

In order to calculate the above integral, the current continuity equation has to be solved:

$$\frac{\partial I_{DS}(y)}{\partial y} = -W \cdot J_{GC}(y) \tag{44}$$

where I_{DS} is given by (11) and is no longer constant along the channel. Eq. (44) cannot be solved explicitly, and as a consequence it needs to be approximated for compact modeling purposes. The current continuity equation is solved under the assumption that J_{GC} only induces a small perturbation of the potential distribution along the channel (i.e., $\partial I_{\mathrm{DS}}/\partial x \approx 0$). We note in passing that this assumption implies that I_{DS} is (approximately) constant along the channel and all equations derived in Section 2 are still valid. For this case, using the symmetric linearization method described in Section 2.4, Eq. (43) results in:

$$I_{GC} = I_{\mathrm{GINV}} \cdot F_S(y_m) \cdot D(y_m) \cdot p_{gc} \tag{45}$$

where I_{GINV} is theoretically given by $J_0 \cdot W \cdot L$ but is considered as an empirical parameter, y_m is the lateral coordinate of the surface potential midpoint as given by (29), and p_{gc} is a function of ψ_m and $\Delta\psi$. The latter can be found in the PSP documentation [32].

The total gate-to-channel current I_{GC} partitions into a source (I_{GCS}) and a drain component (I_{GCD}). Following [21]

$$I_{\mathrm{GCD}} = \frac{W}{L} \cdot \int_0^L y \cdot J_G(y) \cdot \mathrm{d}y \tag{46}$$

and $I_{\mathrm{GCS}} = I_{GC} - I_{\mathrm{GCD}}$. Again using the symmetric linearization method, the above integral results in

$$I_{\mathrm{GCD}} = I_{\mathrm{GINV}} \cdot F_S(y_m) \cdot D(y_m) \cdot p_{gd} \tag{47}$$

where p_{gd} is a function of ψ_m and $\Delta\psi$, which can be found in the PSP documentation [32].

Gate-Overlap Current: Essentially the same model for the tunneling current is used in both the channel and the overlap regions. However, in the latter case the position dependence of the surface potential is negligible, and hence the tunneling current density is approximately uniform. As a consequence, the gate-overlap current I_{Gov} in an overlap region with applied gate bias V_{GX} and surface potential ψ_{ov} is written as:

$$I_{\mathrm{Gov}} = I_{\mathrm{GOV}} \cdot F_S(\psi_{ov}, V_{GX}) \cdot D(z_{\mathrm{gov}}) \tag{48}$$

where I_{GOV} is theoretically equal to $J_0 \cdot W \cdot L_{ov}$, L_{ov} is the length of the gate/source or gate/drain overlap region, and z_{gov} is equal to V_{ov}/χ_B. The above equation is used for both gate-source and gate-drain overlap current by making V_{GX} equal to V_{GS} or V_{GD}, respectively.

Including the above components, the model gives an accurate description of gate current over the whole operation region for both n- and p-channel devices, see Figure 10. The gate current model provides Gummel symmetry as well.

3.4. Extrinsic Charges

For short-channel transistors, a major part of the total input capacitance C_{GG} is determined by the gate-to-source and gate-to-drain overlap capacitances. An accurate modeling of these bias-dependent overlap capacitances is thus important. Using Gauss' law and (34), the total charge in the overlap region is simply given by:

$$Q_{\mathrm{xov}} = \mathrm{CGOV} \cdot V_{ov} \tag{49}$$

where CGOV is a model parameter accounting for the geometry of the overlap region. Here again, X denotes either source or drain (with corresponding changes in ψ_{ov}). Taken together with the analytical approximation of ψ_{ov}

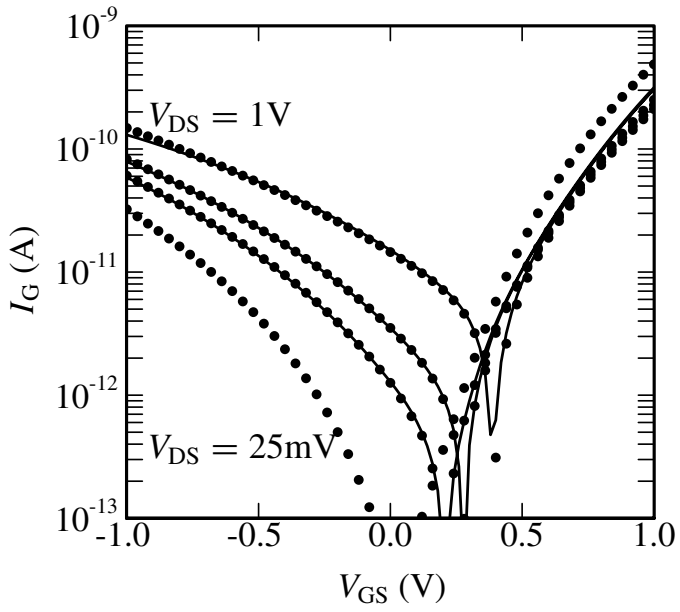

Figure 10. Gate current I_G versus gate-source bias V_{GS} at $V_{SB} = 0$ V and different drain-source bias V_{DS} for a $W/L = 360$ nm/90 nm n-channel MOSFET. Symbols denote measurements and lines represent modeled results using PSP.

illustrated in Figure 8, this expression provides a physical and computationally efficient description of the bias-dependent overlap charges eliminating the need for the mostly empirical modeling of Q_{xov} in older compact models.

In addition to the bias dependence of the overlap capacitance, the PSP model includes both the outer and inner-fringing charges (capacitances). The bias-independent outer fringing capacitance is a model parameter CFR and the outer fringing charge is simply CFR $\cdot$ V_{GX}. As described in [53] the inner fringing phenomena is strongly affected by the formation of the inversion layer and is consequently bias-dependent. In PSP inner fringing is modeled as the reduction of the source and drain terminal charges by ΔQ_S and ΔQ_D and corresponding change in the gate charge $\Delta Q_G = -\Delta Q_S - \Delta Q_D$ required to maintain the charge neutrality. Physically this reduction represents the deviation from the gradual-channel approximation inevitable in strong lateral-field regions close to the source and drain. Availability of ψ_{ov} enables formulation of the physically motivated semi-empirical expressions for ΔQ_S and ΔQ_D sufficient in engineering applications. Typical results for the extrinsic capacitances are shown in Figures 11. Further details including comparison with experimental data and two-dimensional simulations can be found in [11].

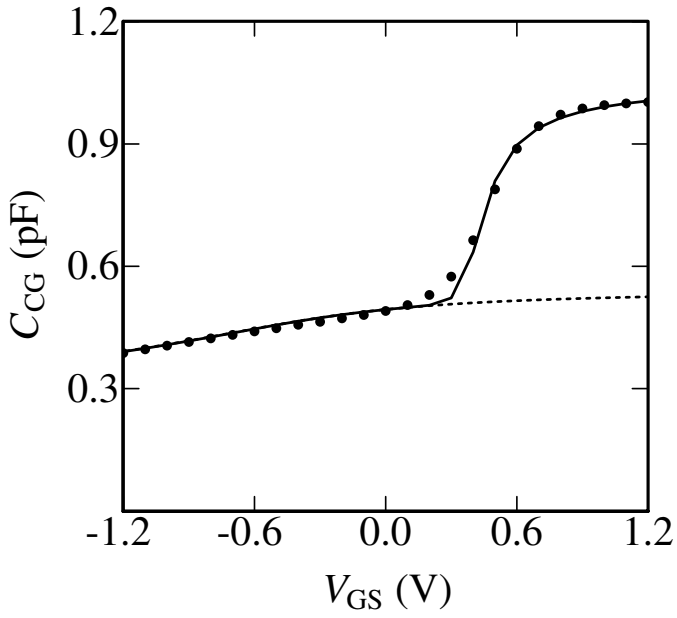

Figure 11. Channel-to-gate capacitance C_{CG} $(= C_{SG} + C_{DG})$ versus gate-source bias V_{GS} for short-channel n-type MOSFET; $V_{SB} = V_{DS} = 0\,\mathrm{V}$, $W/L = 800\,\mu\mathrm{m}/90\,\mathrm{nm}$. Symbols denote measurements, solid line denotes modeled extrinsic and intrinsic capacitances using PSP and dashed line denotes modeled extrinsic capacitance using PSP.

4. Noise Model

The circuit performance in analog and RF circuits is often limited by noise, and accurate modeling of noise behavior in circuit simulation is thus essential. In a MOSFET, generally three different types of noise can be observed: $1/f$ or flicker noise, thermal noise and induced gate noise. These types of noise are all related to the channel current. In reality, the gate tunnel current and the bulk current will also exhibit noisy behavior due to shot noise [63]. This has been taken into account in PSP as well, but is not further elaborated in this chapter.

In Section 4.1, the $1/f$ or flicker noise, as implemented in PSP, is briefly discussed. Since thermal noise and induced gate noise in a MOSFET stem from the same physical origin, they will both be treated in Section 4.2.

4.1. Flicker or 1/*f* Noise

At low frequencies, flicker or $1/f$-noise becomes dominant in MOSFETs. In the past, this type of noise was interpreted either in terms of trapping and detrapping of charge carriers in the gate oxide or in terms of mobility fluctuations. A general $1/f$-noise model by Hung *et al.* which combines both number and mobility fluctuations [64, 65], has found wide acceptance in the field of MOS modeling. The model assumes that the carrier number in the channel fluctuates due to trapping/detrapping of carriers in the gate oxide, and that these number fluctuations also affect the carrier mobility resulting in (correlated) mobility fluctuations. The model was originally formulated for V_T-based models. The PSP flicker noise model is obtained by developing a surface-potential-based version of the general model in [64, 65] resulting in an accurate expression for all operating regions. This formulation further develops an earlier version of the surface-potential-based adaption of [64, 65] given in [11, 22].

4.2. Thermal Noise and Induced Gate Noise

Thermal (or Nyquist) noise is caused by the random thermal (or Brownian) motion of carriers. In a MOSFET, the random motion of carriers in the channel translate to a fluctuation in the channel current I_{DS} flowing between drain and source. The channel current thus exhibits a frequency-independent (or white) noise spectral density S_{id}. In addition, owing to capacitive coupling between gate and channel, the fluctuations in the channel also induce a noise current in the gate terminal at high frequencies. Hence, apart from the channel current thermal noise spectral density S_{id}, the high-frequency noise also consists of the induced gate noise spectral density S_{ig}, which increases with f^2. Since both

S_{id} and S_{ig} stem from the same noise origin, they are partly correlated with correlation coefficient c.

Most available noise models for MOSFETs such as, e.g., the well-known Van der Ziel model [66], make use of the so-called Klaassen-Prins approach [67]. This approach, however, does not accurately account for velocity saturation [68]. As a result these models are inaccurate for short-channel devices [24, 69], where in particular S_{ig} is underestimated. An improved Klaassen-Prins approach, which accurately accounts for velocity saturation, was developed in [24, 69] and is used in MM11, level 1102, and in PSP.

In this approach, the channel current spectral density can be written as:

$$S_{id} = N_d \cdot \int_{V_{SB}}^{V_{DB}} g_c^2(V) \cdot \mathrm{d}V \tag{50}$$

where $N_d = 4 \cdot k \cdot T \cdot I_{DS}^{-1} \cdot L_c^{-2}$, and g_c and L_c denote the corrected channel conductivity and channel length, respectively. For the velocity saturation expression (18) used in PSP:

$$g_c(V) = \frac{g_0^2(V)}{g(V)} \tag{51}$$

$$L_c = L \cdot \frac{\int_{V_{SB}}^{V_{DB}} g_c(V) \cdot \mathrm{d}V}{\int_{V_{SB}}^{V_{DB}} g(V) \cdot \mathrm{d}V} \tag{52}$$

Here $g_0(V)$ is the channel conductivity without velocity saturation:

$$g_0(V) = \mu_{\mathrm{eff}} \cdot W \cdot q_i(V) \tag{53}$$

and $g(V)$ is the channel conductivity (including velocity saturation):

$$g(V) = \frac{g_0(V)}{\sqrt{1 + \left(\mu_{\mathrm{eff}} \cdot E_y / v_{\mathrm{sat}}\right)^2}} \tag{54}$$

Note that the channel current I_{DS} is a simple function of channel conductivity: $I_{DS} = g(V) \cdot \mathrm{d}V/\mathrm{d}y$.

The gate current spectral density can be written as [24, 69]:

$$\begin{aligned} S_{ig} = N_g \cdot & \int_{V_{SB}}^{V_{DB}} g_c^2(V) \\ & \cdot \left(\int_{V_{SB}}^{V} g_c\left(V'\right) \cdot \left[q_g\left(V'\right) - q_g(V) \right] \cdot \mathrm{d}V' \right)^2 \cdot \mathrm{d}V \end{aligned} \tag{55}$$

where $N_g = N_d \cdot \omega^2 \cdot W^2 / I_{DS}^4$. The cross-correlation spectral density between gate and drain current is given by [24]:

$$\begin{aligned} S_{igid} = N_{gd} \cdot & \int_{V_{SB}}^{V_{DB}} g_c^2(V) \\ & \cdot \left(\int_{V_{SB}}^{V} g_c\left(V'\right) \cdot \left[q_g\left(V'\right) - q_g(V) \right] \cdot \mathrm{d}V' \right) \cdot \mathrm{d}V \end{aligned} \tag{56}$$

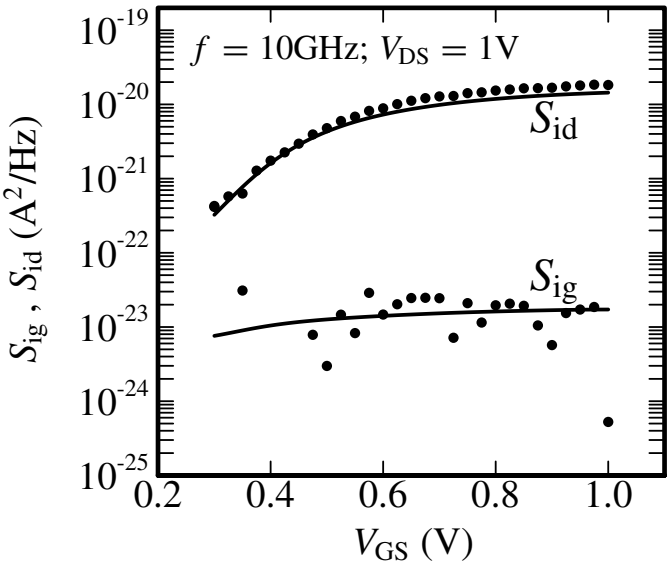

Figure 12. Drain (S_{id}) and gate (S_{ig}) current noise spectral density versus gate-source bias for an $L = 90\,\text{nm}$ n-channel device. Symbols denote measurements and lines represent modeled results using PSP.

where $N_{gd} = -j \cdot N_d \cdot \omega \cdot W/I_{DS}^2$. Finally, the correlation coefficient c is given by:

$$c = \frac{S_{igid}}{\sqrt{S_{ig} \cdot S_{id}}} \tag{57}$$

Using the symmetric linearization method, the improved Klaassen-Prins approach can be straightforwardly included in the ψ_s-framework. The corresponding expressions for S_{id}, S_{ig} and c can be found in the PSP documentation [32]. The resulting noise model gives an accurate description of high-frequency noise in MOSFETs down to deep-submicron dimensions, see Figure 12. The model is in good agreement with measurement data without using any additional noise parameters.

5. Junction Diode Model

In a MOS device, the drain/bulk and source/bulk junctions act as diodes, and as a result they will also contribute to the bulk current and capacitance. Due to the ever increasing junction steepness and pocket implantations, junction leakage is an increasing concern in CMOS technology scaling. The physical phenomena responsible for the increasing junction leakage are Shockley-Read-Hall

generation/recombination (SRH), trap-assisted tunneling (TAT) and band-to-band tunneling (BBT). Present-day compact models [1, 58] lack accurate physical descriptions of these effects. The PSP model contains a new junction diode model named JUNCAP2 [30], that is also available in stand-alone format. In contrast to earlier models [1, 58, 59], this model *(i)* gives single-piece expressions for SRH and TAT, valid in both forward and reverse mode of operation, *(ii)* removes the need for introducing an unphysical ideality factor, *(iii)* extends the existing model for TAT, valid at low fields, to the high-field regime encountered in modern MOS junctions, and *(iv)* is valid for junctions of arbitrary grading coefficient. In addition, the model incorporates shot noise in the junction current.

For the accurate modeling of a typical drain/bulk or source/bulk junction region, JUNCAP2 distinguishes three components: the bottom-edge, the STI-edge and the gate-edge component. These components scale differently with geometry, and, due to different junction steepness and doping concentrations at the different edges, these components show different electrical behavior. This is incorporated in JUNCAP2. As a result, JUNCAP2 gives an accurate description of the electrical behavior of junctions in modern CMOS technologies over a wide range of bias, geometry and temperature [30], see Figure 13.

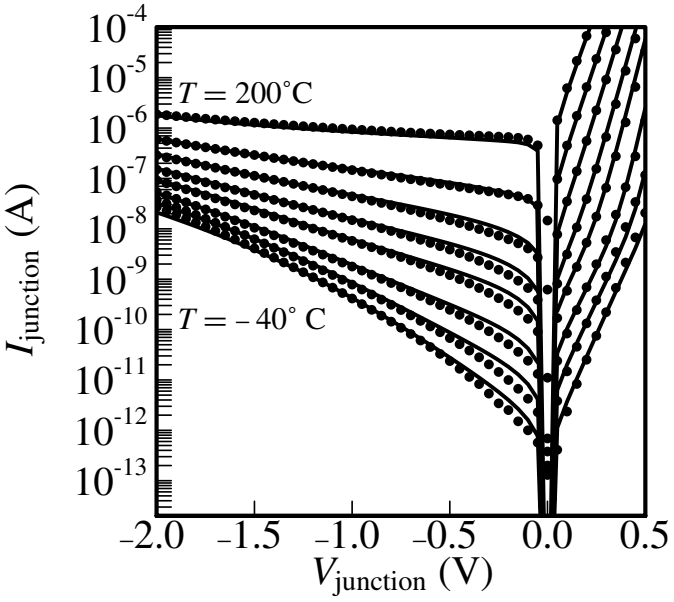

Figure 13. Junction leakage current I_{junction} versus applied junction bias V_{junction} at different temperatures for a typical n^+/p junction in 0.12 µm CMOS technology. Symbols denote measurements and lines represent modeled results using JUNCAP2.

6. Non-Quasi-Static Model

The intrinsic charge model described in Section 2.4 is quasi-static (QS). The QS approach assumes that a charge Q_X can be attributed to a terminal X and that Q_X changes instantaneously with a changing terminal voltage. In other words, it assumes that carriers travel at infinite velocity, which is not physical. A finite carrier velocity results, for example, in a phase shift (or delay) between the channel current and the gate voltage. This phase shift is not taken into account in the QS approach. This implies that for applications at high frequencies (approaching the cut-off frequency of the device) or for applications subject to fast transients, errors have to be expected in the QS approach due to non-quasi-static (NQS) effects. An NQS model of the MOSFET is thus essential for these applications.

Of the several NQS models developed at present, two allow an arbitrary trade-off between model accuracy and complexity: the channel segmentation method [70] and the spline-collocation technique [8, 15, 31]. The latter is more calculation-time efficient and is adopted in PSP after careful verification based in part on the channel segmentation method [31].

The spline collocation technique converts the partial differential equation expressing channel current continuity into a system of coupled ordinary differential equations that can be readily solved by circuit simulators. This is done as follows. Using (8) the continuity equation for the channel current $i(y,t)$

$$\frac{\partial i(y,t)}{\partial y} = W \cdot \frac{\partial q_i(y,t)}{\partial t} \tag{58}$$

is brought into a form [71] $R(y,t) = 0$ where:

$$R(y,t) = \frac{\partial q_i}{\partial t} + \frac{\partial}{\partial y} \cdot \left[\mu \cdot \left(\frac{q_i}{\mathrm{d}q_i/\mathrm{d}\psi_s}\right) - \phi_T\right] \cdot \frac{\partial q_i}{\partial y} \tag{59}$$

This automatically includes both drift and diffusion components of the current in the NQS model and with a proper choice of the $q_i(\psi_s)$ dependence includes all regions of MOSFET operation [15]. The collocation method is a particular form of the weighted residuals technique in which $q_i(y,t)$ dependence is approximated by a simpler function $q_a(y,t)$ and instead of demanding $R(y,t) = 0$ one imposes a weaker set of N conditions:

$$\int_0^L w_k(y) \cdot R_a(y,t) \cdot \mathrm{d}y = 0;\ k = 1, 2, \ldots, N \tag{60}$$

where $w_k(y)$ are appropriately chosen weighting factors and R_a is obtained from R by changing q_i into q_a. Specifically, for the collocation method

$$w_k = \delta(y - y_k) \tag{61}$$

where $y_k = k/(N+1)$. This is equivalent to requiring the continuity equation to be satisfied at N equidistant collocation points y_k rather than at any point along the channel.

A simple choice for q_a is a polynomial

$$q_a = \sum_{n=1}^{m} a_n(t) \cdot y^n \tag{62}$$

with time-dependent coefficients. This approach (with $N = 1$ and $m = 2$) has been used in the first successful application of the collocation method to the MOSFET NQS modeling [72]. Unfortunately, for $m > 2$ the polynomial approximation introduces unphysical oscillations of the inversion charge as a function of distance. This limits the technique to a single collocation point ($N = 1$) which is not sufficient, for example, for RF simulations and some fast transients.

A more powerful technique, the so-called spline collocation method, is to approximate the inversion charge by cubic splines with time-dependent coefficients selected as to provide continuity of q_a and its first two derivatives with respect to coordinate y. In this case q_a is oscillation-free for an arbitrary number of collocation points. Using Eqs. (60) and (61) one obtains a system of N ordinary first degree differential equations of the type

$$\frac{\mathrm{d}z_k}{\mathrm{d}t} = f_k(z_1, \ldots, z_k) \tag{63}$$

where $z_k = q_a(y_k, t)$ and f_k are known functions. Equations (63) are easily solved by circuit simulators (e.g., using coupled RC subcircuits) and the terminal currents are evaluated in terms of z_k and their time derivatives. Complete details are given in [8, 15, 31]. Here we note only that all terminal currents are automatically included in this approach. The NQS model used in PSP directly includes mobility reduction, velocity saturation and other small-geometry effects [31].

An important advantage of the spline collocation method is the arbitrary number of collocation points that translates into an arbitrary precision of the calculations (naturally, increasing N requires longer simulation times). Typically $N = 2$ is sufficient for transient simulations while $N = 5$ is used in RF applications. The latter also requires inclusion of the substrate subcircuit as described in [70]. Typical results for transient simulations are shown in Figure 14.

In addition to the overall reduction of the current, mobility reduction lengthens the transients. An example of RF simulations is shown in Figure 15 indicating a good agreement with measured results and channel segmentation method. In addition, PSP NQS model has been verified by comparison with the direct numerical solution of $R(y, t) = 0$. Since both the large-signal and small-signal NQS models use the same set of equations (63), they are consistent with each other and with quasi-static simulations, which appear as a proper limiting case

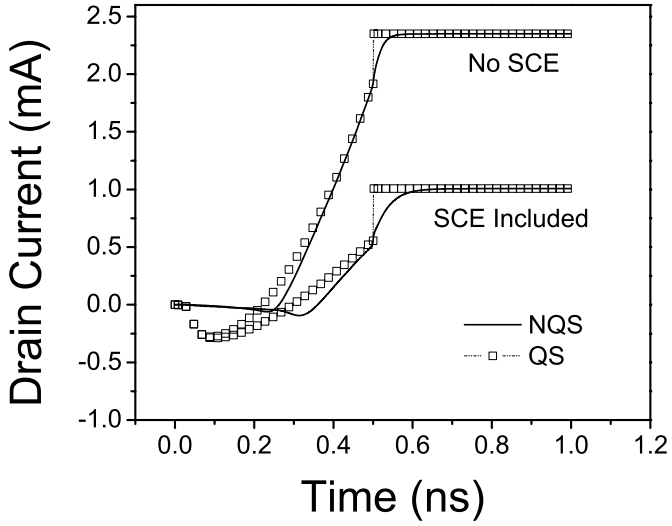

Figure 14. Transient response of $W/L = 5\,\mu\text{m}/5\,\mu\text{m}$ MOSFET with and without short-channel effects (SCE). The gate voltage is ramped from 0 to 3 V in 0.5 ns.

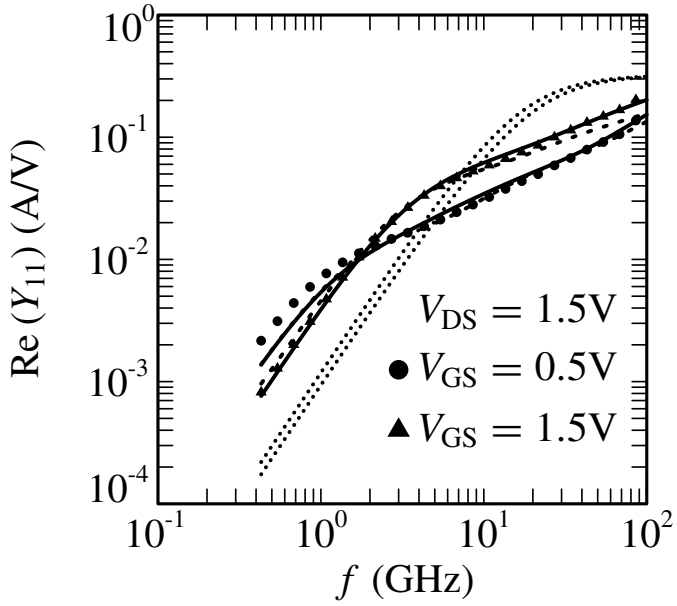

Figure 15. Real part of input admittance Y_{11} versus frequency f for different bias conditions for an n-channel MOSFET; $V_{SB} = 0$V, $W/L = 120\,\mu\text{m}/3\,\mu\text{m}$. Symbols denote measurements, dotted lines denote modeled results using PSP QS-model, solid lines denote modeled results using PSP NQS-model with $N = 5$, and dashed lines denote modeled results using $N = 5$ segmentation model [70] based on MM11. In the simulations bulk and gate resistances have also been taken into account.

of slow transients or in the low-frequency limit. This is not necessarily true for other NQS models.

7. Conclusions

The PSP model is a new compact MOSFET model which combines and extends the best features of the SP and MM11 models. The merger of SP and MM11 into PSP was facilitated by the compatibility of SP and MM11; both models are surface-potential-based, make use of some sort of symmetric linearization and make a distinction between local and global parameter level.

PSP is based on the formulation of surface potential and makes use of an analytical approximation of surface potential with an accuracy better than 1nV for both positive and negative bias on the source-bulk drain-bulk junctions. The derivation of the model expressions is considerably facilitated by the use of the symmetric linearization method. This method was developed in the framework of the SP model, and it has been expanded for PSP in order to include the velocity saturation model of MM11. It results in simple yet accurate expressions for the electrical quantities of the intrinsic MOS device, such as drain-source current, gate current, terminal charges and noise.

The extrinsic model in PSP includes accurate expressions for the gate current, the bulk current due to impact-ionization and gate-induced drain leakage, and the bias-dependent overlap capacitances. For this purpose, PSP uses a description of surface potential in the overlap regions, which is simpler than the above surface-potential description in the intrinsic region.

The noise model in PSP includes flicker noise, thermal noise, induced gate noise, and shot noise in the gate and bulk currents. The thermal noise and induced gate noise are partly correlated, and, in contrast to other models, their description accurately incorporates the impact of velocity saturation. The resulting noise model gives an accurate description of noise in MOS devices down to deep submicron devices without the use hot electron effects.

In addition, PSP contains a new junction diode model JUNCAP2, which is more accurate than state-of-the-art junction diode models. JUNCAP2 includes an accurate description of the Shockley-Read-Hall generation/recombination, trap-assisted tunneling and band-to-band tunneling phenomena, which are important in present-day and future CMOS technologies.

PSP incorporates a support module for the modeling of non-quasi-static (NQS) effects, which is important for high-frequency IC-design. The NQS-model in PSP makes use of the spline-collocation technique, which allows for a trade-off between complexity and model accuracy by changing the number of collocation points. In contrast to other NQS-models, this technique is suitable for both small-signal and large-signal simulations, and it is compatible with the quasi-static description in the limiting cases of slow transient and low-frequency

operation. The spline-collocation technique is less computation-time intensive than the channel segmentation method.

The PSP model has been subjected to the standard convergence tests and verified by comparison with data obtained from several 90 nm and 65 nm node processes. PSP has been selected as a new industry standard for the next generation compact MOSFET model by the Compact Modeling Council (CMC) [73].

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