Chapter 1

2/3-D PROCESS AND DEVICE SIMULATION

An effective tool for better understanding of internal behavior of semiconductor structures

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Abstract: 2/3-D numerical process and device simulation is presented as an extremely useful tool for the analysis and characterization of fabrication processes and corresponding electro-thermal behavior of semiconductor structures and devices standing alone and/or coupled in integrated circuits. In the introductory part of this chapter, a brief description is given of the basic features, processes, and structures implemented in the numerical process and device simulation. Visualization of the internal properties (electrical, thermal, optical, magnetic, and mechanical) allows comprehensive analysis of the critical regions and weak points of the analyzed structures. The presented examples illustrate the potential, power and beauty of numerical simulation of processes and devices for the identification and analysis of the behavior of parasitic devices that exist as inevitable parts of active devices and which degrade the normal operation and reliability of integrated circuits. Commercially available TCAD process and device simulators with verified calibrated complex electro-physical models, advanced numerical solvers securing stable calculations, and user friendly interactive environment provide a unique insight into the internal operation of the analyzed structure. They can be efficiently used for comprehensive physical interpretation of experimentally obtained results and/or particularly for prediction of the properties and behavior of new semiconductor structures and devices as well as for further development and optimization of new technologies and fabrication steps.

W. Grabinski, B. Nauwelaers and D. Schreurs (eds.),
Transistor Level Modeling for Analog/RF IC Design, 1–27.

Key words: process and device simulation; structure (mesh) definition; boundary conditions; electro-physical models; steady state and transient simulation; bipolar and CMOS technology; DMOS technology – power devices; parasitic devices; latch-up effect; electro-thermal interaction.

1. Introduction

Enormous advances in the microelectronics technology with an exponential growth of the complexity and speed following the Moore law [1] and SIA Roadmap [2] are required to secure a continuous development of new technologies, structures, devices, circuits and systems. The better understanding of the electro-physical behavior and potential of new structures and devices with dimensions scaled down to deep submicron range and operating at their physical limits put stringent requirements on modeling and simulation. Since trial manufacturing of highly dense IC with minimal dimensions of individual devices in deep submicron region costs a great deal, modeling and simulation play an increasingly important role in the development and prediction of the properties of modern technologies. By means of simulation, microscopic physical phenomena and effects occurring on very small length scales and in very short time periods can be visualized in macroscopic dimensions and, thus, perceivable to our eyes and mind.

Over the past thirty years, Technology CAD (TCAD) has evolved into a well-accepted branch of the global electronic design automation environment (EDA) characterized for example by a recent acquisition of TCAD tools developer and vendor ISE AG Zurich by Synopsys. Single simulators for process simulation, device simulation, parameters extraction and circuit simulation are integrated by interactive user friendly graphical environments and provide the virtual wafer fab GENESISe-ISE [3] and VWF of Silvaco [4] allowing cost and yield estimation as well as comprehensive parametric analysis of semiconductor processing. Introduction and integration of new physical models for thermo-opto-electro-mechanical effects into advanced simulators enables the simulation of the properties and behavior of microtransducers and very complex micro-opto-electro-mechanical systems (MOEMS). Comprehensive surveys of different physical models, methods of mathematical treatment, features of data compatibility and handling, their visualization and examples of applications of numerical process and device simulation can be found in a large number of books and proceedings [5–7].

The increasing on-chip circuit and system integration allowed by continuing miniaturization of individual semiconductor devices, which are approaching their physical limits, generates a strong pressure on a better understanding of the electro-physical behavior of individual semiconductor structures integrated in IC technology [8]. Design of advanced semiconductor devices with minimum

dimensions at nm scale working in high frequency applications, however, calls for new advanced complex physical models including quantum-mechanical effects for a wide variety of semiconductors, insulators and metals (Si, SiGe, GaAs and other III–V compounds, high k-oxides, silicides) [9]. Mixed mode device and small signal circuit simulators including numerical simulation of 2/3-dimensional structures predicting their behavior, properties and reliability are unavoidable tools of any research team working in the development and optimization of new fabrication processes. There is a continuous need for new experts with complex knowledge and skills who will be able to solve the global problems [10, 11].

In spite of that, most system engineers working in IC design laboratories with EDA tools work on higher abstraction levels with limited knowledge of the internal behavior of individual devices including their parasitic components. Therefore the main aim of this chapter is a presentation of the potential, power and beauty of numerical process and device simulation with its unique insight into the internal semiconductor structure operation for a better understanding of the integrated circuit behavior under various stress conditions in different environments. The reader who is interested in the state of the art numerical process and device simulations including the most advanced physical models with quantum-mechanical effects for deep submicron structures and devices is referred for example to [12] for more details.

A brief description of process and device simulators, their structures, required input parameters, used physical models, format and visualization of output data, and potential applications will be presented. The given examples will characterize the big potential of numerical process and device simulation for a unique insight into the analyzed structure and for identification and analysis of the behavior of parasitic devices that are inevitable parts of almost all active devices in various technologies of IC's.

2. Process Simulation

The behavior and properties of all semiconductor devices are defined by their three geometrical dimensions and concentration profile of impurities. The main goal of process simulation is to model a virtual device with geometry and properties identical with the real structure. The lateral dimensions which specify the active parts of the devices are defined by lithography masks, while the vertical depth and concentration of active impurities depend on the used fabrication processes. Each fabrication process can be modeled usually by a set of partial differential equations (PDE's), which can be solved either analytically and/or numerically. The advanced physical models with calibrated parameters characterizing individual fabrication steps are integrated into the process simulators. As technology development continues, the need for new more precise

process models increases. Continuous calibration of their parameters is based on the best correlation of simulated results with experimental data acquired on special test structures by analytical tools such as secondary ion mass spectrometry (SIMS).

Numerical solutions exploit iterative numerical solvers which calculate the structure properties in a defined region with properly defined boundary conditions. Dense grids with a high number of nodes, where the individual unknowns and properties are defined, provide a higher accuracy, the tradeoff being a longer elapsed time and memory. Therefore, adaptive grid generation in curved regions with steep profiles of physical entities is a necessity particularly for more dimensional simulations. The output results are mostly represented by 2D doping profiles with a 1D cross section, which provides information about the concentration of impurities in selected cross sections in horizontal or lateral dimensions. While some years ago 2D models and solutions were fully sufficient, nowadays only 3D simulation can take into account the global complexity and variety of various phenomena occurring in miniaturized deep sub μm and nano-structures. However, due to the enormous requirements on the computing resources and computing time (full 3D simulation of complete technological process is in general still beyond the capabilities of most today's software tools and computers) they will not supersede the 2D simulations in the near future. To solve the tradeoff between the grid with an increased number of nodes and computation time and memory requirements the simulators allow simulating one half of a symmetrical structure, which is then reflected across the selected boundary.

The current commercially available simulators provide an interactive environment with high a degree of flexibility for input commands, implement advanced physical models with calibrated parameters and numerical solvers with efficient meshing for robust and stable simulation.

The input commands of individual steps make accessible all parameters which characterize the real fabrication processes. They comprise:

Ion implantation – the process by which impurity atoms are implanted into active parts of the substrate material defined by a mask with a given dose, energy and tilt angle, which prevents creation of impurity tails due to the channeling effect. The resulted doping profiles correspond to analytical distribution functions (Gaussian, Pearson, dual Pearson) with tabulated parameters such as the projected range and lateral straggle depending on the collision mechanisms of specific implanted species with the substrate material [13]. If the tables are not available, Monte Carlo simulators for ab initio calculation of interactions of implanted atoms with the substrate atoms can be used [14]. As the projected range in general increases with smaller atoms, BF_2 molecules are used for implantation of shallow junctions to prevent deep penetration of light materials like boron (B). The process of ion implantation creates a big amount of defects and amorphization of Si single crystal occurs when using high doses.

To activate the implanted impurities to the lattice positions and recrystallize the damaged and/or amorphous regions, high temperature annealing should follow the ion implantation process.

Diffusion – is a high temperature process of diffusion of impurities due to the existing concentration gradient, which depends on temperature and time of diffusion, boundary conditions characterizing the surface (interface) concentration of diffusion species at the Si substrate and gas interface. The time and position dependent concentration of impurities are the solution of PDE's (Fick diffusion equations). Various physical models with different levels of complexity depending on the type of impurity (its temperature and concentration dependent diffusion coefficient), point defects and electric field effects implemented in advanced simulators are very well described in [15]. For example, the simplest constant diffusion model which neglects the interactions between the dopants and point defects and electric field effects is used mainly for dopant diffusion in oxides. The pair diffusion model assumes that the gradient of dopant concentration and dopant-defect pairs with the electric field are the driving force of diffusion in active Si regions predefined by the mask. As processing proceeds through various annealing cycles and the concentration gradient exists, the dopants diffuse and redistribute through the structure, therefore the temperature budget should be minimized to ensure very steep and shallow doping profiles for miniaturized structures and devices.

Epitaxial growth – is a growth of single crystalline Si layers on top of the Si substrate at temperatures slightly lower than the melting point. The thickness of the growing epitaxial layer is characterized by the growth rate and time. Various impurities, different in concentration or species from substrate impurities, can be incorporated into the epitaxial layer. As it is a high temperature process, redistribution of impurities occurs at the interface due to the concentration gradient.

Oxidation – is a process of growth of thermal silicon dioxide (SiO_2) at the silicon surface depending on temperature, time and oxidation ambient characterizing the diffusion of oxidants from the gas-oxide interface to Si-SiO_2 interface and its reaction with Si. As the process of thermal oxidation is accompanied by volume expansion, which invokes strong mechanical stresses and materials motion, the ramping up and down temperature cycles with slow temperature changes are used to prevent structure damage. Due to various segregation coefficients of impurities, segregation of dopants occurs at the interface.

Deposition and Etching – are the processes of deposition and etching of different layers (insulators, metals, poly Si). The deposition may be isotropic, anisotropic, polygonal and fill step. The etching means removing of material which is in contact with gas and may be also isotropic, anisotropic and directional. The thickness of a deposited and/or etched layer is defined by the mask and growth/etching rate and time. As the simulated region (volume) is changed, remeshing of the analyzed structure is required.

The input file for the 2D simulation of 0.18 μm NMOSFET with a lightly doped drain in DIOS [15] contains the following commands and parameters:

```
(1)   TITLE("180nm_NMOS")
(2)   # Initial definitions
(3)   grid( x=(-0.4, 0.4) y=(-10.0, 0.0), nx=2)
(4)   substrate (orientation=100, element=B, concentration=5.0E14, ysubs=0.0)
(5)   replace (control(maxtrl=9, refineboundary=-6, refinejunction=-7)
(6)   #Start simulation of Process Steps
(7)   implant (element=B, dose=5.0E13, energy=300keV, tilt=0)
(8)   diff (time=8, temper=900, atmo=O2 )
(9)   deposit (material=po, thickness=180nm) ;poly gate deposition
(10)  mask (material=re, thickness=800nm, x(-0.09, 0.09)) ;poly gate pattern
(11)  etching (material=po, stop=oxgas, rate(aniso=100)) ;poly gate etch
(12)  etching (material=ox, stop=sigas, rate(aniso=10))
(13)  etching ()
(14)  implant (element=As, dose=4.0E14, energy=10keV, tilt=0) ;LDD implantation
(15)  deposit (material=ni, thickness=60nm) ;nitride spacer
(16)  etching (material=ni, remove=60nm, rate(a1=100), over=40)
(17)  etching (material=ox, stop=(pogas), rate(aniso=100))
(18)  implant (element=As, dose=5E15, energy=40keV, tilt=0) ;N+ implantation
(19)  diff (time=@rta_time@sec, temper=1050, atmo=N2) ;final RTA
(20)  mask (material=al, thick=0.03, x(-0.5, -0.2, 0.2, 0.5)) ;metal contacts
(21)  save (file='180nm_nmos', type=DFISE) ;save final structure
```

The results of numerical process simulation by DIOS-ISE are presented in Figure 1. The generated grid with adapted denser grid points in a curved and steep profile region related to 2D doping profile is shown in Figure 1a.

Corresponding 1D doping profile in A-A cross section designated in a is shown in Figure 1b. The influence of different thermal budget on the lateral distribution of N-type impurities and corresponding shortening of channel length can be clearly seen.

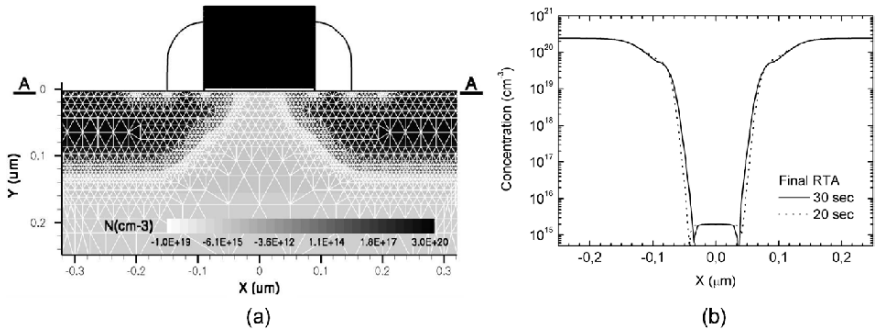

Figure 1. Simulated (a) 2D doping profile with mesh definition, (b) 1D doping profile in A-A cross section for different process temperature budgets.

The simulated results – distribution of dopants in Si are stored in formatted data files and visualization tools are used for quick presentation of the obtained 1D and particularly 2D concentration profiles.

Another important resulted parameter of process simulation is mechanical stress which may induce defects or damage at different layers and interfaces and subsequently influence the electrical properties (interface states density, mobility) of the analyzed structure.

3. Device Simulation

The main goal of device simulation is to provide electrical steady state, transient and small AC signal behavior and characteristics of the studied semiconductor structures for predictive analyses of the properties of new technologies and devices and simultaneously a unique insight into the internal process and structure operation, thus enlarging the users knowledge and expertise. A real semiconductor device, such as transistors, is represented by a virtual device defined by 2/3D structure (output of process simulator) whose electrophysical properties are discretized onto a nonuniform mesh of nodes. The input files for device simulations contain the types of materials, doping profiles of impurities in the given region associated with the discrete nodes, starting temperature, and properly defined boundary conditions with applied external electrical, optical, mechanical, magnetic, and thermal field. An extensive set of advanced electrophysical models with calibrated parameters which characterize the behavior and various effects present in semiconductor structures and interfaces at various applied stresses are incorporated into the advanced device simulators.

The output electrical characteristics are calculated by numerical solution of a set of partial differential equations.

$$\nabla\varepsilon\nabla\psi = -q\left(p - n + N_d^+ - N_a^-\right)$$
$$\nabla\vec{J}_n = qR + q\frac{dn}{dt} \qquad -\nabla\vec{J}_p = qR + q\frac{dp}{dt}$$

For isothermal simulation, the simplest drift-diffusion model comprises three basic semiconductor equations, which are the Poisson and current continuity equations for electrons and holes with potential ψ, free electron and hole concentrations n and p as unknowns. The mobility of free electrons and holes $\mu_{n,p}$, electric field $-\nabla\psi$, generation-recombination rate R and others are considered as variable parameters. They are dependent on the actual values of individual unknowns and therefore an iterative and coupled mode of solution should be used. The total current J in any point of the analyzed structure is then calculated as a sum of electron and hole currents $J_{n,p}$

$$J = J_n + J_p \qquad J_n = -qn\mu_n\nabla\phi_n \qquad J_p = -qp\mu_p\nabla\phi_p$$

where $\mu_{n,p}$ are the mobilities and $\phi_{n,p}$ are the quasi-Fermi potentials of electrons and holes, respectively.

For analysis of devices in which the self-heating effects are not negligible the non-isothermal simulation using a thermodynamic model [16] should be involved. The thermodynamic model assumes that the electrons and holes (their temperatures) are in thermal equilibrium with the lattice temperature and an additional partial differential equation characterizing the influence of self-heating effects and non-isothermal temperature distribution on structure behavior should be coupled and calculated with three basic semiconductor equations.

With continuous miniaturization of semiconductor devices operating in the deep submicron regime the more complex hydrodynamic model [17] should be used for simulation of state of the art devices. In hydrodynamic or energy balance model six PDE's (three basic semiconductor equations and three energy balance equations) should be solved in the coupled mode. The individual free electron and hole temperatures T_n and T_p not equal to the lattice temperature T_l are assumed and calculated from the energy balance equations.

For improvement of the simulation results, particularly for deep submicron devices the Schrödinger equation, which implements the most physically sophisticated quantization model characterizing the tunneling and other quantum-mechanical effects in analyzed structures, should be calculated self-consistently for a more precise evaluation of the potential and free carriers distribution.

A comprehensive review of advanced electrophysical models which complexly characterize the properties and behavior of semiconductor structures and devices can be found in the user manual of simulator DESSIS [18]. Its user friendly interactive graphical environment allows continuous improvement and modification of models and their parameters.

To enlarge the capability, the most advanced simulators provide a mixed mode support for simulation of single or multiple mesh based structures in a circuit with devices defined by SPICE models. For the transient mode of simulation, the device properties are re-solved at any increment of time.

They in general support different device geometries and contain sophisticated nonlinear solvers for numerical simulation. The mesh of nodes should be optimized for any given device structure and type of simulation to get a desired accuracy and efficiency of simulation. The adaptive mesh generators provide densest meshes in the regions with the high gradients of impurities, potential, high current density and curved structures. For example, the simulation of MOSFET requires a very dense mesh in the channel under the gate oxide interface, particularly in the drain region, where the electric field has its highest value (Figure 2).

The influence of the used model (drift-diffusion, thermodynamic, and hydrodynamic) on the output and transfer characteristics of the $1\,\mu$m and

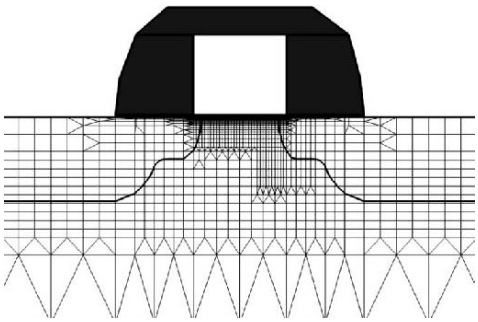

Figure 2. Mesh with non-homogeneous density of nodes of a 0.18 μm NMOSFET.

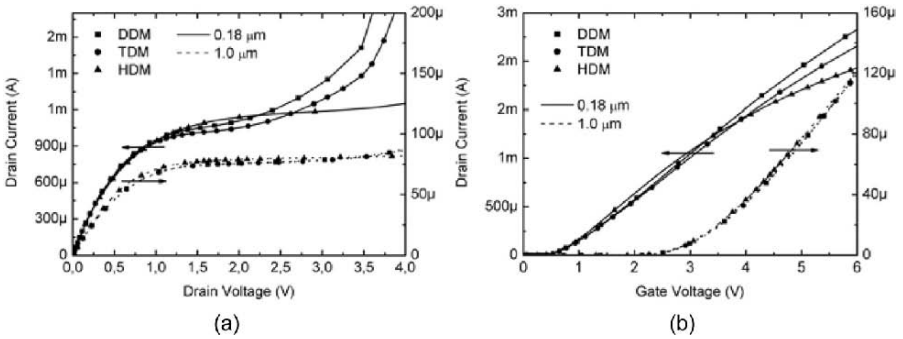

Figure 3. (a) Transfer and (b) output characteristics of a 1 μm and 0.18 μm NMOSFET calculated by drift-diffusion, thermodynamic and hydrodynamic models.

0.18 μm transistors are shown in Figure 3. While the simulated results are similar for all models for 1 μm structure, we can see a big discrepancy for 0.18 μm structure, particularly for a high electrical field, where impact ionization for the drift-diffusion model is overestimated. Therefore the use of the hydrodynamic model for a deep submicron structure is a must.

A unique advantage of process and device simulation is the possibility of simultaneous presentation of output electrical characteristics with visualized internal properties of the analyzed semiconductor structure. Although they can be shown in 1D, 2D or 3D representation, the 2D graphs are most widely used profiles for visualization of different entities. Their correlation with the output characteristics allows analyzing the critical points and regions in the structure depending on the device layout and fabrication design and extract the parasitic devices, which are inevitable parts of many semiconductor structures and devices. Such identified parasitics can be then attributed to the non-standard malfunction behavior of semiconductor devices and IC's. Therefore, reverse engineering based on the interpretation of experimentally obtained data

supported by process and device modeling and simulation is very important not only for the design and optimization of the layout and technology for new devices but also for a better understanding of their properties and behavior.

The 3D simulations require an enormous computer capacity and also 3D visualization of the obtained data, particularly in black & white representation, is not a trivial problem. Therefore, a high degree of user expertise is a must. Nowadays the 3D process and device simulations are still subjects of interest and evaluation in advanced research laboratories, more than the widely applied tools in industrial settings.

An example of 3D thermal simulation for analysis of the temperature distribution in a silicon die is illustrated in Figure 4. Thermal Shut Down (TSD) is a common device in SMART power IC's protecting the whole device against overheating. If the temperature of TSD overcomes a critical value, the power transistor is switched off and no heat is generated any more. The knowledge of the temperature distribution within the die allows the designers to locate TSD close to the hot spots and adjust the appropriate switch off temperature. 3D simulation is necessary to model properly the thermal behavior of a real Si block and 2D and 1D cross sections provide the actual temperature in a selected position.

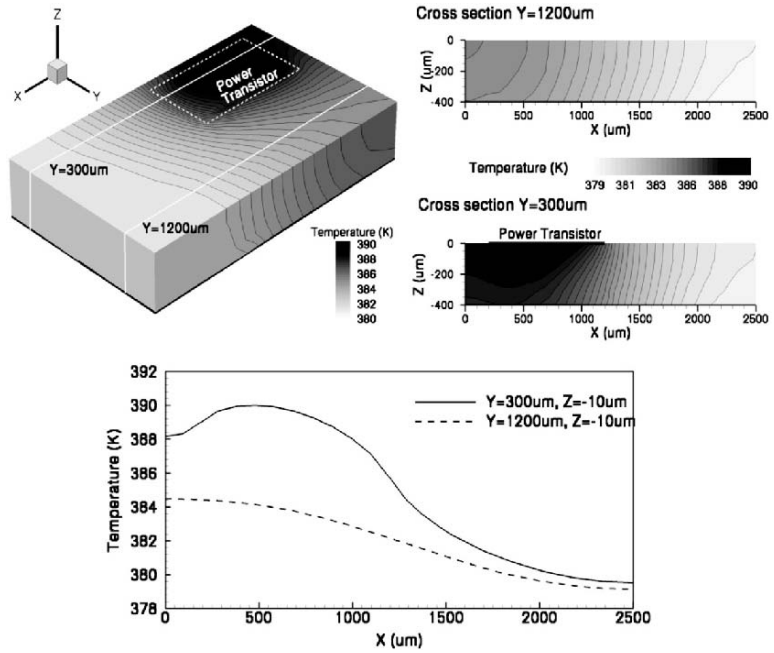

Figure 4. 3D simulation of thermal distribution within a Si block.

4. Examples

Three examples of an efficient use of 2D numerical process and device simulation in the analysis of the output electrical characteristics and extraction of parasitic devices supported by the knowledge of internal properties and behavior of the analyzed structure will be presented.

The first example shows the analysis of a bipolar transistor cell with a buried collector and reverse biased PN junction isolation, where a parasitic lateral bipolar transistor induces a steep increase of the substrate current which contributes to the base current and correspondingly degrades the transistor current gain β.

Analysis of the origin of the latch-up effect and modifications of the fabrication process and design layout of a CMOS inverter structure to increase its robustness against degradation is presented in the second example.

In the third example the complex electro-thermal behavior of a power vertical DMOS transistor multi-cell structure is analyzed, where a parasitic NPN bipolar transistor created under some circumstances generates excessive heat and due to a positive feedback degrades the power transistor.

4.1. Parasitic Lateral Bipolar Transistor in Bipolar Technology

Although the classical bipolar technology is not a mainstream of advanced semiconductor technology, it is still very popular among the designers. The use of 2D numerical process and device simulation for the analysis and interpretation of the measured static *I–V* characteristics of the bipolar NPN transistor and its behavior in the common emitter configuration, namely base, collector, and substrate currents I_b, I_c, and I_s (Gummel plot) and the extracted value of the common emitter current gain β will be presented.

Process simulation by DIOS [15] generating the structure and its doping profile (see Figure 5) and subsequent numerical solution of basic semiconductor equations using the complex physical models implemented in the device simulator DESSIS [18] is used for simulation of static *I–V* characteristics of the bipolar NPN transistor in the common emitter configuration at room temperature (Figure 6). The substrate potential kept at $V_s = -2\,\mathrm{V}$ during all simulations ensures reverse biasing of the N-type collector and P-type substrate isolation junction.

An almost ideal exponential growth is clearly seen of the base and collector currents within many orders of magnitude with corresponding negligible substrate current flowing through a reverse biased PN junction to the substrate. At high values of the base voltage, a sudden super-exponential increase of the substrate current contributes to the total base current and a kink effect in the

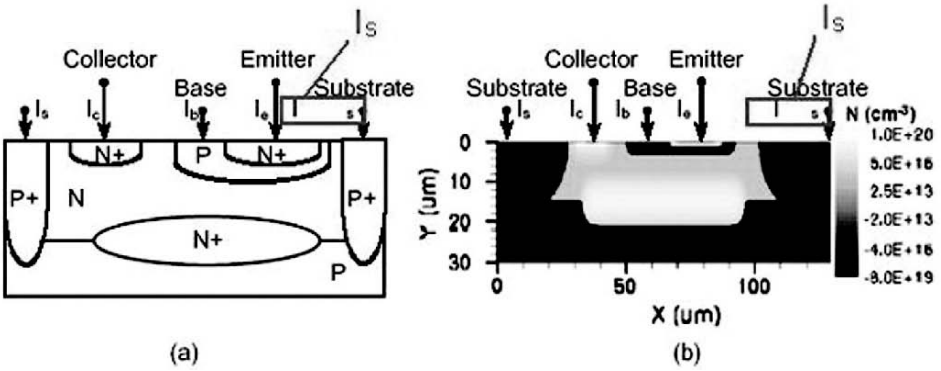

Figure 5. (a) Structure and corresponding (b) 2D doping profile of a bipolar transistor structure cell.

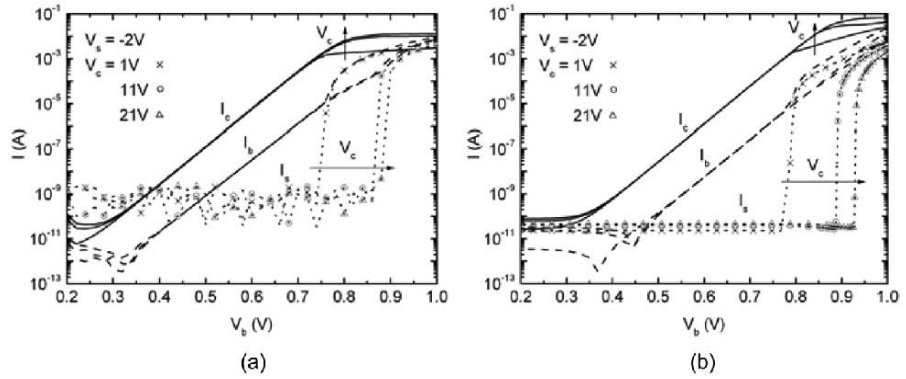

Figure 6. (a) Measured and (b) simulated base, collector and substrate currents I_b, I_c, and I_s in common emitter configuration for different collector voltages $V_c = 1, 11$ and 21 V.

base current is observed. For a proper physical interpretation of this effect, a thorough understanding of the internal behavior of the bipolar transistor cell structure is necessary.

The increasing voltage drop on the series collector resistance decreases the reverse bias of the collector-base junction located on the right side of the analyzed structure far from the collector contact (Figure 7).

For the base voltage of $V_b = 0.86\,\mathrm{V}$ the collector junction is reverse biased in the whole cross section of the analyzed structure. With increasing the base voltage to $V_b = 0.88\,\mathrm{V}$ the collector current and corresponding voltage drop on the series collector resistance increase. There is only a small reverse bias on the collector-base junction, which completely vanishes with a further increase of the base voltage ($V_b = 0.9\,\mathrm{V}$). The collector-base junction which is reverse biased during normal operation of the NPN bipolar transistor becomes open and the holes are injected from the P-type base to N-type collector at the left side of

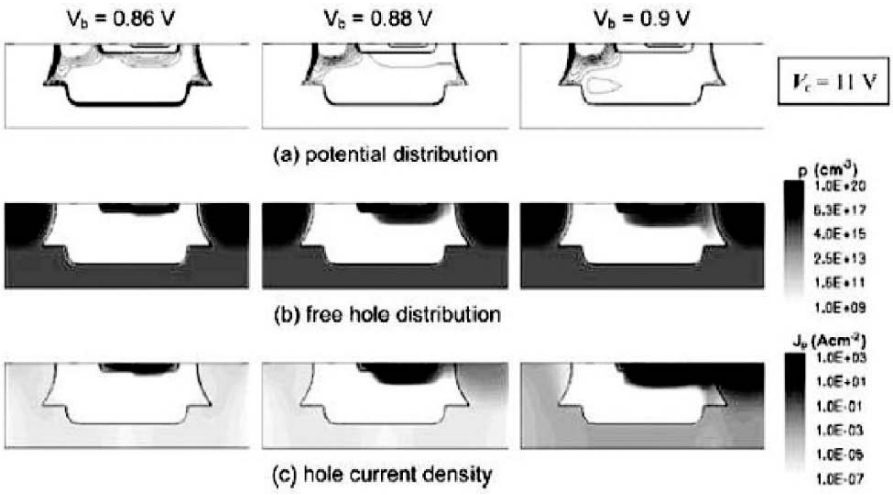

Figure 7. Visualization of the internal properties of a bipolar transistor cell.

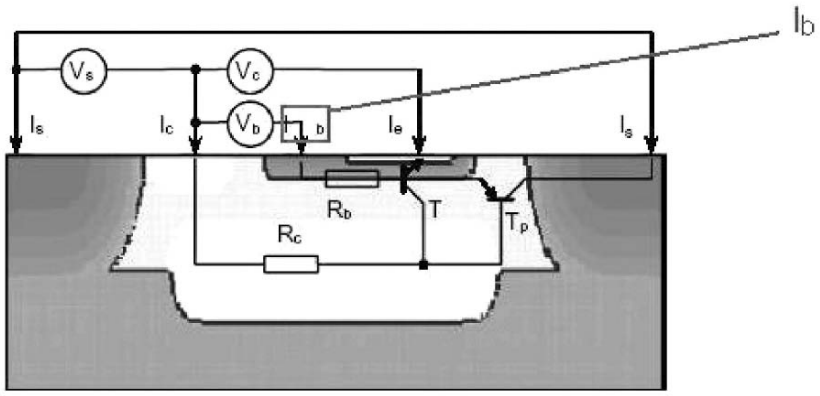

Figure 8. Structure of the bipolar transistor cell and equivalent circuit model for SPICE simulation.

the structure far from the external ohmic contact to the collector (Figure 7b). The holes injected from P-type base to N-type collector are swept by the electric field of the reverse biased junction of the P-type isolation guard ring and the N-type collector and a large hole current starts to flow into the substrate. The described behavior corresponds to the negligible substrate current for $V_b = 0.86\,\mathrm{V}$, its small increase for $V_b = 0.88\,\mathrm{V}$ and finally large increase of the substrate current for $V_b = 0.9\,\mathrm{V}$ (Figure 7c).

Based on the above analysis, the equivalent circuit model for SPICE simulation attributed to the corresponding structure regions was derived (Figure 8) [19]. The bipolar technology with a buried collector and reverse

```
vce 1 0 DC {vc}
Rc 1 2 1000
vb1 4 0 DC 0
Rb 4 3 100
q1 2 3 0 q172
qp 5 2 3 q173
vs 5 0 DC -2
.model q172 npn bf={200+vc*2}
 + is=1e-16 ise=1e-15
.model q173 pnp bf=20
 + is=1e-16 isc=1e-10
.param vc=1
.step param vc list 1 11 21 31
.DC vb1 0 1 0.01
.print dc I (Rb) I(Rc) IC(qp)
.PROBE
```

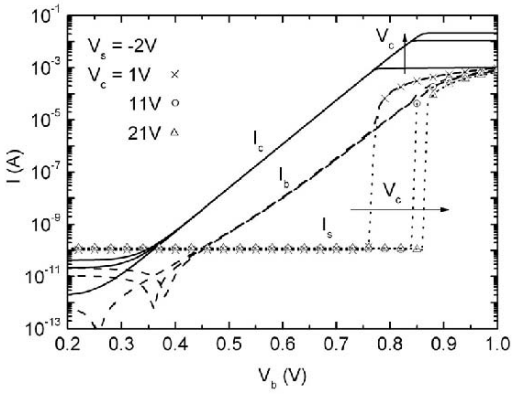

Figure 9. Input netlist and *I–V* characteristics simulated by SPICE.

biased P-type junction isolation may be characterized by a vertical active NPN bipolar transistor with its base and collector series resistances R_b and R_c, and a lateral parasitic PNP bipolar transistor merged with the active transistor. The P-type base and N-type collector of the active vertical transistor create a P-type emitter and N-type base of the parasitic lateral transistor, respectively. The amplifying effect of this parasitic lateral PNP bipolar transistor can be then considered as the origin of the sudden super-exponential growth of the substrate current at a high base voltage, when the large collector current and corresponding voltage drop on the collector series resistance for a given configuration opens the normally reverse biased collector junction of the active bipolar transistor.

The individual components and parameters of the equivalent circuit model (input netlist) for circuit simulation were estimated from 2D device simulation (Figure 9). The obtained *I–V* characteristics simulated by SPICE are in very good agreement with the results of numerical process and device simulation of the corresponding structure of the bipolar transistor as well as with the experimental results, which confirms the validity of the derived model and approach.

4.2. Latch-up Effect in CMOS Technology

The traditional scaling factor $(1/\sqrt{2})$ between successive technology generations allows unprecedented down-shrink of unipolar transistors. which has followed the Moore law [1] for more than 30 years. The key MOSFET design goal is to maximize the transistor speed, and the tradeoff is a relatively high leakage current, corresponding high power consumption and heat dissipation. Also, with MOSFET scaling it will become increasingly difficult to simultaneously

achieve a low sheet resistance for a shallow junction to ensure acceptable series resistances.

Down shrinking of the critical dimensions allows a closer location of NMOS and PMOS transistors. This invokes another problem from which the CMOS technology suffers. Particularly, the big output CMOS inverters and structures for switching applications with an inductive load are sensitive to the so-called latch up effect. We illustrate the origin of latch up on the CMOS inverter structure shown in Figure 10. The two parasitic NPN and PNP bipolar transistors created by N^+-source, P^--substrate and N^--well, and P^+-source, N^--well and P^--substrate, respectively, are clearly seen.

If the output is on logic one and the voltage drop on the series resistance R_n is high enough, the emitter of the parasitic PNP bipolar transistor becomes forward biased and injects holes to the N^--well. These holes are then swept by the electric field of the reverse biased collector junction towards the grounded substrate contact V_{ss} (Figure 11a). The hole current through the series resistance R_p can cause a voltage drop sufficient to open the emitter junction of the parasitic NPN bipolar transistor which injects the electrons to the P^--substrate (base). The injected electrons are then attracted by the electric field towards the N^--well and finally to V_{dd} contact pad (Figure 11b). The electron current increases

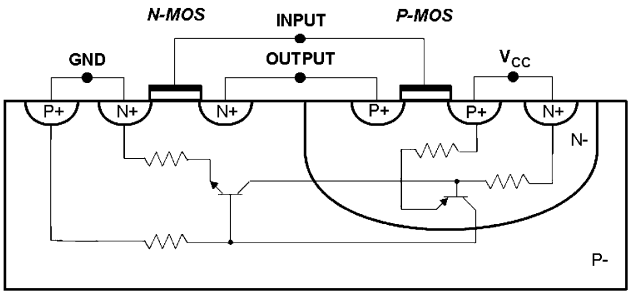

Figure 10. Cross section of CMOS inverter structure A with parasitic bipolar transistors which create a parasitic thyristor.

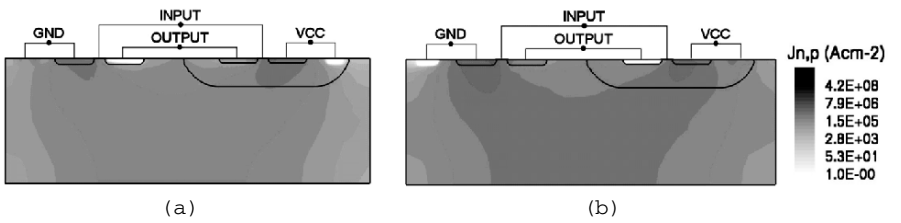

Figure 11. (a) Hole J_p and (b) electron J_n current density in a CMOS inverter structure sensitive to latch up during the trigger current pulse test.

the voltage drop on R_n resistance, which subsequently increases the forward bias of the emitter junction of the parasitic PNP bipolar transistor injecting more holes towards the ground pad V_{ss}. The created positive feedback then leads to a further increase of the total current. A high current continues to flow through structure A also when the trigger pulse is off, which may destroy the device thermally (Figure 12).

In Figure 13 the time dependent response of the output voltage, NMOS and PMOS source currents as well as N^--well and NMOS drain current to input trigger test current impulse $I = 20\,\text{mA}$ are shown. We can clearly see that the output voltage falls down to the thyristor hold voltage and will not recover to the output high value after the trigger impulse is over.

Based on the previous analysis it is clear that the layout design and doping profile should be tuned carefully to protect the device against the latch up.

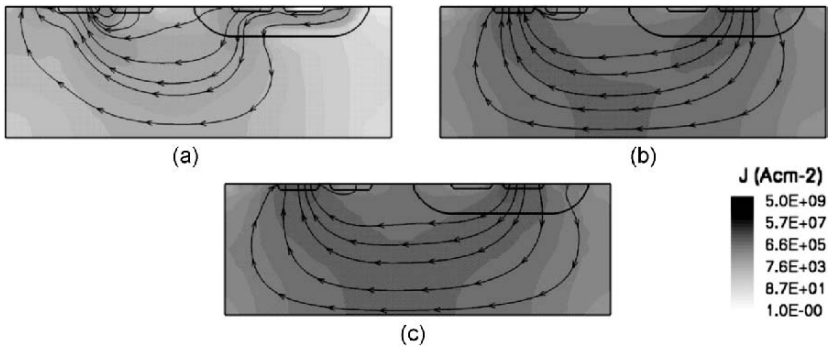

Figure 12. Total current J in a CMOS inverter structure (a) at the beginning (0,1 ms), (b) during (3 ms) and (c) after (7 ms) the trigger current pulse test.

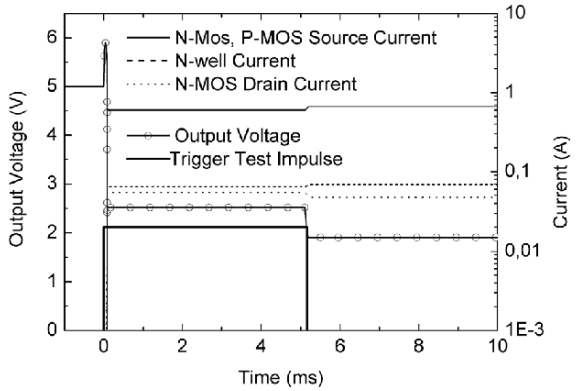

Figure 13. Resulted characteristics of latch up test with trigger current pulse $I = 20\,\text{mA}$ and corresponding output voltage for original structure.

Although there exist different approaches how to avoid or at least minimize the latch up sensitivity [20, 21], two modified structures were analyzed. The analysis followed the test procedure defined by EIA/JEDEC Standard [22], where the devices under test should survive the triggering applied current pulse $I = 100\,\text{mA}$. Interpretation of the obtained results is supported by the 2D numerical process and device simulation with visualized internal properties.

In the first modified structure B we changed the layout and added a P^+-guard ring surrounding the N-channel MOSFET and N^+-guard ring surrounding the P-channel MOSFET (Figure 14a). These guard rings act as additional base contacts of parasitic bipolar transistors and sink the collector currents without a further increase of the open emitter voltage. Although the resistivity of such a structure to the latch up effect is highly improved, it suffers from large area consumption that decreases the density of integration.

To prevent the larger area consumption the concentration profile of impurities was changed in the second modified structure C with the same layout as the original structure A. The latch up robustness was improved by introducing a highly conductive P^{++}-buried layer created on the Si substrate before epitaxial growth of the active layer (Figure 14b).

The resulting characteristics of the latch up test with a trigger current pulse $I = 100\,\text{mA}$ for modified structure C are shown in Figure 15. The output voltage is at its constant high value during the whole test except for two spikes corresponding to the times when the trigger pulse was switch on and off. Similar results were obtained for structure B. It is clear that the resistivity of both structures to latch up was increased considerably and both structures pass the EIA/JEDEC Standard current latch up test.

The internal properties of both structures during and after the trigger pulse are presented in Figure 16. The additional base contacts in structure B sink the hole and electron currents and inhibit creation of the parasitic thyristor. A similar situation is in structure C, where the hole current flows through the highly conductive buried layer and the resulted voltage drop is not sufficient to open and forward bias the NP emitter junction, which prevents formation of

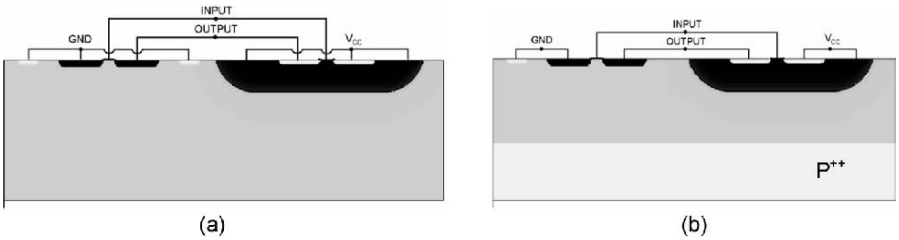

Figure 14. Cross section of the modified structure with (a) guard rings (structure B) and (b) highly conductive buried layer (structure C).

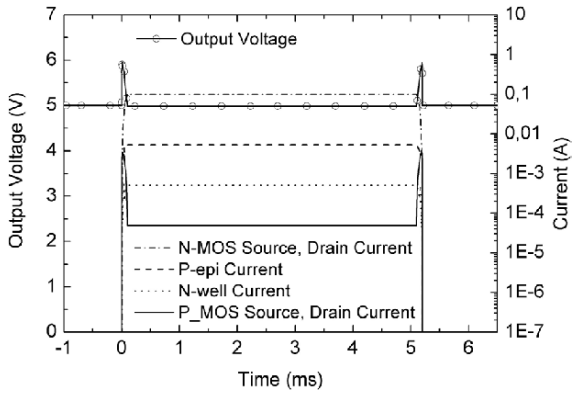

Figure 15. Resulted characteristics of latch up test with trigger current pulse $I = 100\,\text{mA}$ and corresponding output voltage for modified structure C.

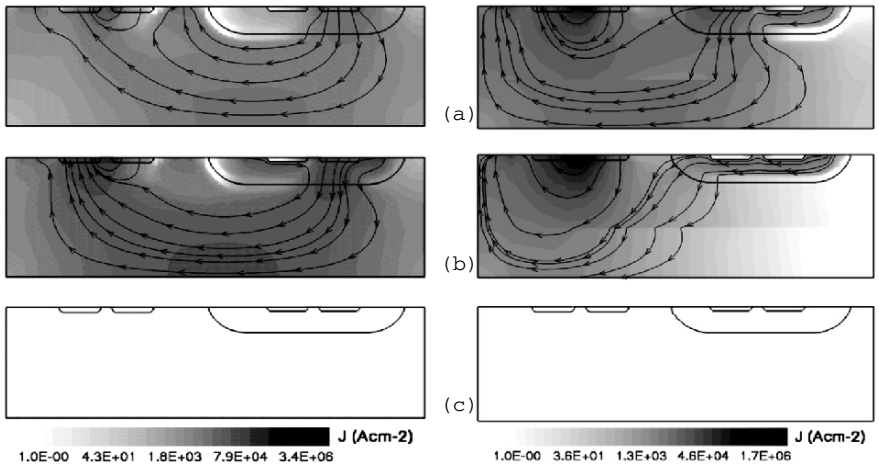

Figure 16. Total current J in a CMOS inverter for structure B (left) and structure C (right) at different time of applied trigger current pulse: (a) $t = 0, 1\,\text{ms}$, (b) $t = 3\,\text{ms}$ and (c) $t = 7\,\text{ms}$.

the positive feedback leading to device failure. We can see that after the trigger pulse the total current drops down to its steady state value for both modified structures.

The presented results of the electrical behavior of three analyzed CMOS inverter structures under latch up test confirm that the 2D process and device modeling and simulation are very efficient, time and cost effective tools for predictive parametric analysis of the sensitivity and robustness of new structures and fabrication processes to the latch up effect.

4.3. Parasitic Bipolar Transistor in Power DMOSFET Technology and its Influence on its Reliability

Many power MOSFETs applications, such as power supplies, DC-DC converters, motor drives and others require devices with a specified breakdown voltage, low on-resistance and high switching speed. For most of these applications, there is a strong demand for devices which should withstand the crucial conditions related to their implementation in switching circuits with an inductive load [23, 24]. Under such extremely harsh switching conditions, the MOSFETs must sustain a great deal of stress without causing destructive failure. The unclamped inductive switching (UIS) condition represents the circuit switching operation for evaluating the "ruggedness", which characterizes the device capability to handle high avalanche currents during the applied stress [25, 26]. We present an experimental analysis of the ruggedness of power DMOSFETs devices. The analysis is supported by the advanced 2D mixed mode device and circuit simulation, which provides a unique insight into the multicell DMOS structure operation and allows to identify the mechanism of current flow through the transistor in its off-state. Finally, creation of a parasitic bipolar transistor and electrothermal behavior of the studied structures are discussed.

The power DMOS transistor contains a large number of individual cells connected in parallel. For our analysis we used numerical simulation of the multicell structure with five adjacent cells (Figure 17). To study the device performance and energy capability, when the transistor is in off state and most of the heat is generated, we set the drain and gate voltages $V_{ds} = V_g = 0$ and assume room temperature $T = 300\,\mathrm{K}$ at the beginning of transient simulation. Hence, for studying the parasitic behavior dependent on self-heating effects, non-isothermal equations using the thermodynamic model must be

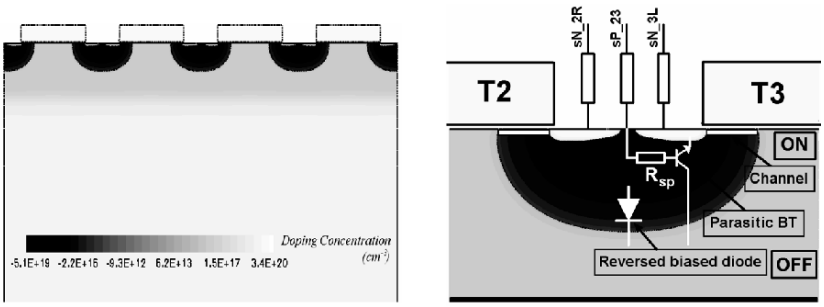

Figure 17. Multicell DMOSFET structure: (a) 2D cross-section, (b) individual cell with highlighted parasitic devices.

incorporated into the device simulation. For transient simulation the drain current I_d was ramped up to 4 mA within 1 μs and the whole simulation period is 100 μs. To obtain realistic electro-thermal characteristics we used a 18 μm wide and 300 μm thick Si block with reflecting boundary conditions at sidewalls and a thermal contact at the device bottom. We modeled the bad cell by a higher series resistance to the P-type well in 2D mixed mode simulation [27]. Such a series resistance characterizes the ohmic contact resistance to the P-well and series resistance of the current path in the P-well as in the real structure the ohmic contact is located in a distance of few μm in the 3rd direction from the analyzed 2D device cross section.

The results of 2D numerical electro-thermal simulation using the thermodynamic model are shown in Figure 18. At the very early stage of the transient simulation ($t = 0.25\,\mu s$) the drain current was homogeneously distributed within all the cells, a slightly smaller current flowed through cell No. 1 due to its higher series resistance $R_{p1} = 2\,k\Omega$ in comparison with other cells, where the resistances were set to $R_{p2-4} = 1.25\,k\Omega$ (Figure 17a). The highest current flowed through the fifth cell with $R_{p5} = 0.625\,k\Omega$. The current flows predominantly through the reverse biased PN junction at the bottom of the P-wells in the avalanche regime (Figure 19a). The highest voltage drop created at the R_{p1} (see inset of Figure 18b) at $t = 0.5\,\mu s$ was sufficient to forward bias the N-emitter and P-well junction which acts as the emitter of a parasitic bipolar NPN transistor. Thus, the conductance of the bad cell was enhanced due to the change of the mechanism and location of the current flow. The original current caused by the avalanche current of the reverse biased PN junction at the bottom of P-well was overtaken by the current of the open parasitic NPN transistor under the channel. Such a cell sinks most of the total current which generated significant Joule heat and resulted in a local temperature growth (Figure 19b). As the avalanche breakdown has a positive temperature coefficient, the drain voltage in the bad

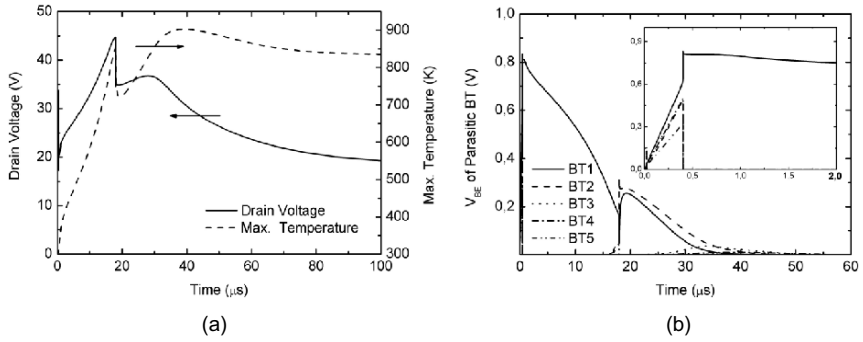

Figure 18. Transient simulation of (a) drain voltage and maximum temperature; (b) inner voltage at emitter junction of parasitic bipolar transistor.

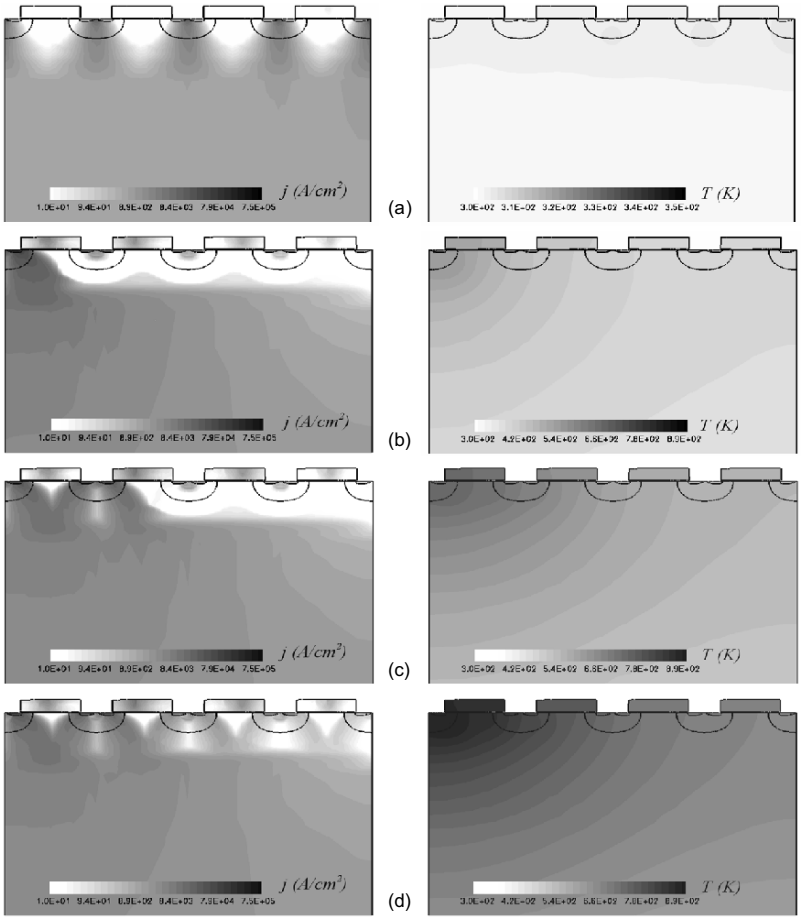

Figure 19. Current and temperature distribution in the analyzed multicell structure at (a) 0.25 μs; (b) 8 μs; (c) 21 μs, and (d) 40 μs.

cell increased further, which was followed by a further temperature growth. The temperature gradient resulted in the heat flow and the closest neighbor cell was heated up above the critical temperature when the second parasitic bipolar transistor in cell No. 2 was opened due to the decrease of the built-in voltage V_{bi} of the emitter-base PN junction with increasing temperature. The non-negligible current started to flow through cell No. 2, which reduced the current via cell No. 1. As a consequence, the generated Joule heat in cell No. 1 decreased and a kink in the drain voltage and maximum temperature can be seen in Figure 2 at elapsed time $t = 21\,\mu$s (Figure 19c). Later, a process similar to that described above took place in cell No. 2, which resulted in a further increase of the drain voltage and local maximum temperature. Due to the heat

transfer the next cells were also heated up and started to conduct higher currents (Figure 19d), which again slightly decreased the total maximum temperature and particularly the drain voltage (Figure 18a). Although oscillations in the drain voltage and maximum temperature appeared during transient simulation of the multicell structure, their physical significance is questionable because the maximum temperature already reached $T \approx 900\,\mathrm{K}$, which should be assumed as a critical temperature for the local destruction of the device [28].

Formation of the parasitic NPN bipolar transistor is a serious concern of the device performance during UIS test. In case the current flowing through an inductance is quickly turned off, the magnetic field induces a counter electromagnetic force (EMF) that can build up surprisingly high potentials across the switch (device under test). The total buildup voltage of this induced potential may far exceed the nominal breakdown voltage $V_{(BR)DSS}$ and energy capability of the transistor, thus resulting in a catastrophic failure [29, 30]. Figure 20 shows a simplified UIS test circuit and corresponding current and voltage waveforms of the tested device under UIS conditions.

The device under test was a conventional vertical DMOS transistor with breakdown voltage $V_{(BR)DSS} = 25\,\mathrm{V}$ and single pulse drain-to-source avalanche energy $E = 733\,\mathrm{mJ}$. Standard test conditions $V_{DD} = 20\,\mathrm{V}$, $L = 1\,\mathrm{mH}$, $V_G = 10\,\mathrm{V}$, and $R_G = 25\,\Omega$ were used for measurement and mixed mode electro-thermal simulations. As the behavior of the DMOS transistor under stress is very complex and depends on combined electro-thermal effects, it is necessary to model correctly the experimental device for non-isothermal simulations. While a few μm thick structure is sufficient for electrical simulations, much thicker silicon substrates ($\approx 100\,\mu\mathrm{m}$) must be used for thermal simulations and a tradeoff is a relatively long CPU elapsed time and memory. As the time of the UIS test is very short in ms range, we neglected the thermal conductivity of the package and set the constant boundary temperature $T = 300\,\mathrm{K}$ at the bottom of the structure.

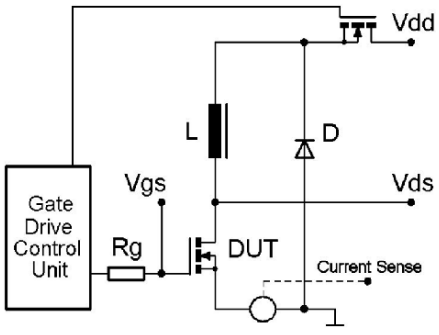

Figure 20. Simple UIS test circuit and corresponding voltage and current waveforms.

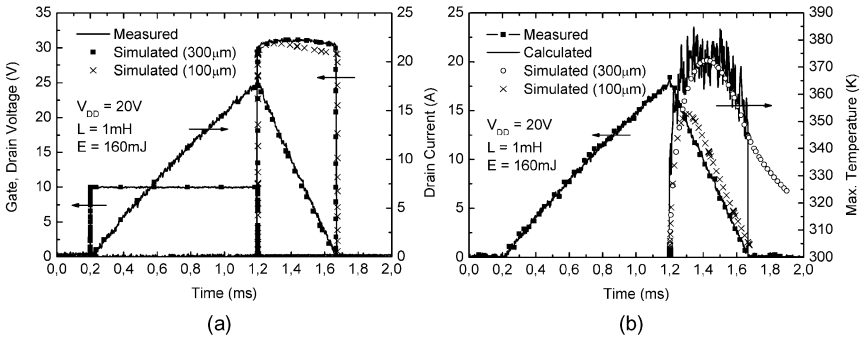

Figure 21. UIS test: (a) measured and simulated waveforms, (b) temperature evolution.

Figure 21 shows the measured and simulated device output current and voltage waveforms and maximum device temperature under UIS test with applied energy of 160 mJ for two structures. They differ in the thickness of the silicon block, the first one had the Si thickness of 100 μm and the second one was 300 μm thick. The experimental device temperature was calculated from the temperature dependence of the static drain-to-source avalanche breakdown voltage $V_{BR(DSS)}$ [31]. Hence, a relatively high noise in the temperature curve can be seen and we have information about the device temperature only during the avalanche regime. However, during the switch-off phase, a high voltage appeared across the device and high current flowed through the device, which caused a great deal of self-heating. It can be seen from the device drain voltage waveform (Figure 21) that the breakdown voltage rises above the starting breakdown voltage value. We can clearly see how important is a proper definition of the geometry of the analyzed structure for non-isothermal simulation. While the simulated electrical characteristics are almost similar for both structures, only a small difference in $V_{(BR)DSS}$ is observable, there is a considerable discrepancy between experimental and simulated maximum temperature dependences with time for the 100 μm thick structure while the agreement for 300 μm structure is excellent.

Figure 22 shows the simulated current, voltage, and temperature waveforms for two different energies during the off state phase of UIS test when the inductor was discharged. For energy $E = 800$ mJ the current related to the reverse biased PN junction at the bottom of the P-well (see Figure 17b) flowed predominantly through the P-well contact, while the current flow through the N-source contact was negligible. However, for energy $E = 1000$ mJ the voltage drop of the drain voltage during the avalanche breakdown can be clearly seen. This voltage drop was caused by opening of the parasitic BJT as indicated by the increased current through N-source and correspondingly decreased current through P-well (Figure 22b). The continuous decrease of the drain current

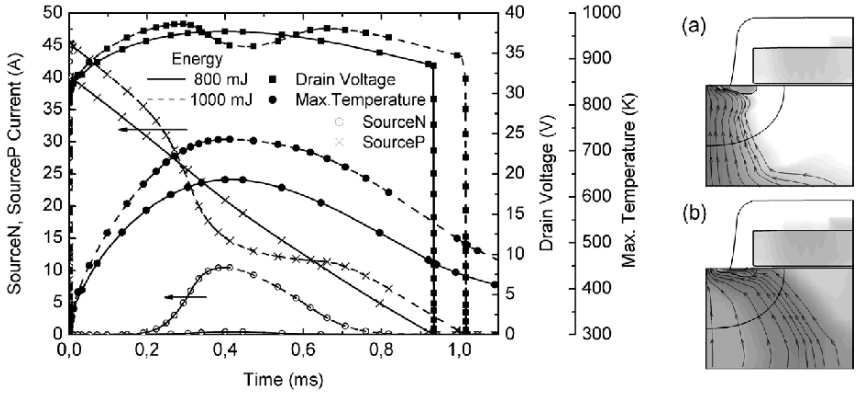

Figure 22. Simulated waveforms of UIS test for different energies (left), detail of the current flow pass in device structure under avalanche breakdown at $t = 0.4$ ms (right): (a) 800 mJ and (b) 1000 mJ.

generated less heat, which resulted in a decrease of the maximum device temperature. Consequently, the parasitic BJT was switched off and the current flowed again through the P-well contact until all energy accumulated in the inductor was dissipated. Numerical simulations with different energies can help to determine the maximum energy which the device can sustain in an ideal case of operation and the behavior and properties of various new structures can be predicted [32, 33].

5. Conclusions

The presented three examples of 2D process and device simulation show how extremely useful tools they are for the analysis, characterization and optimization of fabrication processes and corresponding electro-thermal properties of semiconductor structures and devices. The results of the process and device simulations based on the numerical solution of basic semiconductor equations with complex electro-physical models provide a unique insight into the internal operation of the analyzed devices. Visualization of the internal electrical, thermal, optical, magnetic and mechanical properties allows comprehensive analysis of the critical regions and weak points of the analyzed structures. 2/3D modeling and simulation considerably contribute to a better understanding of the physics of the formation and behavior of parasitic devices that exist as inevitable parts of active devices and degrade their normal operation and reliability. Based on the obtained knowledge, new structures and devices with a modified layout and concentration profiles can be designed and verified.

We report on excellent agreement between the measured and simulated results. Hence, TCAD simulators with properly selected calibrated physical models and defined structures are very fast and cost effective tools for parametric predictive analysis of new technologies, structures and devices integrated in IC's, and also for the physical interpretation of their properties and behavior. The user friendly interactive environment of commercially available TCAD process and device simulators supports their wide use by anybody who is interested in a better understanding of the complex structure and device behavior under various stress conditions.

The key goal of the further development of TCAD tools is to get a time and cost effective vehicle which will provide true simulated results based on more complex physical implemented models, denser structures and/or 3D simulations, and the tradeoff is relatively high CPU time and memory consumption. The problem of getting results with acceptable precision by selection of appropriate models and structures in adequate time must be resolved and optimized for each specific situation.

Acknowledgement

The authors are grateful to Wladek Grabinski for his continuous encouragement in this work. Research on certain topics discussed in this chapter was supported by project APVT 20/0139/02 of the Science and Technology Assistance Agency and grant VEGA 1/2041/05 of the Slovak Ministry of Education.

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