25

Stress Analysis for Processed Silicon Wafers and Packaged Micro-devices

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25.1. INTRINSIC STRESS DUE TO SEMICONDUCTOR WAFER PROCESSING

For quality control and reliability analysis in semiconductor product development, it is important to be able to determine the intrinsic stresses in the devices and interconnects due to various wafer processes. These processing steps include thin film deposition, plating, patterning, etching and heat treatment [1]. The local intrinsic stress built up in the devices, which is closely related to the wafer processes, is one of the major causes of low manufacturing yield and early failures in semiconductor products.

Currently, there are no effective tools that can characterize and monitor the local intrinsic stress induced by wafer processes. Average intrinsic stresses in thin films on a wafer are measured indirectly by the FLEXUS machine (KLA-Tencor Corporation, San Jose, CA) based on the Stoney's equation [5–7]. The FLEXUS machine is widely used in thin film stress analysis treating whole wafers as substrates (the thin film carrier). This approach can only provide information about the intrinsic stress in thin films of large dimensions. It is not capable of determining the intrinsic stresses in the thin films of small dimensions, such as bond pads and UBMs (under bump metallurgy). Other existing methods for intrinsic stress measurements are the X-ray diffraction and Raman microscopy [8–11]. The best spatial resolution of the X-ray diffraction is about 30 μm, which is not enough to determine the stress distribution at a local area especially when the strain gradient is high. The Raman microscopy has a spatial resolution of about 1 μm. However, it is only effective for single crystal materials. And it does not provide whole-field stress maps, which are very important in the analysis of stress distributions. Both methods need a stress free state as reference. This is not always available under actual manufacturing conditions. In addition, both methods require sophisticated measuring instruments and typically can not be used for on-site monitoring and measuring during wafer processing.

In this section, a novel testing methodology to evaluate the whole-field intrinsic stress is presented. Using this methodology, a comprehensive study of a Ni plating process is conducted. The testing structure consists of a Si membrane with SiO_2 and $Si_xN_yH_z$ buffer

layer on top, which is used in the pressure sensor applications. The thin film material and the plating are processed on the top of the Si membrane using the regular device processing. The Si membrane deformation caused by the intrinsic stresses from the plating process is measured by an optical method. A finite element model is then used to calculate the intrinsic stress and the resulting full field stress distribution in the thin film and the Si membrane using the input from the measured membrane deformation.

25.1.1. Testing Device Structure

As shown in Figure 25.1, a sensing device wafer is, essentially, a pressure sensor wafer of specified membrane thickness. Either the whole pressure sensor wafer or a single sensing chip can be used for the monitoring and testing functions. The sensing wafer (or chip) is put into the processes which are under investigation or being monitored. During each material deposition or other process steps in the wafer process, the membrane will deform due to the process induced intrinsic stress.

In this study, an n-type (100) Si of 22 μm thick was grown onto a p-type (100) Si wafer of 380 μm thick as the starting substrate. 3500 Å thick SiO_2 and 4000 Å thick $Si_xN_yH_z$ were deposited on top of the Si wafer as insulating layers. The Si wafer was patterned using Si_3N_4 as the etching mask. The etching stopped automatically at the n-type Si layer where a Si membrane window of 2650×2650 μm^2 was formed at the center of a die of 4214×4214 μm^2 area. This process formed a membrane with a thickness of about 23 μm. This sensing device was used to determine the intrinsic stress developed during an electroless Ni plating process. In the process, Ni films with different sizes and thickness were plated at the central portion of the sensor membranes.

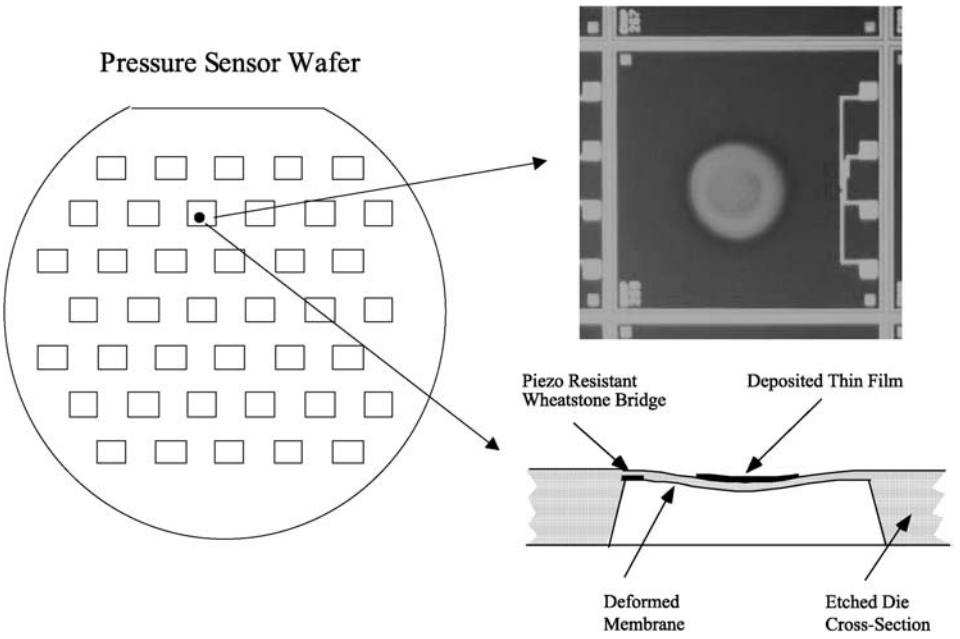


FIGURE 25.1. A sensing device wafer is essentially a Si wafer of specified membrane thickness. The membrane deformations are determined and monitored by an optical measurement technique.

25.1.2. Membrane Deformations

The deformations of the sensor membranes were determined using the Twyman-Green Interferometry technique as shown in Figure 25.2. The technique is a whole-field optical method with very high displacement sensitivity. It provides fringe patterns which are contour maps of out-of-plane displacements. The standard displacement resolution is 0.3165 μm which is one half of the wavelength of the laser used in the measurement. This optical technique has been used to measure static or dynamic deformations of Si membranes as a function of time and during progress of processes [12].

The membrane deformations were measured before and after the Ni plating process. Figure 25.3 shows the front and back view images of a membrane prior to the electroless Ni plating. The front side of the membrane is very flat. The back surface of the membrane has little variations caused by the thickness changes of the membrane as a result of the Si etching process. The Ni films are plated at the center of the Si membrane. In the fringe patterns, the out-of-plane displacement is determined from the fringe orders with a resolu-

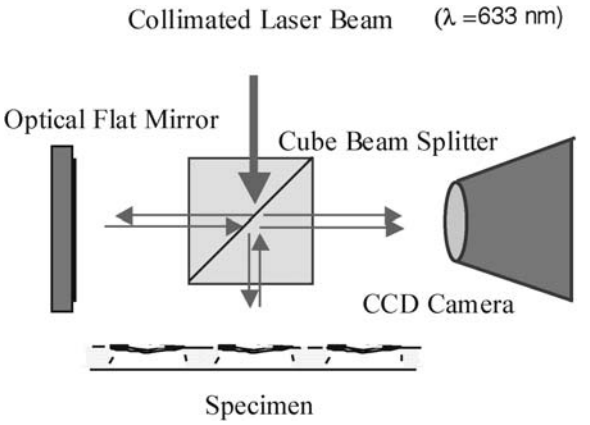


FIGURE 25.2. The deformation in the membranes of the sensor wafer is measured using the Twyman-Green interferometer.

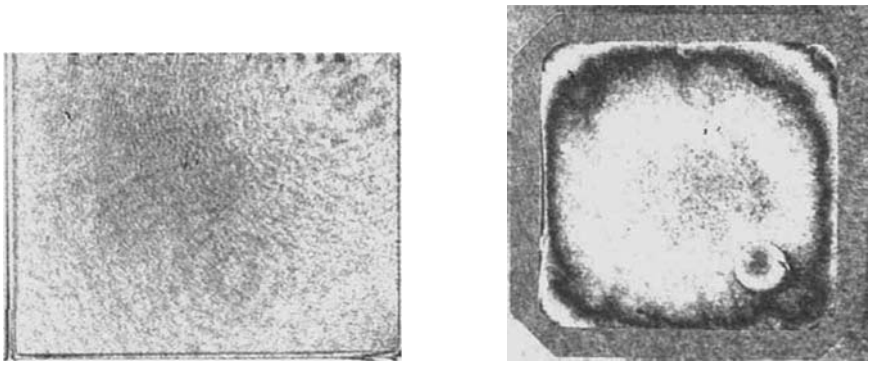
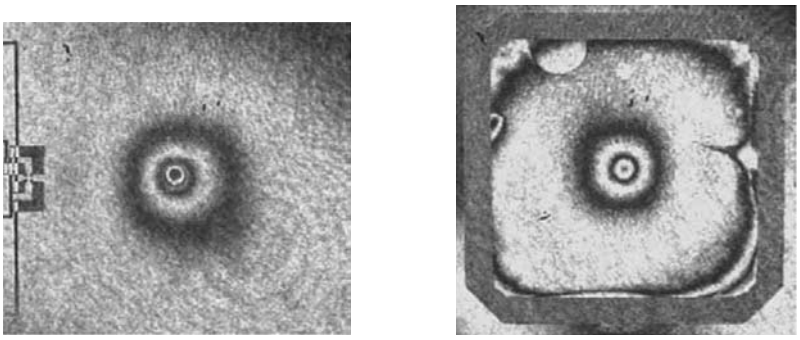


FIGURE 25.3. The front (a) and back side (b) images of a Si membrane before the electroless Ni plating.



(a) (b)

FIGURE 25.4. The membrane deformation produced by the Ni plating. Membrane deformations are measured from the front (a) and back side (b) of the membrane.

tion of 0.3165 μm. However, the resolution of this technique is not limited to 0.3165 μm. A phase-shift mechanism can be used to achieve a resolution of 1/10 of the fringe order.

The back surface of the membrane is optically reflective after the etching process. In practice, the membrane deformation can be measured from the backside of the membrane. The variation in the membrane thickness, which is measured before the plating process, as shown in Figure 25.3(b), is subtracted from the final deformation measured after the plating process. Thus, the final result is the deformation caused by the plating only. The measurement provides the whole-field deformation of the membrane including the area directly under the Ni film. However, sometimes, the etching process results in a rough surface with optical noises. In that case, the front side deformation can be used for the analysis. If the front side is used for deformation measurements, the thickness of the Ni film should be taken into consideration. If the data is taken from the backside of the membrane, the membrane thickness variation should be subtracted.

Figure 25.4 shows the typical interferometric fringe patterns obtained after the Ni plating process. The measurements were conducted at room temperature. In the experiment, membrane deformations were measured from the front and backsides of the membrane. The membrane size is 2600 × 2600 μm; membrane thickness is 23 μm; Ni film diameter is 200 μm; and Ni film thickness is 6 μm.

Since the plating temperature of the electroless Ni is at 85°C, in addition to the intrinsic stress, the measurements conducted at the room temperature will include the thermal stress caused by the Coefficient of Thermal Expansion (CTE) mismatch between the Ni and Si membrane. In order to determine the deformation induced by the intrinsic stress only, the measurements were also conducted at the plating temperature, 85°C. A hot plate with an enclosure and a glass window was used to heat the wafer and keep it at 85°C. Figure 25.5 shows the results of the measurements at the plating temperature. The images are membranes with the plated Ni films of 200, 500, 1000 and 1500 μm in diameters, respectively. The Ni thickness is 6 μm.

From the comparison of the membrane deformations obtained at the room temperature and those at the plating temperature, it was found that the deformation directions of the membranes were the same. When the measurements were conducted at room temperature, the thermal stress added into the intrinsic stress and the measurements showed that the magnitude of the deformation increased, but the deformation shape remained the same.

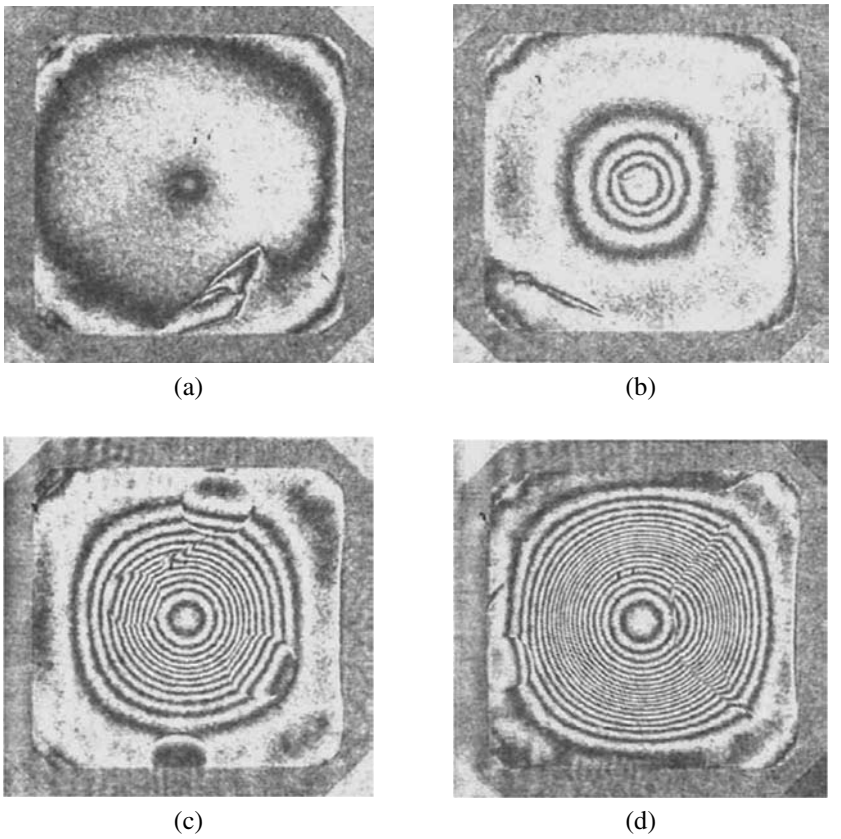


FIGURE 25.5. The membrane deformation produced by the Ni plating. The diameters of the Ni films are (a) 200 μm, (b) 500 μm, (c) 1000 μm, and (d) 1500 μm. Deformations are measured on the back surface of the membrane at 85°C, which is the plating temperature.

It means that the intrinsic stress in the Ni film has the same sign as the thermal stress in the Ni film caused by the negative ΔT (temperature decrease), which was a tensile stress.

25.1.3. Intrinsic Stress

In order to obtain the actual values of the intrinsic stresses, a finite element model (FEM) was used (Figure 25.6). With a parametric FEM model, we can model the geometry of the membrane sensing device exactly and can cover a range of wafer designs. In the process of the stress calculation, a pre-assumed intrinsic stress value was applied to the Ni film in the FEM model and the resulting membrane deformation was calculated. The membrane deformation from the FEM model was then compared with the experimentally measured membrane deformation. According to the comparison, the intrinsic stress value was adjusted in the FEM model until the deformation output from the model matched the experimental results. Figure 25.7 shows the final output of the FEM and the experimental results on the membrane deformations for the four Ni film sizes. With the right amount of intrinsic stress input in the model, the deformations output can be closely matched with the experimental results. Since all the boundary conditions are exact, the intrinsic stress in the FEM model, therefore, represents the intrinsic stress value in the Ni film.

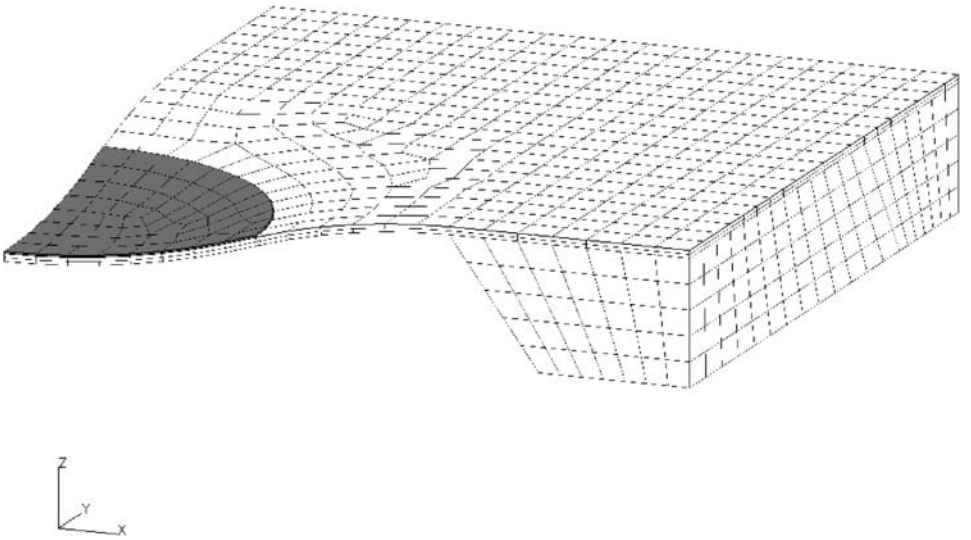


FIGURE 25.6. The FEM axisymmetric model simulated the membrane deformation with intrinsic stress input in the Ni film.

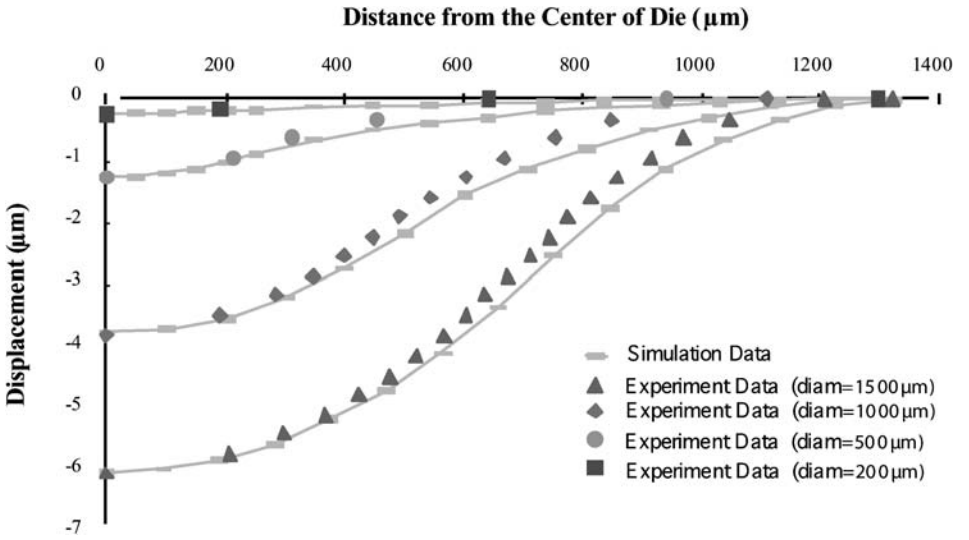


FIGURE 25.7. Experimental and FEM results on the membrane deformations for the four Ni film sizes at plating temperature.

Figure 25.8 gives the intrinsic stress values in the four Ni films with diameters of 200, 500, 1000 and 1500 μm. It is clear that the intrinsic stresses are dimensional sensitive. The intrinsic stresses increase as the Ni film dimension increases. In the real UBM, the Ni pad size is 120 μm, and the Ni intrinsic stress is around 50 MPa.

The resulting stress distributions in the Ni and the Si membrane can also be calculated from the FEM model. Figure 25.9 shows the normal and shear stress in the Si membrane at the edges of the Ni film. The resulting stress distributions are obtained based on the

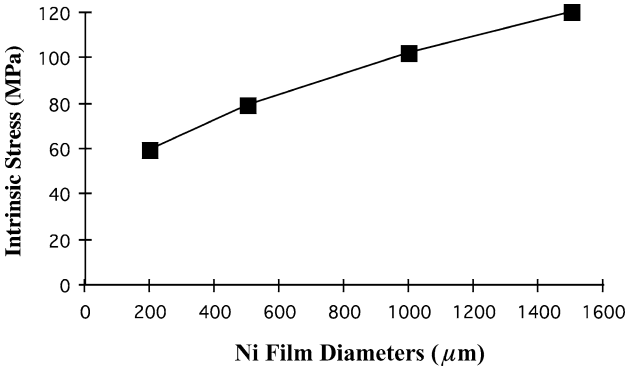


FIGURE 25.8. The intrinsic stress values in the four Ni films with different diameters. The intrinsic stress is a function of the Ni film size.

assumption that there is no Si membrane deformation before the metal was deposited. In practice, this assumption is not necessarily needed since the process induced Si membrane deformation can be obtained by subtracting the initial deformation from the final deformation after each process step.

25.1.4. Intrinsic Stress in Processed Wafer: Summary

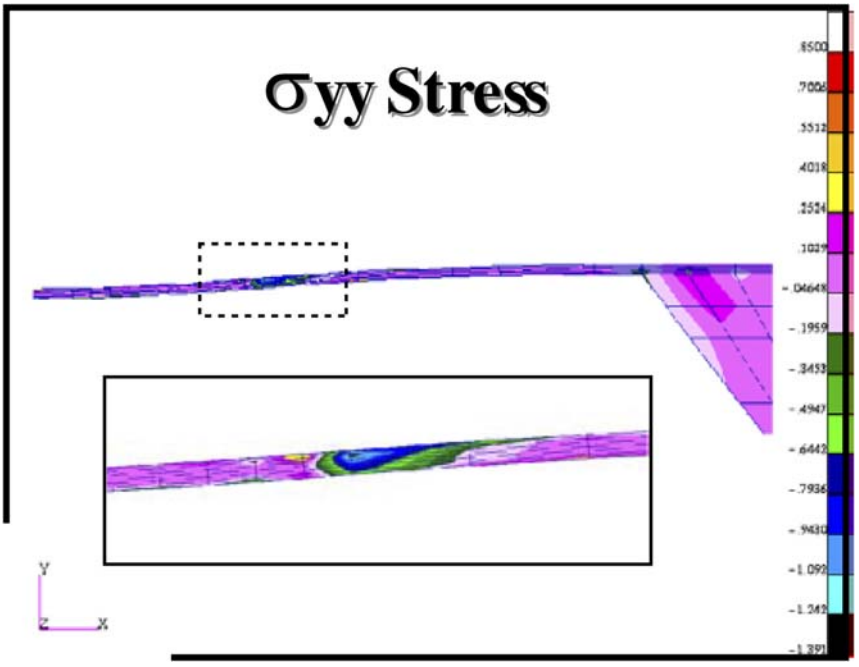
The proposed technique uses a silicon membrane to detect and display the intrinsic stress, which is the stress accumulated during the plating processes. Deformations in thin reflective Si membrane are measured accurately with laser interferometry and the stress calculations are completed by finite element method (FEM).

In the study of the electroless Ni plating process, it is found that the intrinsic stress value in the Ni film is a function of the film dimension, and the dimension dependency is very strong. As the film dimension increases, the intrinsic stress should approach the value measured by the FLEXUS machine which provides the intrinsic stress values in a thin film with a dimension close to infinity. This hypothesis is currently being verified.

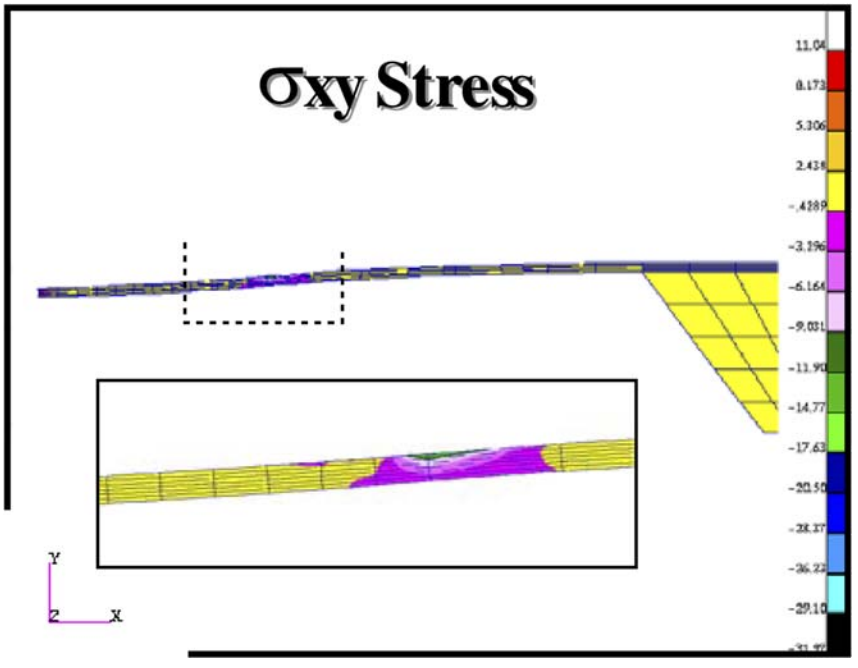
The intrinsic stress from the wafer process is a critical parameter affecting the reliability of the device, such as the bump strength, UBM (under bump metalization) strength, thin film adhesion, failure in the passivation layer and die cracking. The technique experimented should have impact on the following areas:

(a) Intrinsic stress measurements of different UBM.
(b) Process characterization, a simple technique to determine the local thin-film stress induced by metalization, deposition, plating, etching and heat treatment.
(c) In-situ monitoring of stress change in interconnect lines during electromigration and thermal migration in the accelerated testing.
(d) Local stress in active region after ion implantation (doping) and subsequent annealing.

The current technique used in the intrinsic stress measurement is the FLEXUS machine. Very often, it does not have enough sensitivity to measure the deformation if the thin film is patterned on a regular Si substrate. In practice, the Si substrates have to be thinned down to get enough sensitivity. In the FLEXUS machine, the wafer deformation is measured by the laser reflection, which can only obtain the average thin-film stress but not the



(a)



(b)

FIGURE 25.9. The normal (a) and shear stresses (b) in the silicon membrane at the interface with the Ni film by FEM analysis. High stresses are shown in the silicon membrane next to the edge of the Ni layer.

local stress variations. The proposed device with a thin membrane can provide extremely high sensitivity. By using a full field optical method, local deformations from small and various thin film geometry can be determined with very high resolution. With the aid of the FEM method, the intrinsic stress and the resulting stress field can be determined. This technique has its advantages to complement the FLEXUS machine for determinations of local stress fields caused by the intrinsic stress.

There is no practical limitation regarding the dimensions and shapes of the thin films studied. Currently, a great interest is in the area of determining the intrinsic stress in the UBM processes. In this study, the dimensional effect on intrinsic stress in the electroless Ni UBMs is analyzed. This Si membrane based testing sensor has great potentials in the wafer process characterization with high accuracy solution and a low cost. This new technology could also promise the capability to study the stress in much finer structures, such as interconnect line, stress change due to electromigration and thermal migration in interconnect lines and, more importantly, the stress at gate SiO_2/Si interface.

25.2. DIE STRESS RESULT FROM FLIP-CHIP ASSEMBLY

In flip chip plastic ball grid array (FC-PBGA) packages, silicon die is attached on a laminate substrate by solder joints. Underfill material is filled in the gap between the die and the substrate to protect the solder joints for better reliability. After the underfill process, the die and the substrate are rigidly bonded together and no interface delamination and separation should be present. A silicon die, with a coefficient of thermal expansion (CTE) of 2.6 ppm/°C, and a laminate substrate, with a CTE from 15 to 25 ppm/°C, are connected by underfill material. As a result of CTE mismatch, significant thermal stress occurs in the die and the substrate during thermal cycles. In component level reliability testing, this thermal stress is the major cause of many failure modes including die cracking. Lately in the development of FC-PBGA packages, reducing die stress and improving reliability has been a very serious issue.

25.2.1. Consistent Composite Plate Model

The flip chip package can be treated as a multilayer composite system. The consistent plate model treats the chip, the underfill and the carrier substrates, i.e., the chip/carrier module, as plies of an integrated laminated plate. The only assumptions made are those normal to thin and classical laminate plate theory [2].

The term consistent plate model comes from the assumption of consistent deformations in the chip and substrate. The strain in the system will therefore depend only on the strain on the reference plane somewhere in the middle of the plate, $\boldsymbol{\varepsilon}^0$, and the curvature of the laminated plate, $\boldsymbol{\kappa}$,

$$\begin{Bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_{xy} \end{Bmatrix} = \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \varepsilon_{xy}^0 \end{Bmatrix} + z \begin{Bmatrix} \kappa_x \\ \kappa_y \\ \kappa_{xy} \end{Bmatrix}. \tag{25.1}$$

The constitutive relation for any ply of a laminated plate is

$$\boldsymbol{\sigma} = \mathbf{Q}(\boldsymbol{\varepsilon} - \boldsymbol{\Lambda}), \tag{25.2}$$

where the stress vector $\boldsymbol{\sigma}$ and induced strain vector $\boldsymbol{\Lambda}$ are

$$\boldsymbol{\sigma} = \begin{Bmatrix} \sigma_x \\ \sigma_y \\ \sigma_{xy} \end{Bmatrix}, \quad \boldsymbol{\Lambda} = \begin{Bmatrix} \Lambda_x \\ \Lambda_y \\ \Lambda_{xy} \end{Bmatrix} = \begin{Bmatrix} \alpha_x \Delta T \\ \alpha_y \Delta T \\ \alpha_{xy} \Delta T \end{Bmatrix}. \tag{25.3}$$

Here α is the coefficient of thermal expansion and ΔT is the temperature change.

The matrix $\mathbf{Q}$ is the transformed reduced stiffness of the lamina and is given by Ref. [4] as following

$$\mathbf{Q} = \begin{Bmatrix} \overline{Q}_{11} & \overline{Q}_{12} & \overline{Q}_{16} \\ \overline{Q}_{12} & \overline{Q}_{22} & \overline{Q}_{16} \\ \overline{Q}_{16} & \overline{Q}_{16} & \overline{Q}_{66} \end{Bmatrix}. \tag{25.4}$$

The load-deformation relationship for the consistent plate is given by

$$\begin{bmatrix} \mathbf{N} \\ \mathbf{M} \end{bmatrix} = \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{B} & \mathbf{D} \end{bmatrix} \begin{Bmatrix} \boldsymbol{\varepsilon}^0 \\ \boldsymbol{\kappa} \end{Bmatrix} - \begin{bmatrix} \mathbf{N}^\Lambda \\ \mathbf{M}^\Lambda \end{bmatrix}, \tag{25.5}$$

where the conventional mechanical stress resultants, the mechanical forces and moments, are

$$\mathbf{N} = \int_t \boldsymbol{\sigma} dz, \tag{25.6}$$

$$\mathbf{M} = \int_t \boldsymbol{\sigma} z dz. \tag{25.7}$$

The matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{D}$ are the usual extensional stiffness, bending-stretching coupling stiffness and bending stiffness of the plate [4]. The integrations in the above equations are carried out through the composite plate thickness. The equivalent thermal forces and moments are

$$\mathbf{N}^\Lambda = \int_t \mathbf{Q}\boldsymbol{\Lambda} dz, \tag{25.8}$$

$$\mathbf{M}^\Lambda = \int_t \mathbf{Q}\boldsymbol{\Lambda} z dz. \tag{25.9}$$

The total potential energy stored in the plate is given by

$$U = \frac{1}{2} \iint_\Omega \begin{Bmatrix} \boldsymbol{\varepsilon}^0 \\ \boldsymbol{\kappa} \end{Bmatrix}^T \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{B} & \mathbf{D} \end{bmatrix} \begin{Bmatrix} \boldsymbol{\varepsilon}^0 \\ \boldsymbol{\kappa} \end{Bmatrix} d\Omega - \iint_\Omega \begin{bmatrix} \mathbf{N}^\Lambda \\ \mathbf{M}^\Lambda \end{bmatrix}^T \begin{Bmatrix} \boldsymbol{\varepsilon}^0 \\ \boldsymbol{\kappa} \end{Bmatrix} d\Omega. \tag{25.10}$$

This strain energy equation together with a Ritz approximate solution method can be used to solve for the approximate strains and curvatures in the multilayer system.

25.2.2. Free Thermal Deformation

When there is no external mechanical load, Equation (25.5) can be reduced to

$$\begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{B} & \mathbf{D} \end{bmatrix} \begin{Bmatrix} \boldsymbol{\varepsilon}^0 \\ \boldsymbol{\kappa} \end{Bmatrix} = \begin{bmatrix} \mathbf{N}^\Lambda \\ \mathbf{M}^\Lambda \end{bmatrix}. \tag{25.11}$$

Equation (25.11) can be solved directly for $\boldsymbol{\varepsilon}^0$ and $\boldsymbol{\kappa}$.

As shown in Figure 25.10, three special cases are of particular interests for electronics packaging analysis, namely, the beam bending, the cylindrical bending and the axisymmetrical bending. When material anisotropy for each layer is small, Equation (25.4) can be written as

$$\mathbf{Q} = \begin{Bmatrix} \dfrac{E_i}{1-\nu_i^2} & \dfrac{\nu_i E_i}{1-\nu_i^2} & 0 \\ \dfrac{\nu_i E_i}{1-\nu_i^2} & \dfrac{E_i}{1-\nu_i^2} & 0 \\ 0 & 0 & \dfrac{E_i}{2(1+\nu_i)} \end{Bmatrix}. \tag{25.12}$$

Here E_i and ν_i are the Young's modulus and Poisson's ratio for the ith layer lamina. Note Equation (25.12) is given for the axisymmetrical case. For the cylindrical and beam bending cases, we can simply replace the term $E_i/(1-\nu_i)$ with E_i.

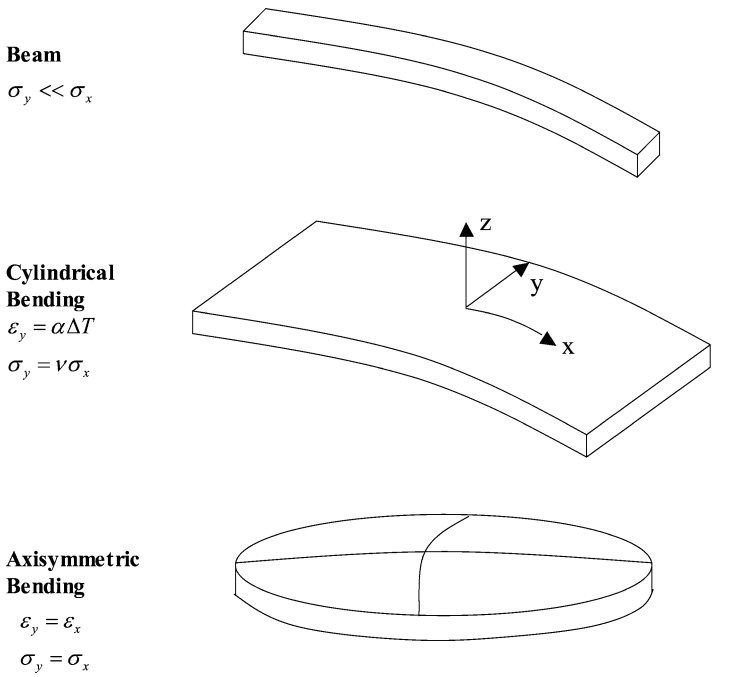


FIGURE 25.10. Three possible deformation modes for multilayered structures.

The deformation of the composite plate can be further simplified such that for beam bending,

$$\sigma_y \ll \sigma_x;$$

for cylindrical bending,

$$\begin{Bmatrix} \kappa_x \\ \kappa_y \\ \kappa_{xy} \end{Bmatrix} = \begin{Bmatrix} \kappa_x \\ 0 \\ 0 \end{Bmatrix}, \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \varepsilon_{xy}^0 \end{Bmatrix} = \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ 0 \end{Bmatrix},$$

for axisymmetrical bending,

$$\begin{Bmatrix} \kappa_x \\ \kappa_y \\ \kappa_{xy} \end{Bmatrix} = \begin{Bmatrix} \kappa_x \\ \kappa_x \\ 0 \end{Bmatrix}, \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \varepsilon_{xy}^0 \end{Bmatrix} = \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_x^0 \\ 0 \end{Bmatrix}.$$

The force and the moment equations for the above three cases become

$$\begin{bmatrix} A_x & B_x \\ B_x & D_x \end{bmatrix} \begin{Bmatrix} \varepsilon_x^0 \\ \kappa_x \end{Bmatrix} = \begin{bmatrix} N_x^\Lambda \\ M_x^\Lambda \end{bmatrix}. \tag{25.13}$$

Here coefficients A_x, B_x, D_x, N_x^Λ and M_x^Λ are given by the following equations [2,3]

$$\begin{cases} A_x = \displaystyle\int_t \frac{E_i}{1-\nu_i} dz \\ B_x = \displaystyle\int_t \frac{E_i}{1-\nu_i} z dz \\ D_x = \displaystyle\int_t \frac{E_i}{1-\nu_i} z^2 dz \\ N_x^\Lambda = \displaystyle\int_t \frac{E_i \alpha_i \Delta T}{1-\nu_i} z dz \\ M_x^\Lambda = \displaystyle\int_t \frac{E_i \alpha_i \Delta T}{1-\nu_i} z dz. \end{cases} \tag{25.14}$$

Again, Equation (25.14) is given for the axisymmetrical case. For cylindrical and beam bending cases, we simply replace the term $E_i/(1-\nu_i)$ with E_i in the above equation.

25.2.3. Bimaterial Plate (BMP) Case

As an example, we consider a flip chip package shown in Figure 25.11. Using the consistent composite plate model, the flip-chip package can be treated as a system of two plates bonded together if only the die bending curvature and the stress on top of the die is interested. The underfill and solder joins can be treated as part of the substrate in this scenario. The Young's modulus, Poisson's ratio, CTE and thickness of upper plate (plate 1 or die) are E_1, ν_1, α_1, h_1, respectively (Figure 25.12). The corresponding quantities for

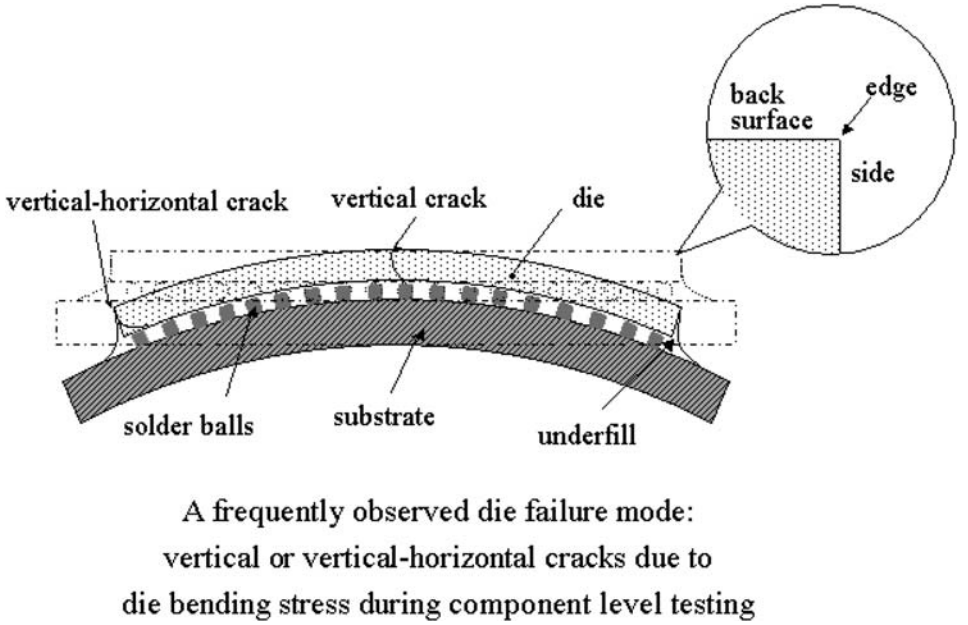


FIGURE 25.11. A schematic diagram of a flip-chip plastic ball grid array package and die failure modes due to die bending. The dashed lines represent the package at underfill curing temperature, which is stress free. The solid lines represent the package at room temperature, at which the package bends due to the CTE mismatch between the die and the substrate.

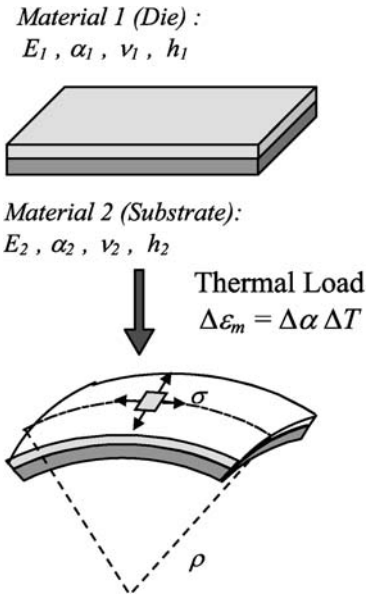


FIGURE 25.12. Bimaterial plate model for a flip chip module.

the lower plate (plate 2 or substrate) are E_2, ν_2, α_2, h_2, respectively. In the flip chip package, the two plates were bonded together at a certain temperature T_0. The bimaterial plate (BMP) system will bend into a surface which is part of a sphere when temperature is reduced to T (Figure 25.12). Solving Equation (25.13) for the BMP system, we have

$$\begin{cases} \varepsilon_x^0 = \dfrac{D_x N_x^\Lambda - B_x M_x^\Lambda}{A_x D_x - B_x^2} \\ \kappa_x = \dfrac{A_x M_x^\Lambda - B_x N_x^\Lambda}{A_x D_x - B_x^2}. \end{cases} \tag{25.15}$$

Please note that ε_x^0 is dependent on the location of x–y plane while κ_x is consistent through the plate thickness. Substituting Equation (25.14) into Equation (25.15) and after some mathematical manipulations we have

$$\begin{cases} \varepsilon_x^0 = \dfrac{hm(4+3h+h^3m)(\alpha_2+\alpha_1)\Delta T}{(1+hm(4+6h+4h^2+h^3m))} \\ \kappa_x = \dfrac{6\varepsilon_m hm(1+h)}{h_1(1+hm(4+6h+4h^2+h^3m))}, \end{cases} \tag{25.16}$$

where $h = h_2/h_1$ is the thickness ratio of the lower plate to the upper plate, $m = M_2/M_1$ is the ratio of the biaxial modulus of the lower plate $[M_2 = E_2/(1-\nu_2)]$ respect to the upper plate $[M_1 = E_1/(1-\nu_1)]$, and $\varepsilon_m = (T - T_0)(\alpha_1 - \alpha_2)$ is the thermal mismatch strain between the two plates.

In practice, it is convenient to express the curvature in a dimensionless quantity or, so called, characteristic curvature:

$$\overline{\kappa} = \frac{h_1}{6\varepsilon_m}\kappa_x = \frac{hm(1+h)}{1+hm(4+6h+4h^2+h^3m)}. \tag{25.17}$$

The characteristic curvature is a function of only the thickness ratio h and the biaxial modulus ratio m.

From Equation (25.2) and Equation (25.16), the stress on the top surface of plate 1, the die, can be expressed as

$$\sigma_{top} = \frac{\varepsilon_m M_1 hm(2+3h-h^3m)}{1+hm(4+6h+4h^2+h^3m)}. \tag{25.18}$$

The stress is uniform at any point on the top of the die which is a direct result of neglecting the edge effect. The dimensionless stress or characteristic stress is defined as

$$\overline{\sigma} = \frac{\sigma_{top}}{\varepsilon_m M_1} = \frac{hm(2+3h-h^3m)}{1+hm(4+6h+4h^2+h^3m)}. \tag{25.19}$$

It is instructive to express the stress on top of the die in terms of the curvature or characteristic curvature.

$$\sigma = \kappa_x \frac{h_1 M_1(2+3h-h^3m)}{6(1+h)}, \tag{25.20}$$

$$\overline{\sigma} = \overline{\kappa}_x \frac{2 + 3h - h^3 m}{1 + h}. \tag{25.21}$$

According to Equations (25.20) and (25.21), the stress contains the curvature κ_x. Therefore, the curvature κ_x can provide direct information of the stress.

25.2.4. Validation of the Bimaterial Model

The mechanical behavior of the FC-PBGA package is similar to a mechanical system with two bonded plates. A bimaterial laminate model can be used to estimate the stress and bending curvature in each plate. The bimaterial plate model (BMP) has been widely used in the stress determinations of the wafer level process with thin films deposited on silicon wafers. With the thin film approximation, which is known as Stoney's equation [13], it provides an effective method to determine the stresses in thin films deposited on wafers [14]. However, this model can not be directly applied to the FC-PBGA packages because of the assumptions in the model that the film is much thinner than the wafer. In practice, the die stress in the FC-PBGA packages is usually determined from finite element method (FEM) models which require simulation tools and are comparatively time consuming when packages with different geometry are analyzed.

A typical FC-PBGA package is shown in Figure 25.11. In the assembly process, the die is attached to the substrate through solder joints. The die attach process does not produce high die stress because of the creep and relaxation in the solder joints. Most of the die stress is produced by the underfill process. When the underfill material is cured at high temperature (usually 150 to 170°C), the die and the substrate is connected. As the package cools down to room temperature, the thermal stress accumulates because of the CTE mismatch between the die and the substrate. A bending deformation is developed by cooling the package from the underfill curing temperature to room temperature. Further cooling to lower temperature in the reliability test will induce more package bending and higher die stress. During the package qualification, thermal cycles from −55 to 125°C are used for the package level test.

In a real package, the underfill material is adhered to the die and substrate, the degree of the creep and relaxation is not significant in the underfill material when it is fully cured. The stress free temperature of the system is near the underfill curing temperature. When the package is thermally cycled, the thermal stress in the die can cause several failure modes in die cracking at the low temperature. Figure 25.11 also shows the failure due to die cracking that have been identified during the reliability tests: (a) vertical crack, the crack initiated from the die back side and propagated vertically down into the die, (b) vertical-horizontal crack, the crack initiated from the back side propagated vertically first then turned to horizontal. The BMP model developed can be applied in the study of these two types of die cracks.

The tensile stress at the backside of the die is obviously the cause of the vertical cracks initiated from the backside. It is clear that the back surface of the die is in tension. The cracks are initiated from the back surface or the edges of the back surface and across the die from edge to edge. The depth of the crack depends on the stress level in the package. Simulation shows that the tensile stress at the backside of the die is distributed almost over entire back surface.

The BMP model is validated by experiments and finite element method (FEM). The curvature was directly validated by curvature measurement using an optical method. The stress calculated from the BMP model was compared with FEM results.

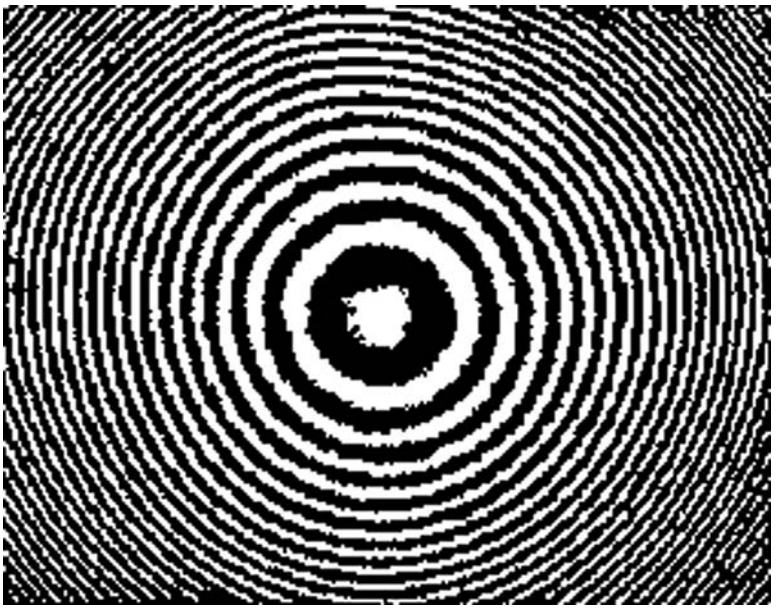


FIGURE 25.13. A typical interference fringe pattern obtained from the Si chip surface with the Twyman-Green interferometer.

In order to validate the curvature model for different thickness ratio and different materials, two sets of sample were prepared. The dice chosen in this study are single Si with (100) orientation. The dimensions are 6.78 mm × 5.50 mm × 0.54 mm. The dice are both-side polished. Substrates are printed circuit board (PCB) and Cu substrates. The dimension of the dice is kept unchanged for different samples. The thickness of the substrates varies from 0.25 times to 2 times of the die thickness for both PCB and Cu substrates. The length and the width of the substrates are kept the same as those of the dies. The die and substrate are bonded together by a thin layer of epoxy. After about 1 hour curing at 83°C, the epoxy layer firmly bonds the die and substrate. As the assemblies cool down to room temperature, bending and stress are generated due to the CTE mismatch. The thickness of the epoxy layer is less than 10 μm, which is negligible in the die bending and die stress calculation.

The curvature measurement was carried out using a Twyman-Green interferometer [15] with an *in situ* heating chamber. A typical fringe pattern of the die bending is shown in Figure 25.13. It is the interference pattern of a Si die (6.78 mm × 5.50 mm × 0.54 mm) on a 0.77 mm thick Cu substrate at 23.5°C. The package is flat at 78.5°C. The fringe pattern is a displacement contour of the sample surface. Each circular fringe corresponds to 316.4 nm out-of-plane deformation. Figure 25.13 clearly shows that the fringe pattern is consisted of concentric circles. The bimaterial plate theory treats the two plates as an axisymmetric mechanical system. The experiment proves that the deformation of the sample is indeed an axisymmetric spherical surface. It is noteworthy to point out that the zero bending temperature (78.5°C) is lower than the epoxy curing temperature 83°C in this case. The reason is that the thin epoxy layer had experienced a small stress relaxation before the test. It is crucial to check the zero bending temperature for each sample in order to get the accurate data.

The FEM calculation is carried out using the commercial software ANSYS 5.5. Two-dimensional (2D) 8-node axisymmetric solid elements were used to calculate the die bend-

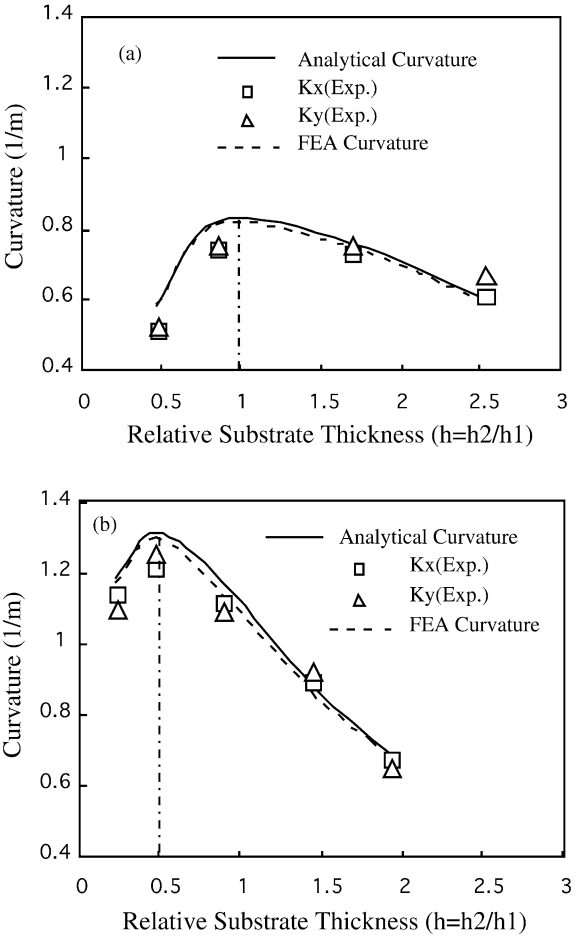


FIGURE 25.14. Bending curvatures (a) Si die on PCB substrate and (b) Si die on Cu substrate.

ing and the stress on top of the die. The FEM model treats the bimaterial plates as circular plates in order to be consistent with the analytical BMP model. Linear elastic deformation is assumed in the FEM model.

The bending curvatures from experiment measurement, BMP model and FEM are plotted in Figure 25.14. Figure 25.14(a) is the result of die on PCB substrate, and Figure 25.14(b) is the result of die on Cu substrate. The Young's modulus, Poison's ratio and CTE of Si used in the calculation are 131 GPa, 0.28 and 2.5 ppm/°C, respectively. The corresponding values are 21 GPa, 0.33, and 20 ppm/°C respectively, for PCB substrate, and 117 GPa, 0.35, and 17 ppm/°C, respectively, for Cu substrate. The experimental results of the curvature are in two orthogonal directions. The x-direction is along the length of the samples and the y-direction is along the width of the samples. The horizontal axis of the figure is the thickness ratio $h = h_2/h_1$, with the die thickness of $h_1 = 0.54$ mm fixed. For each substrate thickness, at least two samples were tested; the curvatures shown in the figure are the averaged values. Both Figure 25.14(a) and Figure 25.14(b) clearly show that the calculated curvatures from both BMP and FEM agree well with the experimentally mea-

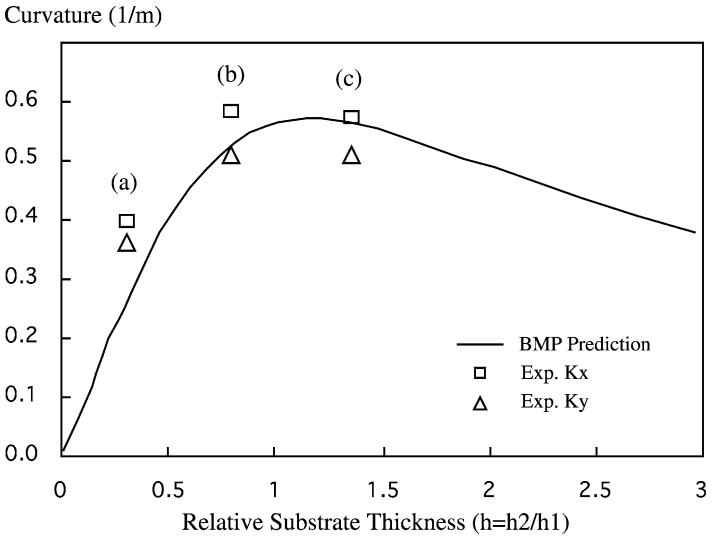


FIGURE 25.15. Curvature measured by Twyman-Green interferometer and calculated by BMP model for flip-chip packages.

sured curvatures. The curvatures of the two orthogonal directions are the same from the experimental measurement.

A very interesting feature shown in Figure 25.14(a) and Figure 25.14(b) is that there is a maximum bending curvature in both substrate systems. For PCB substrates, the maximum bending curvature occurs when the substrate to die thickness ratio equals to one, and the corresponding value for the Cu substrate occurs when the substrate to die thickness ratio equals to 0.5. This maximum bending curvature should be avoided in package design in order to reduce the package bending and die stress.

A set of real FC-PBGA packages was also tested. The die dimension is 7.0 mm $\times$ 6.5 mm $\times$ 0.61 mm. The underfill has a thickness of 0.13 mm. Figure 25.15 shows the curvature of this set of packages measured by Twyman-Green interferometer. The two orthogonal curvatures are plotted in the same figure. The curvature predicted by the BMP theory is plotted for comparison. An approximation made in the calculation of the curvature is that the underfill layer is treated as part of the substrate since the underfill layer has similar material properties as the substrate. It is clear that the predicted curvature by the BMP model is very close to the average curvature from experimental measurements in real packages.

The stresses on the top of the dies were calculated by BMP model and FEM for different samples. The stresses are shown in Figure 25.16. Although the BMP is based on plate approximation and the FEM uses 2D axisymmetric solid elements, the stress results are very close. The FEM calculation does show some edge effect at the die outer peripheral, this effect only affects the local area of about the dimension of order of the die thickness. The stress maintains constant in the rest part of the die. The FEM calculated stress shown in Figure 25.16 is the stress near the die center. The good agreement enables us to use BMP model to have a quick estimate of the stress on top of the die.

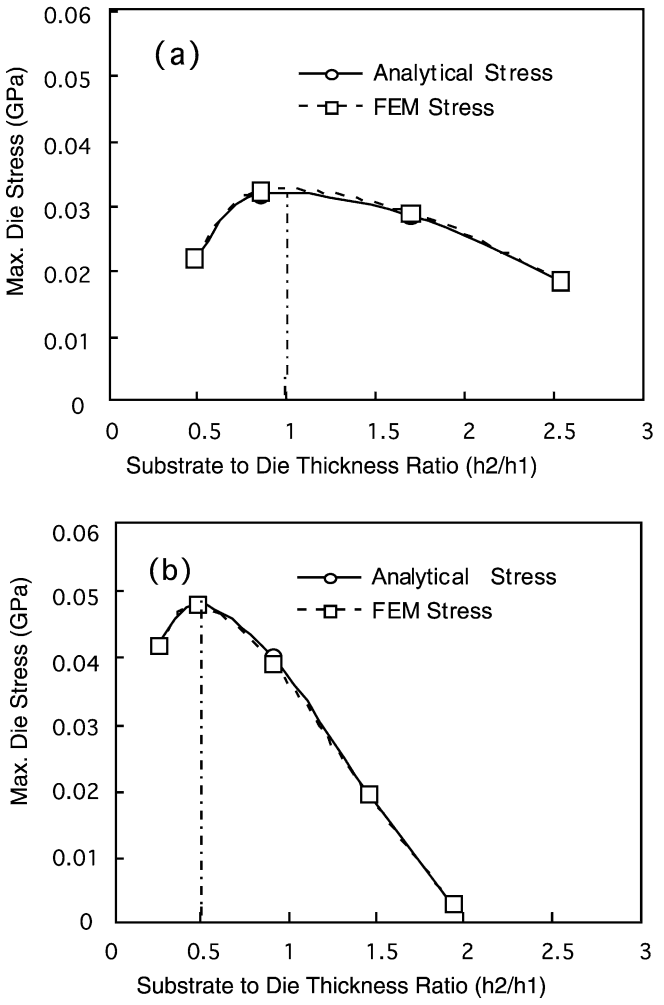


FIGURE 25.16. The stress on top of the die calculated from BMP model and FEM for (a) Si die on PCB substrate and (b) Si die on Cu substrate.

25.2.5. Flip-Chip Package Design

Since the BMP model gives closed-form solutions for bending curvature and die stress, it is very convenient to use the model to do parametric study in package design. The data can be tabulated or plotted as a handy reference. Figure 25.17 plots the characteristic curvature and characteristic die stress as a function of thickness ratio for different biaxial modulus ratios of the substrate to die. The reason to choose the characteristic curvature defined in Equation (25.17) is that it is dimensionless, thermal load independent and absolute thickness independent. This ensures that Figure 25.17 is universally applicable for arbitrary material combination, arbitrary geometry combination, and arbitrary thermal load. It is clearly shown that for every different material combination there is a maximum stress. As the ratio of the biaxial modulus of the substrate to die (m) increases, the maximum die stress (σ) increases and the position of the maximum die stress in terms of thickness

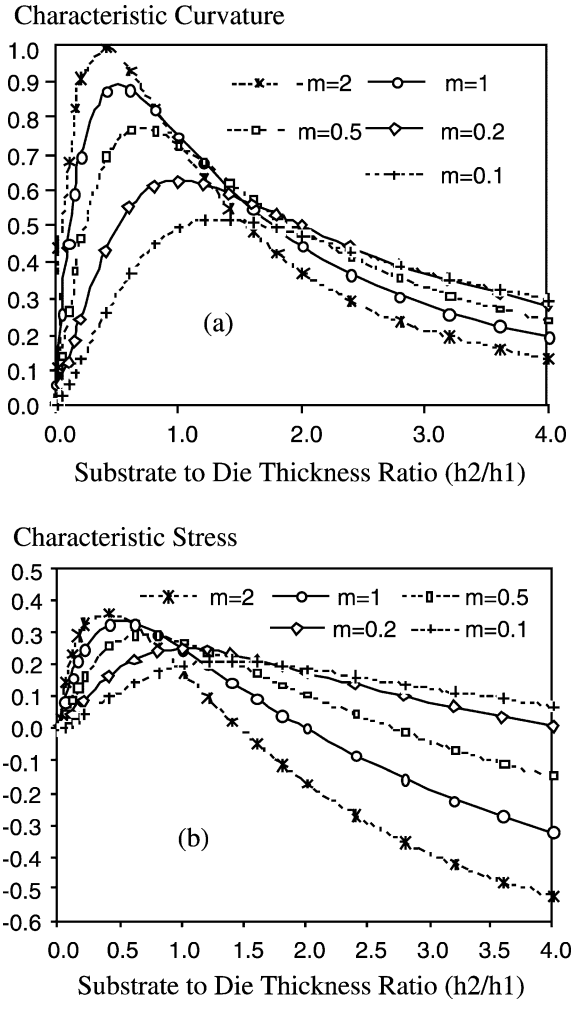


FIGURE 25.17. Dimensionless or characteristic curvature and stress in a bimaterial plate system as a function of thickness ratio and biaxial modulus ratio: (a) characteristic curvature; (b) characteristic stress.

ratio (h) tends to be smaller simultaneously. The position of maximum curvature is dependent on the material properties. Most of the FC-PBGA packages have the maximum curvature at $h \approx 1$, which is a coincident of the fact that most of packages are Si on PCB with $m \approx 0.2$. For Si on Cu ($m \approx 1$), the maximum curvature is located at $h \approx 0.5$. The characteristic curvature is approaching to zero as relative die thickness approaching zero or infinite. It is a reflection that the either the die or the substrate is too weak to let the system bend at these two extremes.

Figure 25.17(b) plots the stress on the top of the die predicted by the BMP theory. Although the die stress is related to the die bending, it is not simply related. The behaviors of the two quantities are very similar in certain range of thickness ratio h. This can be clearly seen in Figure 25.17(a) and Figure 25.17(b). Actually, if $h \to 0$, from Equation (25.21), $\overline{\sigma} \to 2\overline{\kappa}$. The behavior of stress is totally different from the curvature if h is large. From Equation (25.17), $\lim_{h\to\infty} \overline{\kappa} = 0$. On the other hand, Equation (25.19) leads to $\lim_{h\to\infty} \overline{\sigma} = -1$.

The physical meaning is that the system does not bend too much as the substrate is relatively thick or in other words the die is relatively thin. In this case, the curvature approaches to zero. The stress comes from two competing factors. One is the bending, and the other is the thermal mismatch strain. If the substrate is much thicker than the die, the bending of the bimaterial plate system is not significant and the die stress mainly comes from the mismatches in thermal deformations. Therefore, the die will be under a compressive stress, which is not critical to die cracking. If we are only interested in the lower thickness ratio range, a simple relation of the curvature and the die stress can be established. From Equation (25.21), one can have a relation $\overline{\sigma} = C\overline{\kappa}$ where $C = \overline{\kappa}/\overline{\sigma} = (1+h)/(2+3h-mh^3)$. Generally, C is not a constant. For Si on PCB with $h = 1$, $C(m = 0.2, h = 1) = 0.41$. If we use this $C = 0.41$ for thickness ratio from 0 to 1.5, the correlation between the curvature and stress is very good.

Although the BMP model neglects the edge effect, it does not introduce large errors in the estimation the curvature and the die stress. Three dimensional FEM calculation results show that the package size effect and aspect ratio effect only make 5% difference [16]. Furthermore, the BMP model provides us more insight in the packaging design when the die size is becoming very large. From Equations (25.16) and (25.18), it can be clearly seen that the curvature and die stress are independent of the package size. The curvature is only the function of modulus ratio (m), thickness ratio (h), thermal load (ε_m), and die thickness (h_1), and the die stress is only the function of modulus ratio (m), thickness ratio (h), thermal load (ε_m), and die biaxial modulus (M_1). This indicates that the increase of die size will not cause intrinsic limiting factor coming from die stress as long as material combination and thickness ratio is properly chosen. In real packaging design, one does experience lower yield when package size increases. The reason is that the number of defects per die increases for larger package due to the larger area of die (assuming defect density is a constant).

Another important observation is that the die stress is independent of absolute die thickness when the thickness ratio is fixed. Equation (25.18) does not contain the factor of absolute die thickness. In real flip-chip packaging design, it was found that thinning and polishing the die can significantly enhance the yield. This can be understood by looking at the Figure 25.17. Thinning the die and keeping the substrate thickness unchanged is equivalent to increasing the thickness ratio (h). This actually offsets the maximum stress location to get a good yield if the die is originally thicker than the substrate. The other advantage is that polishing the die can reduce the defect density, which means higher die strength, and as a consequence, the yield is improved significantly.

25.2.6. Die Stress in Flip Chip Assembly: Summary

An analytical model and governing equations are established for describing the intrinsic behavior of flip-chip packages. The model is validated by experiment and FEM calculation. The curvature and the bending stress are independent of the die size. The bending stress is independent of absolute die thickness if substrate to die thickness ratio (h) is kept the same. Both the curvature and the die stress have maximum values as the thickness changes. For FC-PBGA packages, which correspond to biaxial modulus ratio ($m = 0.2$), the die stress is maximum when the thickness ratio (h) equals to one. The die curvature and the bending stress are approximately proportional in certain range of thickness ratio.

25.3. THERMAL STRESS DUE TO TEMPERATURE CYCLING

Due to thermal expansion mismatch between the microelectronics package and the printed circuit board on which the package is mounted, thermal stress is introduced in the cooling step of the industry standard solder assembly process. Dynamic stress is further produced in the completed package-board assembly, especially in the solder joints, when the assembly is subjected to power cycling, thermal cycling, or thermal shock. The dynamic stress/strain has a great impact on the long-term reliability of the solder joint.

25.3.1. Finite Element Analysis

Non-linear finite element simulation methodologies have been adopted to investigate the time-dependent thermal stress/strain in the solder joints. As an example, the finite element modeling of a FC-PBGA assembly under accelerated temperature cycling conditions is given here. ANSYS 6.0 is used for all aspects of the study: pre-processing, solution, and post-processing.

Due to symmetry, only one-quarter of the module-board assembly is modeled. Figure 25.18 shows one quarter of the module-board assembly for the FC-PBGA. The solder material is modeled as a viscoplastic solid. The PBGA substrate along with the printed circuit board are modeled as composite materials with their copper power and ground planes, and their orthotropic, temperature dependent dielectric materials explicitly modeled. The physical and mechanical properties of the silicon chip, underfill material and board are summarized in Table 25.1.

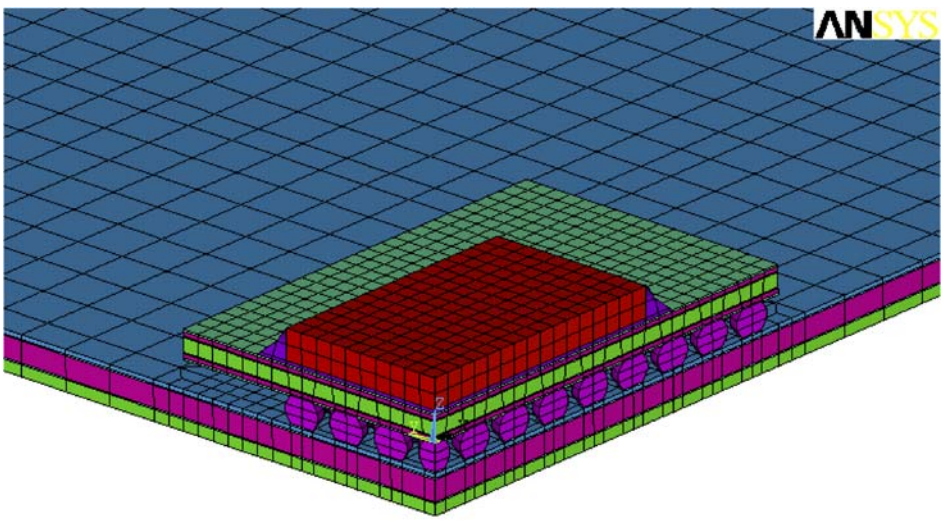


FIGURE 25.18. Finite element model of a FC-PBGA assembled on a board.

TABLE 25.1.
Material properties used in modeling of an FC-PBGA assembly.

Material	Modulus @ 23°C (GPa)	Poisson ratio @ 23°C	CTE (10^{-6}/°C) @ 23°C	T_g (°C)
Si Chip	186	0.28	3.2	NA
Underfill	3.4	0.33	24	145
PBGA substrate (Power Plane)	45.6	0.34	17.6	NA
PBGA substrate (Dielectric)	16.4 (x, y) 2.6 (z)	0.48 (x, y) 0.16 (z)	14.8 (x, y) 67 (z)	170
SnPb solder	Viscoplastic, see Ref. [21]	0.29	22	NA
Printed circuit board (Power Plane)	45.6	0.34	17.6	NA
Printed circuit board (Dielectric)	88.6 (x, y) 2.7 (z)	0.48 (x, y) 0.16 (z)	22.4 (x, y) 67 (z)	170

25.3.2. Constitutive Equation for Solder

Accurate constitutive modeling of the solder plays an important role in the simulation of solder joint reliability. ANSYS does have viscoplastic elements as a standard option, but they use Anand's constitutive model [17,18]. The use of these elements is convenient since the user does not have to modify the source code. Anand's model was developed for hot working metals, which unifying plasticity and creep via a set of flow and evolutionary equations:

Flow Equation

$$\frac{d\varepsilon_p}{dt} = A[\sinh(\xi\sigma/s)]^{1/m} \exp\left(-\frac{Q}{kT}\right). \tag{25.22}$$

Evolution Equations

$$\frac{ds}{dt} = \left[h_0(|B|)^a \frac{B}{|B|}\right]\frac{d\varepsilon_p}{dt}, \tag{25.23}$$

$$B = 1 - \frac{s}{s^*}, \tag{25.24}$$

$$s^* = \hat{s}\left[\frac{\dfrac{d\varepsilon_p}{dt}}{A}\exp\left(-\frac{Q}{kT}\right)\right]^n. \tag{25.25}$$

Darveaux et al. [19] were the first to modify the constants in Anand's constitutive relation to account for both time-dependent and time-independent phenomenon. Parameters for near-eutectic 62Sn/36Pb/2Ag are given in Table 25.2 (see Refs. [19,21]).

TABLE 25.2.
Anand's constants for 62Sn36Pb2Ag solder in ANSYS.

ANSYS	Parameter	Value	Definition
C1	S_o (psi)	1800	Initial value of deformation resistance
C2	Q/k (1/K)	9400	Activation energy/ Boltzmann's constant
C3	A (1/sec)	4.0×10^6	Pre-exponential factor
C4	ξ	1.5	Multiplier of stress
C5	m	0.303	Stain rate sensitivity of stress
C6	h_o (psi)	2.0×10^5	Hardening constant
C7	$s\hat{}$ (psi)	2.0×10^3	coefficient for deformation resistance saturation value
C8	n	0.07	Strain rate sensitivity of saturation (deformation resistance) value
C9	a	1.3	Strain rate sensitivity of hardening

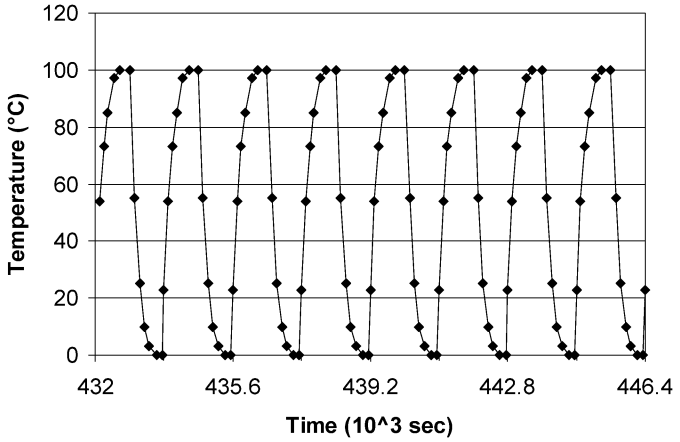


FIGURE 25.19. Cyclic temperature loading used in finite element modeling.

25.3.3. Time-Dependent Thermal Stresses of Solder Joint

The cyclic temperature loading imposed on the FC-PBGA/PCB assembly is closely matched to the temperature profile measured in accelerated temperature cycling test and is shown in Figure 25.19. It can be seen that for each cycle (30 minutes) the temperature is between 0 and +100°C, with 10 minutes ramp, 5 minutes hold at the two temperature extremes. In addition, pre-cycling, temperature-time history which corresponds to 5 days at 23°C is also included in the simulation.

Residual stresses in the solder joint after the FC-PBGA module was assembled to the board, cooled down to room temperature but before the temperature cycling test are shown in Figure 25.20. As expected the residual stresses relaxed very rapidly in the first hour after the assembly process. The stresses shown in Figure 25.20 are for the solder ball which is

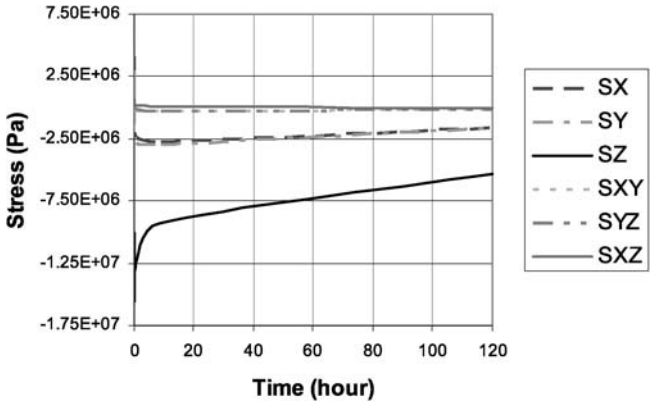


FIGURE 25.20. Residual stresses in the solder joint after assembly process.

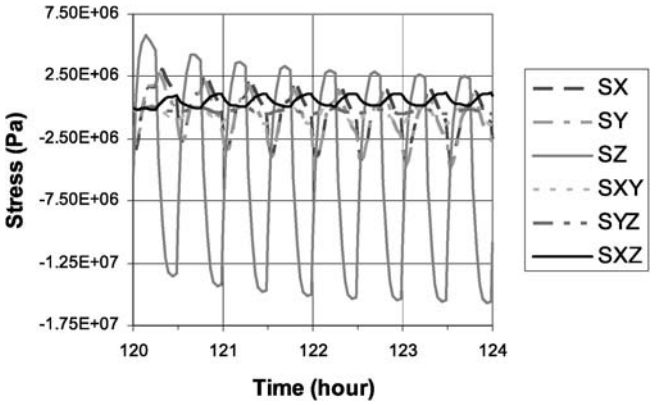


FIGURE 25.21. Time-dependent stresses in the solder joint due to cyclic temperatures.

under the corner of the chip as indicated in Figure 25.24. The dynamic stresses and strains in the same solder ball due to cyclic temperature variation are shown in Figure 25.21 and Figure 25.22, respectively. It can be seen from Figure 25.21 and Figure 25.22 the stresses and strains oscillate within certain ranges in accordance with the cyclic temperature load. Figure 25.23 shows the normal stress (σ_z) and the normal viscoplastic strain hysteresis loops for multiple cycles. For viscoplastic analysis, it is important to study the stress-strain responses for multiple cycles until the hysteresis loops become stabilized. Figure 25.23 indicates that the plastic strain is quite stabilized after the third cycle and the creep response converged after the fourth cycle.

25.3.4. Solder Joint Reliability Estimation

In addition to time-dependent thermal stress modeling, another goal of the simulation is to calculate the plastic work per unit volume (or viscoplastic strain energy density) accumulated per thermal cycle. Over the years, an energy based metric for predicting crack initiation and growth in solder joints was developed and refined [19–21]. The plastic work accumulated during the last cycle is used for crack growth and solder joint fatigue life cor-

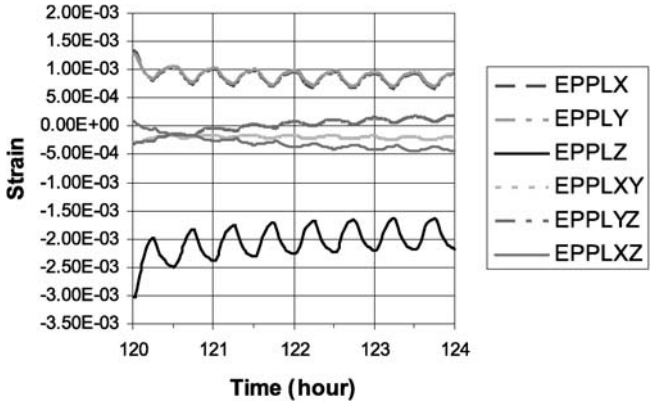


FIGURE 25.22. Time-dependent strains in the solder joint due to cyclic temperatures.

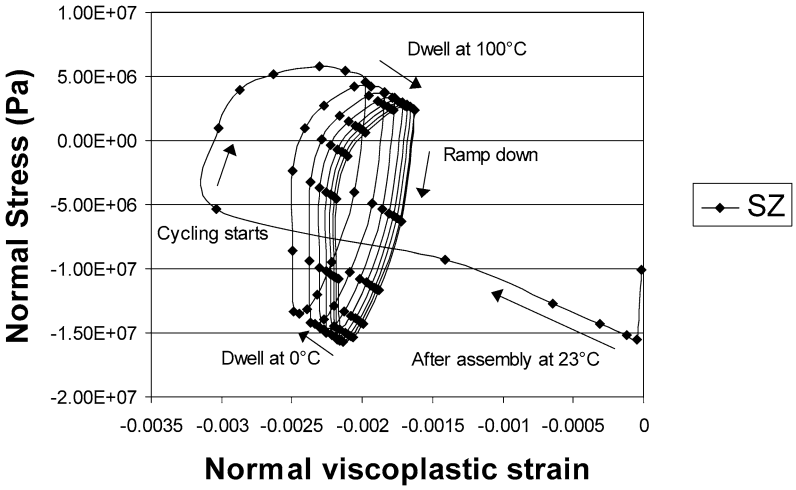


FIGURE 25.23. Hysteresis loops of stress and viscoplastic strain.

relations. The characteristic fatigue life (N_a) for the solder ball with a pad diameter of a can be written as

$$N_a = A(\Delta W_{ave})^B + C(\Delta W_{ave})^D, \tag{25.26}$$

where A, B, C, D are constants that depend on material and solder joint design and assembly process and ΔW_{ave} is the volume averaged viscoplastic strain energy density increment per cycle.

In practice, several complete thermal cycles are simulated in order to establish a stable stress–strain hysteresis loop. The A, B, C, D constants are determined by correlating the simulated results to the temperature cycling test results. Figure 25.24 shows the viscoplastic strain energy density increment calculated from the eighth to the seventh cycle. It is noticed that the solder ball with the highest accumulation in viscoplastic strain energy density is located just under the corner of the die edge. Experimental results show that the

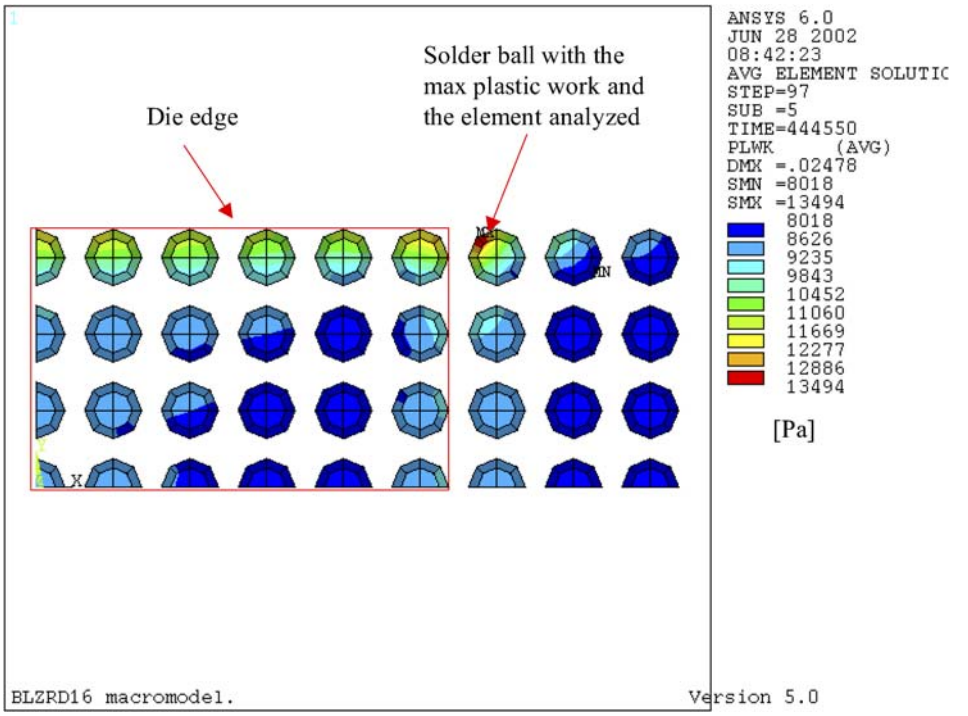


FIGURE 25.24. Calculated plastic work (viscoplastic strain energy density) increment.

balls under the corner of the die edge usually fail first in accelerated temperature cycling test.

25.3.5. Thermal Stress Due to Temperature Cycling: Summary

Dynamic thermal stress as a result of thermal cycling has a great impact on the long-term reliability and integrity of the electronic packages. A non-linear finite element simulation methodology is introduced and applied to simulate the time-dependent thermal stress/strain in the solder joints of a FC-PBGA assembly. The simulated results can be correlated with temperature cycling test results and can be used to predict solder joint reliability under various use and testing conditions.

25.4. RESIDUAL STRESS IN POLYMER-BASED LOW DIELECTRIC CONSTANT (LOW-*k*) MATERIALS

Bulge testing methods have been applied to measure thin film mechanical properties of metals [22–24], semiconductors (Si) [25], and dielectric materials [26–30]. However, it has rarely been applied to polymeric materials [27,29] perhaps the difficulty lies in sample preparation of very thin and pinhole free polymer membranes. The polyimide tested in Refs. [27] and [29] lie in the thickness range of several microns. However, the interlayer dielectric (ILD) materials used in multilevel Very Large Scale Integrated (VLSI) intercon-

nects are thinner films, typically one micron or less. The preparation of such thin polymeric membranes of low-k material without pin-holes is challenging.

In this section, we report a method to prepare thin polymeric membranes for bulge testing. By combining this test with the bending beam measurement of film thermal stresses, we have determined some of the mechanical properties of poly-arylethers (PAE) low-k thin films.

The PAE film, as reported in Ref. [31], was experimentally found to be susceptible to etching by oxidizing chemicals such as acids. It could only survive in H_2O_2 solution for a few minutes and was easily dry etched in O_2 plasma, but it was not attackable by bases. We adopted two approaches, namely, A and B, to be given below for preparing these PAE thin films for bulge tests.

In approach A, a 0.5-μm-thick, low-stress, and low-pressure-chemical-vapor-deposited (LPCVD) nitride film was patterned into square windows by dry etch in a $CF_4 : O_2 = 125 : 25$ mTorr gas mixture at 200 W, followed by Si etching in KOH 30 wt% solution at 90°C. A bilayer of Al (500 Å) top layer/Ti (2000 Å) was e-beam evaporated onto the nitride film. The reason for using the bilayer metal film is that the stress is tensile in the e-beam deposited Ti, but compressive in Al. The low-k material was then spun onto the Al/Ti film, then pre-baked for 1 min at 150°C, and cured for 60 min at 400°C. The thickness of the low-k film was varied by changing the spin rate of the coater and by multiple coatings, and measured by a Tencor Alpha-step Model 200. The nitride layer was then removed in the $CF_4 : O_2 = 125 : 25$ mTorr gas mixture at 100 W, using the Ti layer as the etch stop. Then the Ti film was etched using $H_2O_2 : NH_4OH = 1 : 2$ solution at room temperature and the thin Al was removed by KOH 30 wt% solution, leaving a window-like low-k film for bulge testing [32] see Figure 25.25(a) for a schematic cross-sectional view.

In approach B [32,33], we use a Si membrane as the sacrificial layer. The starting silicon substrate was a wafer of boron diffusion-doped to a depth of 3 μm with a concentration higher than 5×10^{19} B/cm^3. A wet thermal oxide of 5000 Å was grown on the Si substrate at 1050°C, followed by a deposition of 1500 Å LPCVD stoichiometric nitride. The residual stresses in the thermal oxide and nitride were about 330 MPa compressive and 1 GPa tensile, respectively, so the bending moment exerted on the Si substrate by the combined dielectric layers was minimized. A window was opened on the backside by dry etching the nitride as mentioned previously, and followed by wet etching the thermal oxide in buffered oxide etchant (BOE). Then the Si was etched in two steps; first, the etching by 30 wt% KOH at 75°C to a thickness of about 100 μm, and then the etching by ethylene diamine pyrocatechol (EDP) at 90°C until the etch stopped on the B-doped region. The result was a uniform Si membrane of 4.6 μm. The uniformity was better than 0.16 μm over a 1600 μm × 1600 μm area as measured by a Twyman-Green (TG) laser interferometer [34]. Finally the nitride was stripped in $CF_4 : O_2 = (125 : 25$ mTorr) gas mixture at 100 Watts, and the underlying oxide was removed by BOE etch. The process flow is schematically shown in Figure 25.25(b).

The low-k material was spun onto the Si membrane, then pre-baked and cured. To remove the Si membrane, it was first dry etched in the $CF_4 : O_2$ (125 : 25 mTorr) gas mixture at 100 Watts for 1 min in order to remove the native oxide, and then immediately loaded into a home-made pulsed XeF_2 etcher. The chamber pressure was 300 mTorr, and the etching time was 2 min for each cycle, and 2 to 3 cycles was performed. The completion of etching was determined visually through a plexi-glass cover on the etcher, aided by the observation that the low-k film itself is transparent. In comparing approach A and B, we found that the latter is less likely to break the polymer membrane. The key advantage of

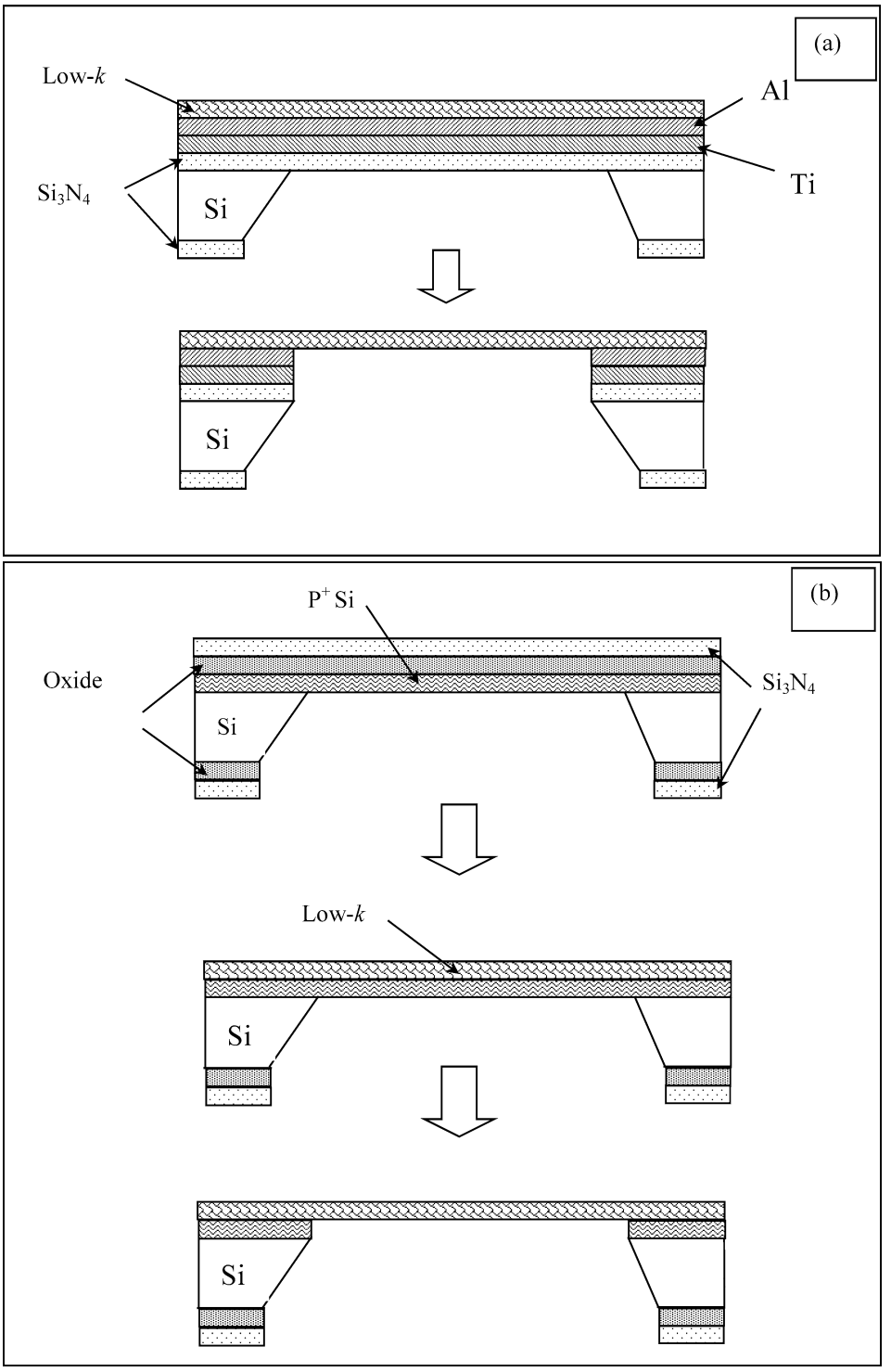


FIGURE 25.25. Cross-sectional view of the steps used to prepare the low-k membrane (a) Al/Ti/Si_3N_4 as the sacrificial layers, (b) P^+ (boron-doped) Si as the sacrificial layer.

the XeF_2 etcher is that it does not affect the thin polymer film and produces no pinholes in the film.

The PAE test film was prepared using approach B. It was coated at 3000 rpm for 30 sec, and the thickness was measured to be 4.6 ± 0.1 kÅ.

The raw data from a bulge test provides the total deflection of the membrane (δ) versus differential pressure (P). For a square membrane test sample, there are two approaches to extract the initial stress and biaxial modulus from the raw data. The first is a direct fit between P and δ, using the analytical formula, e.g., given by Pan et al. [26]:

$$P = \frac{C_1 \cdot t}{R^2} \cdot \sigma_0 \cdot \delta + \frac{C_2 \cdot f(\gamma) \cdot t}{R^4} \cdot \frac{E}{1-\gamma} \cdot \delta^3, \tag{25.27}$$

where $C_1 = 3.41$, $C_2 = 1.37$, $f(\gamma) = 1.446 - 0.427 \cdot \gamma$. R is half of the length of each side of the square, γ is Poisson's ratio, σ_0 is the residual stress, t is the film thickness and $E/1-\gamma$ is the biaxial modulus of the film. The second method of data extraction is to calculate the stress and strain at the center of the membrane [32]:

$$\sigma = \frac{P \cdot R^2}{C_3 \cdot t \cdot \delta}, \tag{25.28}$$

$$\varepsilon = C_4 \frac{\delta^2}{R^2}, \tag{25.29}$$

where $C_3 = 3.04$ and $C_4 = 0.451$ for square-shaped membranes. Poisson's ratio was assumed to be 0.42.

The maximum membrane deflection (δ) versus the differential pressure (P) curve for the dense polymeric film is shown in Figure 25.26 to be nearly linear. Since TG laser interferometer was used to measure the maximum membrane deflection, we were limited by the total number of countable fringes up to ~65. The initial stress in the film was calculated to be 35.2 ± 0.2 MPa after a curve fitting of Figure 25.26 using Equation (25.27). It is obvious that if we calculate the biaxial modulus using Equation (25.27), the result will be very unreliable because of the large initial stress. If we increase pressure for larger deformation, we are limited by the countable fringes, besides we might cause plastic deformation and creep in the polymeric film. Therefore, Equations (25.28) and (25.29) were used to calculate the stress (σ) and strain (ε). In the calculation, the small membrane deflection region was rejected, because in this region the measurement accuracy was relatively low. The biaxial modulus was estimated to be 6.40 ± 0.35 GPa on the basis of the curve fitting of the σ–ε curve, see the inset in the lower right corner of Figure 25.26.

In order to estimate the coefficient of thermal expansion of the low-k films, the thermal stress versus temperature curve was measured using a Flexus 2-300 machine (KLA-Tencor Corporation, San Jose, CA) under a nitrogen flow of 3 liter/min. The substrates used were 320-μm thick double-side-polished Si wafers. The low-k film was coated on the front side of the wafer and the wafer curvature was measured from the backside. The PAE films were coated at 3000 rpm for 30 seconds. Four samples of each kind were tested. We found that the initial stress as well as the slope of the stress-temperature curve varies significantly. The initial stress of the PAE film varied from 32 to 68 MPa. This is tentatively attributed to the difference in the coating solution and the cooling temperature profile during hard-bake. In general, the initial stress measured by bulge testing is lower than that by the Flexus testing; this may be due to relaxation of the film stress after part of

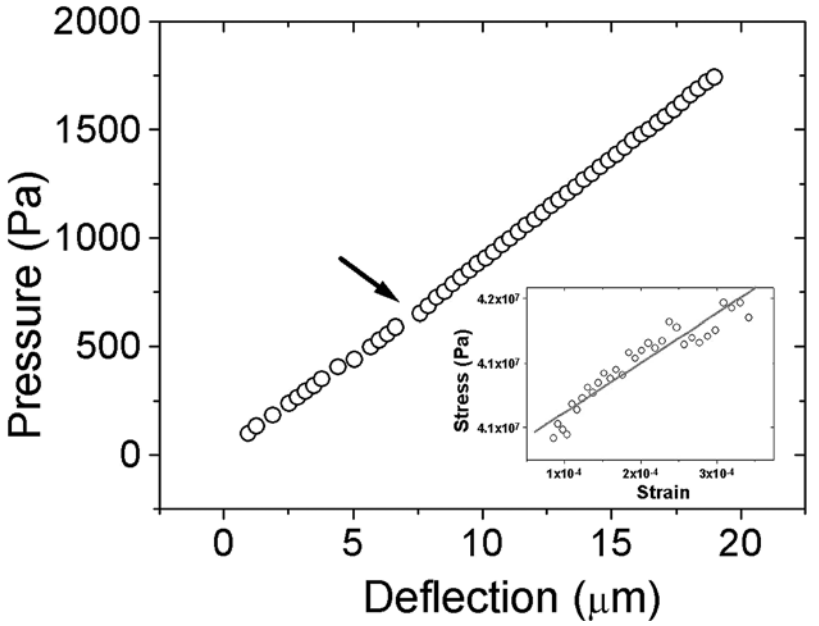


FIGURE 25.26. The total deflection of a 0.46-μm thick dense PAE membrane versus the applied differential pressure. Lower-right inset: the stress versus strain at the center of the membrane.

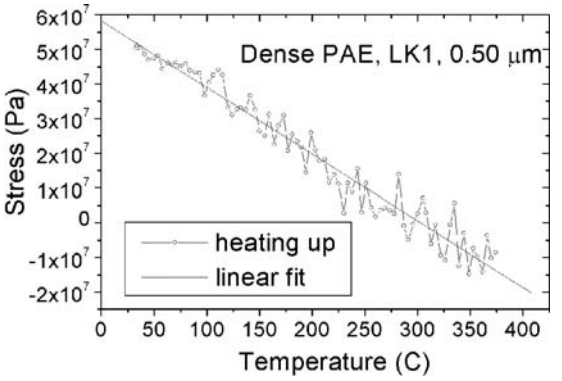


FIGURE 25.27. The stress versus temperature relationship of a blanket PAE film on a 4-inch (100) Si wafer.

the substrate Si was removed in the bulge testing. The slope of the stress-temperature curve is linked to the biaxial modulus and CTE of the film through the following equation:

$$\frac{d\sigma}{dT} = \left(\frac{E}{1-\gamma}\right)_f \cdot (\alpha_s - \alpha_f), \tag{25.30}$$

where $(E/1-\gamma)_f$, α_s, and α_f are the biaxial modulus of the film, the substrate CTE and the film CTE, respectively.

Figure 25.27 shows a typical stress versus temperature curve, where the temperature profile was ramping up from room temperature (24°C) to 375°C in 1.75 hr, held at 375°C

for 0.25 hr, and ramped down to room temperature in 2 hr. The slope of the PAE film ranges from 1.526×10^5 Pa/°C to 1.923×10^5 Pa/°C, and the corresponding CTE calculated range from 26.8–32.6 ppm/°C.

In summary, we have extended the bulge testing method to polymeric thin film of sub-micron thickness. The biaxial modulus and thermal expansion coefficient of the PAE film was obtained.

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