Chapter 4

EARLY PREDICTION OF CONDUCTED-MODE EMISSION OF COMPLEX IC'S

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Abstract A new design methodology is presented for predicting the conducted-mode emission generated by an integrated circuit. Using the Integrated Circuit Electromagnetic Model (ICEM) developed by the International Electro-technical Commission (IEC), the influence of the internal power supply distribution is modeled, and the sensitivity to design options or external factors such as supply voltage variations may be studied. Using ICEM models written in VHDL-AMS leads to efficient simulation, from the early steps of the design process, of self-perturbation and self-immunity of a complex integrated circuit. These ICEM models may be part of an IP-block definition, preserving confidentiality. Providing an early stage information on the EMC quality of the chip facilitates the way to a first-time working silicon. A full 8-bit micro-controller with core, memories and I/O blocks, from an existing industrial design, is used to validate the methodology.

Keywords: Electromagnetic compatibility, ICEM, VHDL-AMS, prediction, modeling, simulation.

1. Introduction

Early performance estimation and quality validation remains a key concern in the design of complex IC's. IP's definition and design reuse solve partly that problem for area, delay and even power, but characteristics like Electromagnetic compatibility (EMC) compliance is rarely addressed. Industrial designs are directly concerned with electromagnetic compatibility, particularly for portable equipments: an electronic system must be certified for given emission and susceptibility levels. Traditionally EMC compliance was only con-

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sidered at the board level. This includes of course radiating effects but also simple supply transients: the di/dt of supply currents will directly pollute the environment. And the higher complexity, lower dimensions and higher switching rates of modern chips will produce higher spike density on the supply rails. It becomes a real necessity to be able to estimate, from the first steps of the design process, the effect of architecture choices on EMC properties.

Till recently, the classical approach to this problem was to measure produced chips, generally in packages, to certify the design. The only correction action may be to choose another package, change some lumped elements or even re-design the chip, with a new silicon, but without any real help for the chip designer. Only recently [Steinecke et al., 2004] some comparison between models and measures, using gate level models was presented. But of course this leads to huge simulations, and requires to know the precise gate structure and routing details at the time of each simulation.

The focus of this research is to address the problem at the architecture level, as early as possible during the design process, to efficiently estimate current supply transients of a full chip, in a given package. At this level, each block is better handled as a macro-function, without precise detail of the internal structure, even if the structure is already frozen, as for example when reusing IP's. Therefore we need an EMC model for each basic block. The model chosen is directly inspired from the ICEM model [IEC EMC Task Force, 2001]. Classically, this model is derived from measures on a packaged chip in activity, and is used to analyze the effect of the package itself on the CEM performances. Defining ICEM models at the level of the macro-function basic blocks, and assembling them in a mixed-mode simulation environment, we got a full chip CEM model. As for the classical ICEM model, the basic block CEM models are constructed to model the activity dependent current supply transients of the particular block, the digital functionality itself being modeled by classical VHDL code. The full chip simulation is then run in a VHDL-AMS environment, to allow complex stimuli to be applied, corresponding to a given digital activity. Interconnections of blocks are modeled by lumped parasitic elements, according to place and route of the blocks. To validate this model approach, the results were compared to measures in the precise case of an industrial chip, an 8-bit micro-controller. The results gives good correspondence, at reasonable computer cost.

2. Modeling IC conducted emission

The ICEM proposal developed in 2001 [IEC EMC Task Force, 2001] was developed to model the effect of parasitic elements of board, package and chip itself, on the spike shape of supply currents, and so helps to analyze the electromagnetic compatibility of a chip in its environment, in the domain of con-

ducted emission. The parameters of the model are obtained by standard measures [IBIS 4.0] on a chip after foundry.

Figure 4.1 gives the principle of the measure, along with the equivalent model which is extracted. In this model, the activity of the chip itself is mod-

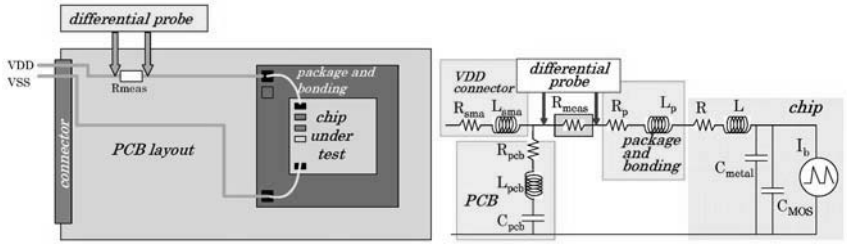

Figure 4.1. Principle of the ICEM measure and equivalent model

eled by a complex switched current source I_b, and the internal power distribution is modeled with lumped elements, R, L and C_{metal}. C_{MOS} globalizes the capacitance effect of the active elements. The power supply connector is modeled by R_{sma} and L_{sma}, and the PCB wiring by R_{pcb}, L_{pcb} and C_{pcb}. This approach uses a simple lumped model[1], limited here to the VDD rail effect. R_{meas} is a small value resistance added to measure the supply current with a differential probe. It should be noted that the I_b current is not directly measurable, but the values of the lumped elements can be derived by special analysis techniques [Levant et al., 2002]. This approach is an efficient way to analyze the effect of supply decoupling or a particular package on di/dt for example, and is actually used in the final step of a PC board design.

3. The proposed methodology

In a top-down approach based on design reuse, the design itself is viewed as an assembly process of well defined structures, characterized in terms of silicon area, signal delays and power consumption, but generally with no information on the internal details, for confidentiality reasons. Moreover, considering all the details in a simulation will lead to excessive computer cost. VHDL has solved part of the simulation bottleneck for digital systems, and gives good evaluation of signal delays. Some extensions allow the estimation of power, but no information is generally available in the digital domain for transients on the supply rails. One objective of this research is to facilitate the full chip simulation of supply transients, using high-level VHDL-AMS models for the basic blocks, and ICEM models for the floor plan and package parasitic elements.

The global model is build by assembling the basic block models: each block is modeled with an ICEM model representing its internal activity and parasitic elements, and interconnections of the blocs are modeled by lumped elements. Of course here the basic blocks are macro-functions which may be very complex: these are classically of the level of complexity of what is stored as memory or core IP's in an IP library.

To obtain the ICEM parameters of a block, a good practice may be to simulate this block as a SPICE model, in the particular environment of a given chip (or any realistic environment), the rest of the chip being modeled by pure digital VHDL, in order to stimulate the block with realistic patterns. The ICEM model is then derived by fitting the current source parameters to match the time transients of the supply currents. Passive elements are mainly metal line and parasitic MOS capacitances, which may be obtained from the SPICE net list, knowing the internal structure. This structure is then summarized in a lumped model, masking its details.

This job has to be done only once, and the result is stored in the IP library, within the IP model. If the block itself is structured, a structured model may be similarly derived. The practical example here after will give some strategy to derive particular models.

On the top of the full chip, a lumped model, derived from measures, is added for the package and the printed board. Every switched current source is parametrized by the digital stimuli of the block, and a VHDL-AMS model is used to model the current source. The interest to use a VHDL-AMS model for the transient current of a given digital part is to produce an activity model driven by the actual applied signals, generated by simple VHDL digital models, which are efficient in simulation. This leads to a light mixed-mode model for complex chips, just fitted to the exact desired characteristics.

4. A practical example

The example of a particular micro-controller, the 8-bit μC 80C51 'VIPER' from ATMEL, in a 0.35μ technology [Perdriau et al., 2002], is used to present the proposed methodology. Figure 4.2 shows the 4 main blocks of the internal structure of this μC: the CPU core, the EEPROM memory storing the program code, the SRAM memory for data, and the I/O drivers.

Figure 4.3 shows the VDD supply current measured in four different operational modes, from which spectral characteristics can be derived. These modes are chosen to see the effect of the different architectural blocks on the supply consumption and transients: in the RESET mode, only the CPU core is active; in the NOP mode, the opcode address decoder is added; in the instruction RRA (rotate right accumulator) the ALU is active; the MOV instruction uses the address generator and the SRAM.

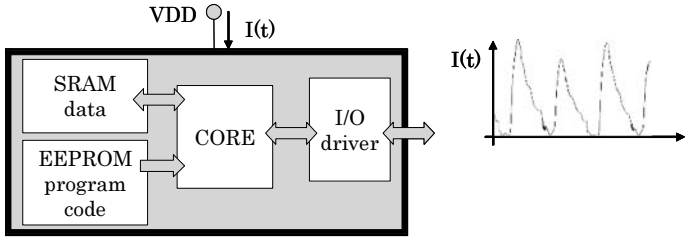

Figure 4.2. Example of IC structure under test for ICEM measures

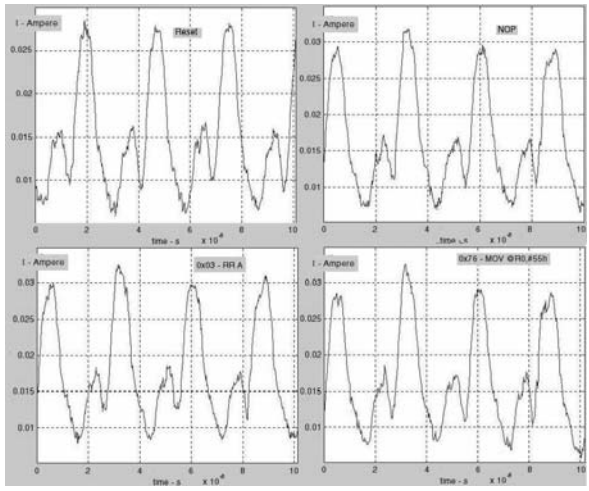

Figure 4.3. Measurement of the VDD supply current of an 8-bit μcontroller in 4 activity modes (8-bit μcontroller 80C51 'VIPER' from ATMEL, in a PLCC 44 pins package, techno 0.35μ)

From these experiments, it is clear that the ALU action and the memory accesses are negligible, and that no instruction dependence is visible : only very little spikes or offset changes can be observed. The main reason is probably that in the case of such a CISC processor, all these spikes come from the clock tree distribution, the ALU and the memories being much more slower. So the first idea to focus on the CORE activity, and the I/O drivers, in order to derive a model for this internal activity, which will be used to build the full chip model.

A general global model (Figure 4.4) is used to simulate the full chip for EMC characterization. Each basic block is here represented by a transient current source which models its dynamic internal activity. This can be obtained from full SPICE-level simulation, which is of course very time-consuming. The main blocks to be modeled as VHDL-AMS models are the CPU Core and

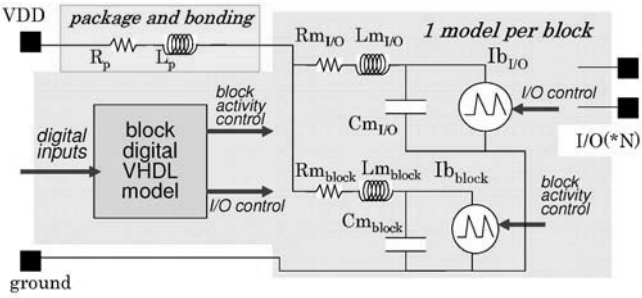

Figure 4.4. Block-based model of an IC for ICEM characterization

the I/O modules, which are dominant here. Passive components are derived from floor plan and P&R information, or could be simple prospective values. To derive the model, every block is successively simulated in its environment, the others being simulated by simple digital VHDL models. So the analyzed block is simulated in a realistic environment, corresponding to the complex behavior.

Example of a general block model:

```
ENTITY ICEM_IP_Model IS
 GENERIC (Tr :  real); -- rising time
 PORT (controls :  IN std_logic; -- * N inputs
       TERMINAL Vdd, Vss :  electrical);
END ENTITY ICEM_IP_Model;
ARCHITECTURE ICEM OF ICEM_IP_Model IS
 -- CONSTANT definitions for internal R, C and L
 TERMINAL Vddgen :  electrical;
 QUANTITY Vb ACROSS Isw,Ic THROUGH Vddgen TO Vss;
 QUANTITY Vrl ACROSS Irl THROUGH Vdd TO Vddgen;
BEGIN
 -- Isw computation :  to be adapted
  Ic == (Cmos + Cmetal) * Vb'dot;
  Vrl == Rint * Irl + Lint * Irl'dot;
END ARCHITECTURE ICEM;
```

Each block is modeled by an entity connected between the internal Vdd and Vss rails (PORTs defined as electrical TERMINALs), with digital control inputs (PORT signals IN). GENERICs are used to have the input rise time delay as a parameter to the model. Local wiring parameters (R_m, L_m) and metal and MOS capacitances (global value in C_m) are here constants internal

to the architecture (GENERICs could also be used). The internal switching current source has to be adapted to the particular blocks modeled. Here too, parameters may be internal constants or GENERICs.

5. The CPU core model

From a complete SPICE simulation of the core in RESET mode, an event-driven, piecewise linear (PWL) model, matching the simulated waves, is derived [Levant et al., 2002], and used to model the supply current activity of the core, in response to the digital inputs.

Example of the structure of the entity and architecture definitions:

```
ENTITY CoreGenerator IS
  GENERIC (Tr :  real); -- rise time for control signals
  PORT (XTAL1A : IN std_logic;
        TERMINAL Vdd, Vss :  electrical);
END ENTITY CoreGenerator;
ARCHITECTURE a OF CoreGenerator IS
  -- CONSTANT and local SIGNAL definitions
BEGIN
  PROCESS
  BEGIN
    LOOP -- for waiting driving signal XTAL1A
      -- compute PWL parameters and activates Tstart
    END LOOP;
  END PROCESS;
  IF domain = quiescent_domain USE
    -- starting values in DC
  ELSE
    -- compute currents
  END USE;
  BREAK ON Tstart;
END ARCHITECTURE a;
```

In this model, XTAL1A is a simple digital VHDL signal, but Vdd and Vss are VHDL-AMS terminals (electrical), to model the current activity. The generic map gives the particular rising delay of the signal, which is used in the model.

As expected, the internal current spikes produce external reduced spikes, due to the smoothing effect of packaging and supply decoupling. Compared to measures in RESET mode, this gives acceptable results (Figure 4.5): peak values and transition times, compared to the top left screen of Figure 4.3 are

in the same range, and very close. The main difference is the lack of the small additional pulse in each clock period, which comes from the clock driver. The simulation time goes down from 3 hours for the SPICE net list simulation to 4 seconds for the VHDL-AMS model.

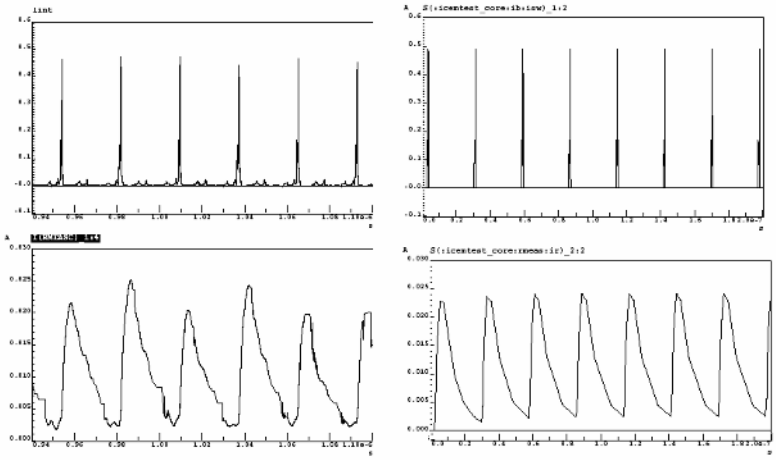

Figure 4.5. Core current in the RESET phase - Left: complete SPICE simulation: internal (top) and external (bottom) current - Right: VHDL-AMS model: internal (top) and external (bottom) current

6. The memory blocks

A VHDL-AMS model for the SRAM memory block was developed, and is detailed in [Perdriau et al., 2002, Perdriau, 2004]. The model is derived from the analysis of the internal architecture of the 1280-byte SRAM block from ATMEL. Separate models are given for the address decoder, which activity is address-dependent, and for the memory cells, which are not (only small differences are observed due to the output drivers). This allows to fit well with complete SPICE simulations, but in this application the spike current values are in the order of 1/20 of the CORE currents. Even if not really significant in this analysis, the VHDL-AMS model will be added to the standard VITAL model of the SRAM in the complete simulation. A simulation example of a memory access takes 2 seconds for this model, compared to 1 hour for the equivalent SPICE net list.

Example of the structure of the entity and architecture definitions:

```
ENTITY RAM1280Generator_h IS
  GENERIC (Tr :  real); -- rising time
  PORT (ADD : IN std_logic_vector(10 DOWNTO 0);
```

```
        DATA : IN std_logic_vector(7 DOWNTO 0);
        ME, WEN : IN std_logic;
        TERMINAL Vdd, Vss :  electrical);
END ENTITY RAM1280Generator_h;
ARCHITECTURE a OF RAM1280Generator_h IS
  QUANTITY Vb ACROSS Ib THROUGH Vss TO Vdd;
  CONSTANT DecPulseTiYZ:real_vector... -- Intensity vectors
  CONSTANT DecPulseIiYZ01:real_vector... -- 0->1 transition
  CONSTANT DecPulseIiYZ10:real_vector... -- 1->0 transition
  -- local CONSTANT and SIGNAL definitions
BEGIN
  ...
  PROCESS -- address decoder
    ...
  BEGIN
    LOOP
      WAIT UNTIL ADD'event;
      -- compute Hamming distances for X and YZ decoders
      PeriodStart := now;
      FOR n IN DecPulseTiYZ'low+1 TO DecPulseTiYZ'high LOOP
        Istartd <= ...; -- Current at start point
        deltaId <= ...; -- Current variation between points
        IF n = DecPulseTiYZ'low+1 THEN
          -- time for start and end points
        ELSE
          Tstartd <= ...; Tendd <= ...;
          WAIT FOR DecPulseTiYZ(n)-DecPulseTiYZ(n-1);
        END IF;
      END LOOP;
      deltaId <= 0.0; Istartd <= 0.0; previousADD <= ADD;
    END LOOP;
  END PROCESS;
  -- idem for X decoder and cells
  -- Current pulse generation memory cell activity
  IF domain = quiescent_domain USE
    Ib == Istartd;
  ELSE
    Ib == Istartd + deltaId*(now-Tstartd)/(Tendd-Tstartd)
    + Istartm + deltaIm*(now-Tstartm)/(Tendm-Tstartm);
```

```
END USE;
BREAK ON Tstartd, Tstartm;
...
```

SPICE analysis of the EEPROM leads to even lower values: access to one memory cell gives spike values of the current in the order of 1/35 of the value for the same operation on an SRAM cell. For this part, only a digital simulation, based on the VITAL model, will be used, and produces the digital signals driving the rest of the chip.

7. The I/O drivers

The I/O buffers are modeled by an IBIS [IBIS 4.0] model, adapted for ICEM simulations. The main changes are that, in the buffer, the MOS drain currents are functions of gate/source and gate/drain voltages, and must take into account the non ideal transient times of the control signals generated by the core. Moreover, concerning the supply currents, the limiting diodes must be considered, in the case of excessive I/O voltages. Values obtained may be in the order of the CORE current spikes, and are very dependent on the I/O data itself.

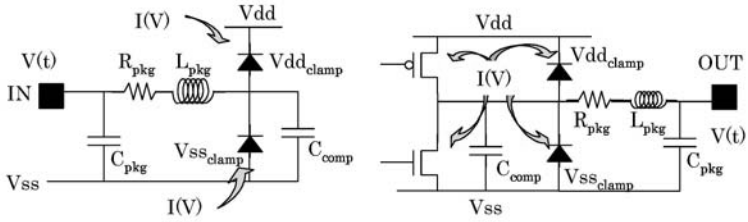

Figure 4.6. IBIS I/O Models: input (left) and output (right)

The VHDL-AMS model of the buffer [Perdriau, 2004], with generic parameters, implements table lookup and interpolation functions for MOS and diode characteristics. Parameters are the MOS tables, IBIS passive parameter values, and rise and fall times of the control signals. The MOS characteristics are split into 3 regions: one triode and two saturated regions.

Example of the structure of the entity and architecture definitions:

```
ENTITY totempole IS
  GENERIC (-- generic for MOS and diode parameters);
  PORT (io :  in std_logic;
        TERMINAL Tvdd, Tvss, pad :  electrical);
END ENTITY totempole;
ARCHITECTURE behavioral OF totempole IS
```

```
  QUANTITY vpmos ACROSS ipmos THROUGH Tvdd to pad; -- PMOS
  QUANTITY vnmos ACROSS inmos THROUGH pad to Tvss; -- NMOS
  SIGNAL in_realP, in_realN : real := 0.0;
  QUANTITY in_rampP, in_rampN : real := 0.0;
BEGIN
  -- NMOS and PMOS grid signals
  -- and quantity with rising time
  in_realP <= 1.0 WHEN io = '1' ELSE 0.0;
  in_realN <= 1.0 WHEN io = '0' ELSE 0.0;
  in_rampP == in_realP'ramp(tr,tr);
  in_rampN == in_realN'ramp(tr,tr);
  -- Currents from the parametric MOS tables
  ipmos == interpolate_mos(...);
  inmos == interpolate_mos(...);
END ARCHITECTURE behavioral;
```

Using these pad and buffer models, it is now possible to model the influence of the input and output of the clock driver. A real clock signal is generated, with a rise time of 3 ns, as in the experimental conditions. Putting these models directly on the supply rails results in the external current shown at Figure 4.7.

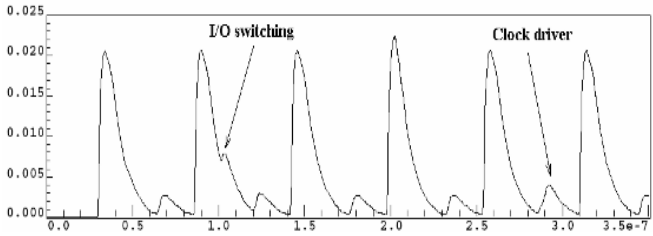

Figure 4.7. External current with I/O switching and clock driver

With this added I/O models, the intermediate pulse appears, correlated with the clock driver activity. On this simulation, the effect of I/O switching on the supply current is also visible. Their rise time and period are higher, and will produce low frequency perturbations. A complete simulation of the I/O ports in the system environment takes no more than 10 seconds.

8. Conclusion

The basic idea of the methodology presented here to address the ICEM evaluation, is to model the dynamic activity of each block with a transient current

source driven by the digital inputs, and, adding lumped elements for the passive components, focus on the supply rail currents of the whole chip, using high level mixed-mode simulation. These models have to be developed for each of the blocks which have a significant impact on the global behavior, in terms of supply currents.

Detailed SPICE simulations requires the knowledge of the internal structure, including precise implementations and place and route information, only accessible by parameter extraction on the mask data. This can only be done by the original designer of the block itself. From the experiments presented here, it seems possible to define a higher level model, in VHDL-AMS language, which could be put in the library of the IP block, for the final designer. Integrated in signal integrity tools, and supplied to PCB and system designers, these will allow fast board-level simulations of parasitic conducted emission.

The system designer may then even specify the expected EMC performance of the IC and verify the sensitivity of the design to previously described parameters, speeding up the design flow and supplying a "correct-by-design" circuit.

The example chosen here is a CISC μcontroller, which dynamic activity is mostly dominated by the clock tree activity, and not by the actual program running. For a RISC processor for example, it should be mandatory to implement, in the VHDL-AMS model of the core, an activity model for the input and output instruction bus activity for example. Defining activity classes based on instruction classes is a possible approach to this problem. The analysis of the effect of pipelining of instructions are future possible extensions of this work.

This work was done in close cooperation with ATMEL, to analyze the CEM properties of a chip after foundry in order to validate the methodology. It was then used by ATMEL during the re-design of a bad run of another project [Levant et al., 2004]: the good predictions of this modeling approach would have given a first-time correct chip, thus reducing foundry costs.

Standardization of this approach will be based on the new version of the IBIS model (version 4.1), which includes I/O VHDL-AMS descriptions, and on the work of the ICEM normalization group of UTE.

Notes

1. The model used here is limited to a lumped R-L-C approach, acceptable for this precise IC. For higher clock rates and future chips, a transmission line model will be necessary.

References

IBIS (I/O Buffer Information Specification) version 4.0. ANSI-EIA. `http://eda.org/pub/ibis/ver4.0/ver4_0.pdf`

IEC EMC Task Force. *IEC62014-3: Integrated circuit electromagnetic model*. Draft technical report, IEC, November 2001. `http://intrage.insatlse.fr/~etienne/icemcdv.PDF`

J. L. Levant, M. Ramdani, and R. Perdriau. *Power supply network modeling*. EMC Compo 2002, pp. 75-78, November 2002.

J. L. Levant, M. Ramdani, and R. Perdriau. *PLL Jitter Improvement using the ICEM Model*. EMC Compo 04, pp. 129-137.

R. Perdriau, D. Lambert, A.M. Trullemans, M. Ramdani, and J.L. Levant. *A VHDL-AMS simulation methodology for transient supply current extraction*. EMC Compo 2002, pp. 99-104, November 2002.

R. Perdriau. *Méthodologie de prédiction des niveaux d'émission conduite dans les circuits intégrés, à l'aide de VHDL-AMS*. Thèse de doctorat UCL, mars 2004.

T. Steinecke, H. Köhne, M. Schmidt. *Modeling, Simulation and Measurement of Conducted Emissions on Chip Level*. EMC Compo 04, pp. 21-26.