# 9

# Porous Silicon for Micromachining

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## 9.1. INTRODUCTION

The basic porous silicon processing has been used for micromachining for many years. In the early days, this was usually in the form of electropolishing. This was found to be an effective technique to etch through the full thickness of the wafer leaving a thin membrane. For example, etching through an n+ wafer and stopping on an n-type membrane has been applied [1]. This had the advantage of producing a well-defined membrane thickness with a relatively simple process. If the current density was too low and/or the HF concentration too high, porous silicon was formed on the surface. In these early days, this was simply seen as an etching experiment gone wrong. In the 1990s, the potential for micromachining was seen [2–4]. The material was found to be an effective technique for forming SOI and micromachining. The porous silicon could be oxidized at low temperature or was able to hold the structures in position to be removed at a later stage. Due to the extremely high surface area, the porous silicon can be removed very easily, for example in KOH at room temperature or even developer for photoresist. Furthermore, since the etching is an electrochemical process the porous formation can be performed selectively. The above processes all used microporous silicon. In recent years, macroporous silicon has also been shown to be highly effective for micromachining. Macroporous silicon was first used to make deep straight holes for capacitors [5,6]. The same process has since been shown to be effective for the fabrication of truly 3D mechanical structures [7].

This chapter gives an overview of the development of both micro and macroporous silicon techniques for micromachining. A comparison is given between the different techniques with a number of devices to illustrate the potential.

## 9.2. BASIC PROCESS

Porous silicon formation is generally an electrochemical process, although purely chemical etching recipes based on HF/HNO3 exist to create porous silicon. In addition to HF, a number of alternative etchants can be used. Some examples of available etchants are as follows:

- HF,
- HF + surfactants,
- AFEM,
- HF-dimethyl-formamide.

The basic process, which requires two electronic holes to remove one silicon atom from the surface of the silicon, is the following two-step process:

$$Si + 2h^+ + 2H^+ \rightarrow Si^{4+} + H_2 \tag{9.1}$$

$$Si^{4+} + 6HF \rightarrow SiF_6^{2-} + 6H^+. \tag{9.2}$$

Once an atom has been removed the chance of further removal from that point is greater than the surrounding area. Thus, the formation of porous silicon is able to continue. This also shows the reason why p-type silicon is more readily made porous. For n-type silicon, illumination is usually required to generate the holes. The basic process set-up is given in Figure 9.1.

The basic process is based on HF solutions. In the first solution, only HF is used. The addition of a surfactant is used to reduce surface tension and also ensure that the $H_2$ bubbles formed have the chance to leave the surface before they get too large [8]. The next etch solution is ammonium fluoride etch mixture (AFEM) [9]. This solution become of interest since it is able to form porous silicon but has a low etch rate for aluminium, which, since porous formation is often used as a post-processing step, is often present. The potential problem with AFEM is that there appears to be an additional chemical component in the etching that may result in unwanted etching. However, with some additional care this etchant can be used. The interest in the fourth etchant, DMF, began with the desire to make macroporous silicon in p-type material [10]. Macroporous silicon has a quite different structure from the microporous material. Micropores have a random structure whereas macroporous are regular [11]. Since that time it has also been shown that DMF can also be used to make porous silicon in n-type silicon [12].

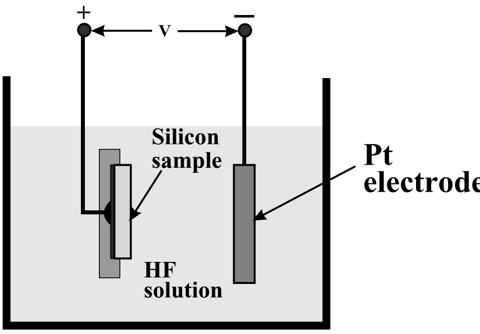



FIGURE 9.1. Basic process set-up for porous formation.

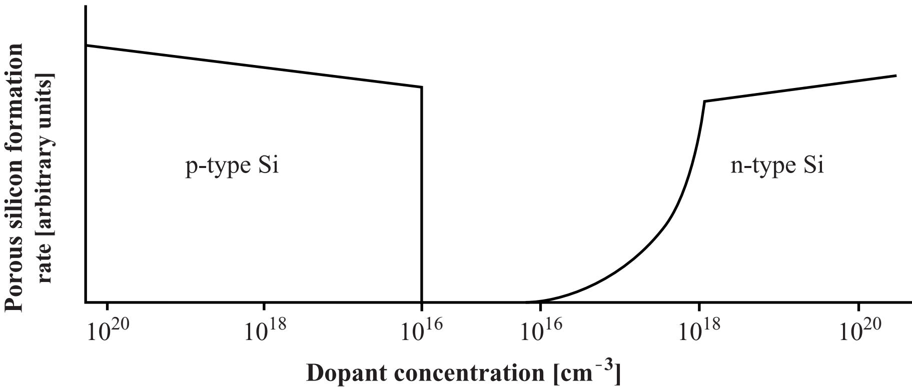



FIGURE 9.2. Porous silicon formation rate for n- and p-type silicon.

This etchant has a low etch rate for oxide, but a reasonable porous formation rate. This is discussed in more detail later.

Figure 9.2 shows that p-type silicon is most readily made porous due to the fact that electronic holes are required in the process [2]. As is discussed later, n-type porous formation requires illumination to generate electronic holes. Therefore, in the non-illuminated condition regions in the wafer can be selectively made porous. This is usually in the form of making p-type selectively porous. These are all microporous structures.

### *9.2.1. Micromachining Using Microporous Silicon*

The basic structure of the microporous silicon is shown in Figure 9.3 [11]. This shows a sponge-type structure. This type of structure was first observed by Canham in 1990 to emit visible light [13]. This first observed emission was in the form of photoluminescence, but subsequently both photo- and electroluminescence have been observed [14–17]. Other applications for microporous silicon include humidity sensors [18], gas sensors [19] and thermal isolation [20], where the porous silicon can easily be oxidized without mechanical stress through expansion. Its potential as a sacrificial layer was presented in the early 1990s [2–4]. The advantages of this material are that it can

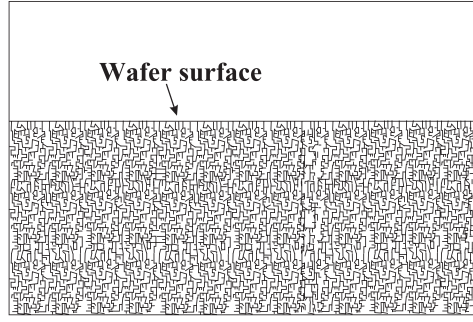



FIGURE 9.3. Structure of p-type porous silicon.

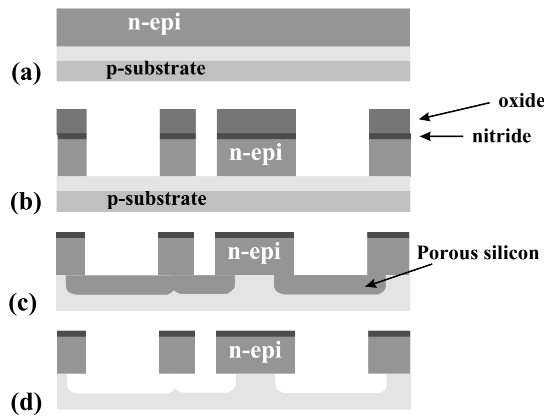



FIGURE 9.4. Basic process sequence for sacrificial porous silicon.

hold the mechanical structures in position until the end of the processing and then can be removed very easily due to the large surface area. For example, KOH at room temperature or resist developer can be used. For a review on porous silicon as a sacrificial layer, see [21].

As described above, the preference for p-type formation and the fact that it is an electrochemical process is extremely useful for micromachining. The basic process sequence is shown in Figure 9.4 [22]. Free-standing epi structures can be fabricated by making the substrate porous and then removing the porous layer at a later stage. The advantage is that the n-type epi is not attacked by porous formation and therefore does not need sidewall protection. The basic process is thus as follows: the starting point is the n-type epi on the p-type substrate (Figure 9.4a). Using an oxide, or other mask, the epi is defined to reveal the substrate (Figure 9.4b). Then using a back contact, in the configuration shown in Figure 9.1, the exposed regions of the substrate are made porous (Figure 9.4c). Finally, the porous silicon is removed to create free-standing structures (Figure 9.4d).

An example of a fabricated structure is given in Figure 9.5. The picture on the right shows the nitride mask on the top of the epi and the air gap under the epi.

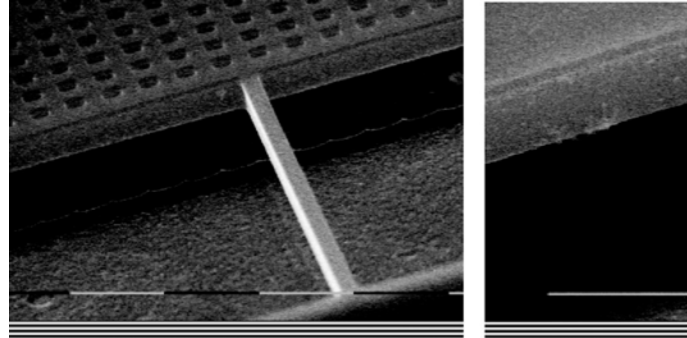
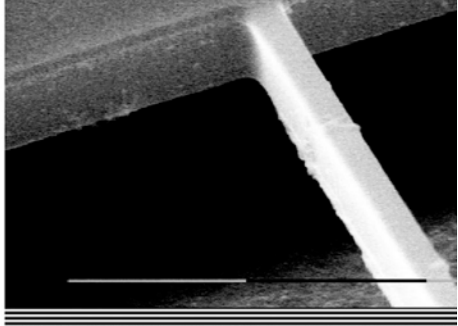



FIGURE 9.5. Free-standing structures fabricated using sacrificial porous formation.

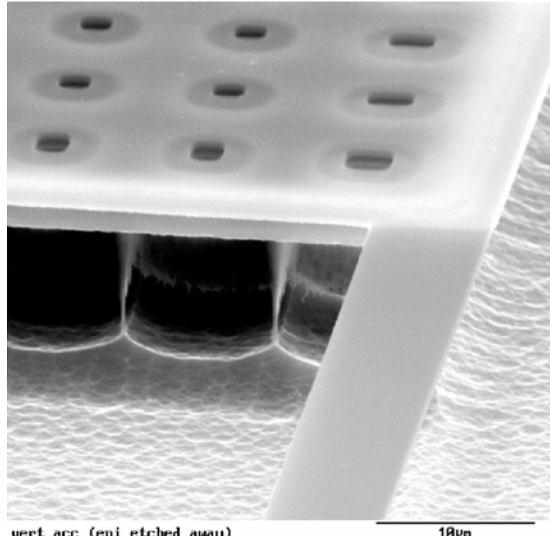



FIGURE 9.6. Partially released structure showing the wine-glass effect.

Figure 9.5 (left) shows the characteristic ridges between the etch holes. This is due to reduced current as the un-etched region narrows, and is often referred to as the wine-glass effect. This effect can be seen more clearly in Figure 9.6.

If aluminium is already on the frontside of the wafer this should be protected or an etchant should be used which does not attack it. As mentioned above, AFEM is a suitable option and such an example is given in Figure 9.7 [9]. However, this does present

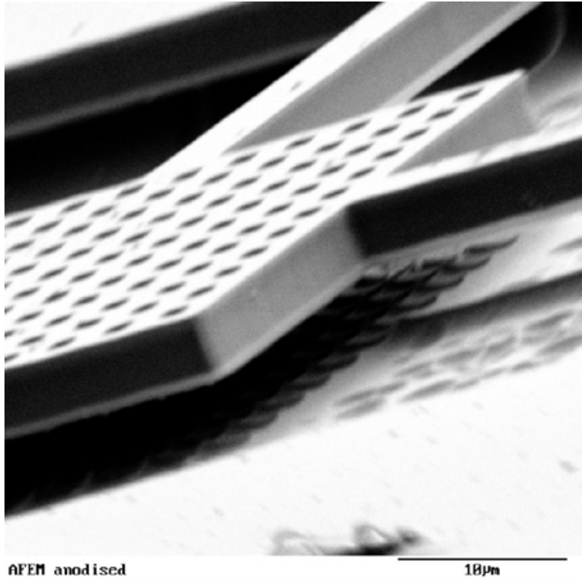



FIGURE 9.7. Micromachined structure fabricated using AFEM.

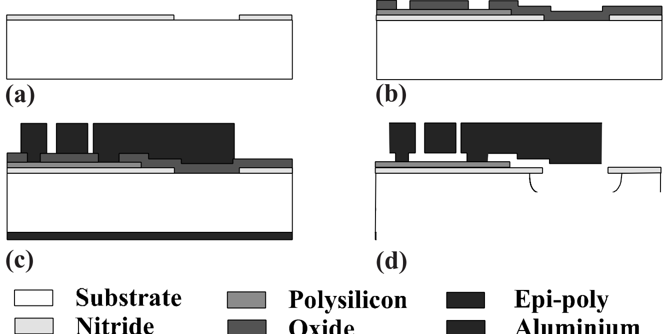



FIGURE 9.8. Basic process of epi poly combined with porous formation.

some other problems since this introduces a chemical element to the etching and it is no longer purely electrochemical. In order to protect the n-type epi, which would have been etched chemically by the etchant, a silicon nitride layer is needed after the definition of the structures. The lighter colour at the base of the structure is where the epi has been etched leaving only the thin nitride layer.

Porous formation can also be used to increase the air gap under surface micromachined or epitaxial structures. When oxide is used as a sacrificial layer a single etch step can be used. First, the oxide is removed using chemical etching and then porous formation is begun by applying a voltage.

This technique has also been combined with epi-poly processing [23]. In a similar process epi-poly structures, 4–8 μm thick, were produced with large air gap underneath (Figures 9.8 and 9.9).

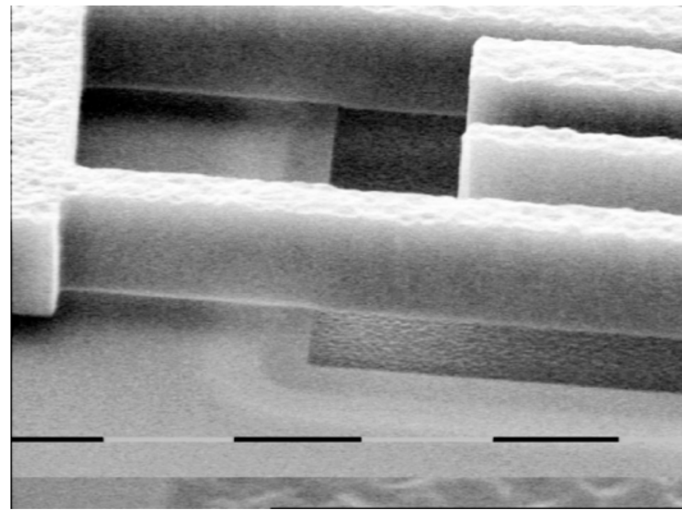


FIGURE 9.9. SEM photograph of structure fabricated using the double sacrificial etch.

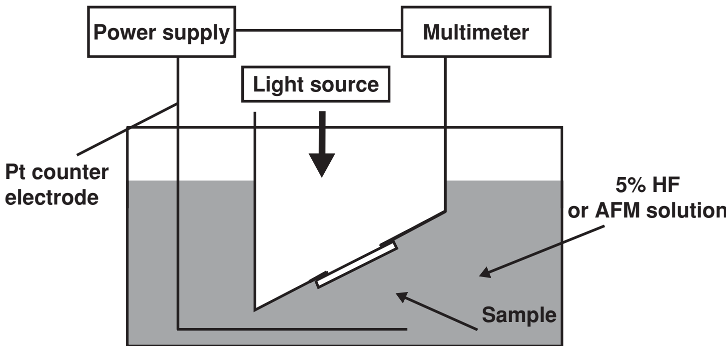



FIGURE 9.10. Etch set-up for the macroporous formation in n-type silicon.

### *9.2.2. Micromachining with Macroporous Silicon*

The macroporous process was first proposed by Lehmann for making deep straight holes with high aspect ratios [5]. The basic process is as follows. As shown above, porous formation requires electronic holes, which are in short supply in n-type silicon. However, illuminating the backside of the sample will generate electron–hole pairs (Figure 9.10). Alternatively, a liquid contact can be used. The holes move to the front of the wafer and start the etching process. This is illustrated in Figure 9.11.

This process was developed for making large capacitors [6]. The basic process is given in Figure 9.12. The starting material is an n-type wafer (Figure 9.12a). On this wafer, a SiN making layer is deposited and patterned to define the macropores (Figure 12b). A starting point for the pores is made using KOH (Figure 9.12c) and then electrochemically etched in HF to form straight pores (Figure 9.12d). Using this technique high aspect ratios can also be achieved, as shown in Figure 9.13.

A further interesting feature of this process can be seen in Figure 9.14. This shows that the current density does not control the vertical etch rate, but the width of the pores.

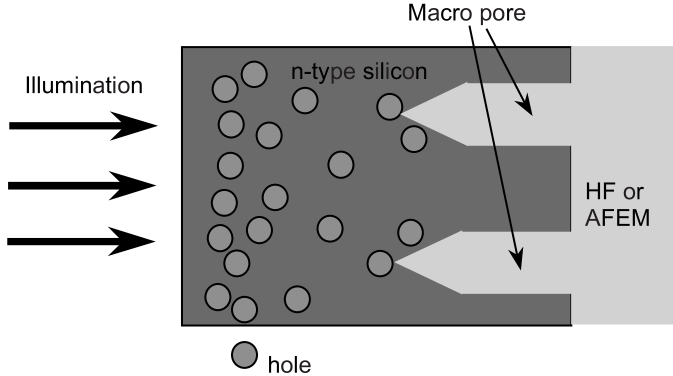



FIGURE 9.11. Etch process in n-type silicon.

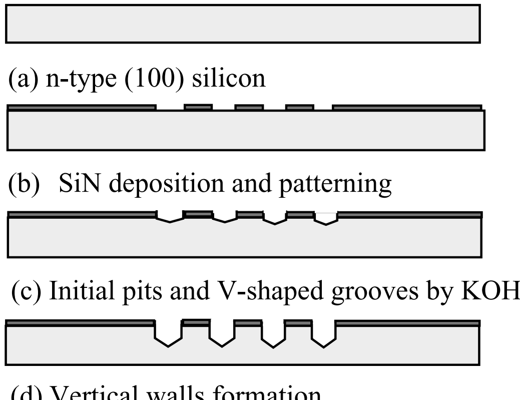



FIGURE 9.12. Basic process sequence for macroporous formation.

The process can therefore be modified to make free-standing structures. This is shown in Figure 9.15. The first three steps are the same as the standard process. Then, when the required depth is reached, the light intensity is increased to increase the pore width and release the structures (Figure 9.15d).

Therefore three-dimensional structures can be manufactured, since the change in width only occurs at the tip of the pore. An example of a fabricated structure is given in Figure 9.16.

The limitation of this process is the use of KOH to form the starting point of the pore. This means that the holes or slots have to be orientated in the ⟨110⟩ direction as (100) wafers are used. The initial assumption was that the point formed by the KOH was necessary to start the pore. However, it has been shown that plasma etching or isotropic etching can be used [24]. This removes the limitation of KOH and thus any shape can be fabricated. Examples of the structures can be seen in Figure 9.17.

The above discussion has been limited to n-type silicon because of the abundance of holes in p-type silicon.

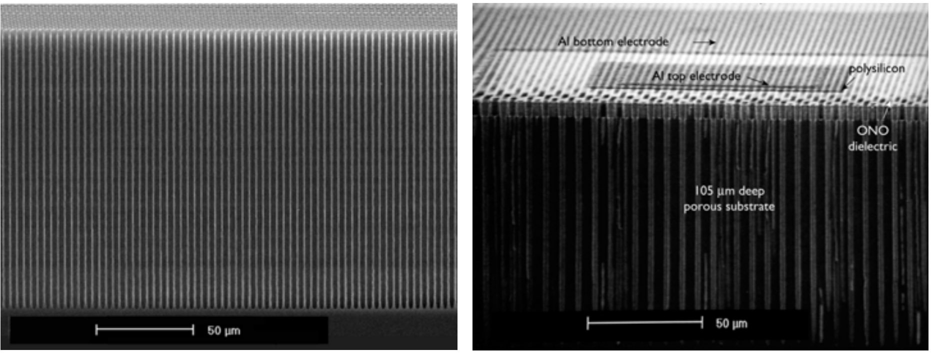



FIGURE 9.13. Deep straight trenches fabricated using macroporous techniques [6]. Reproduced with kind permission from Fred Roozeboom, Philips, The Netherlands.

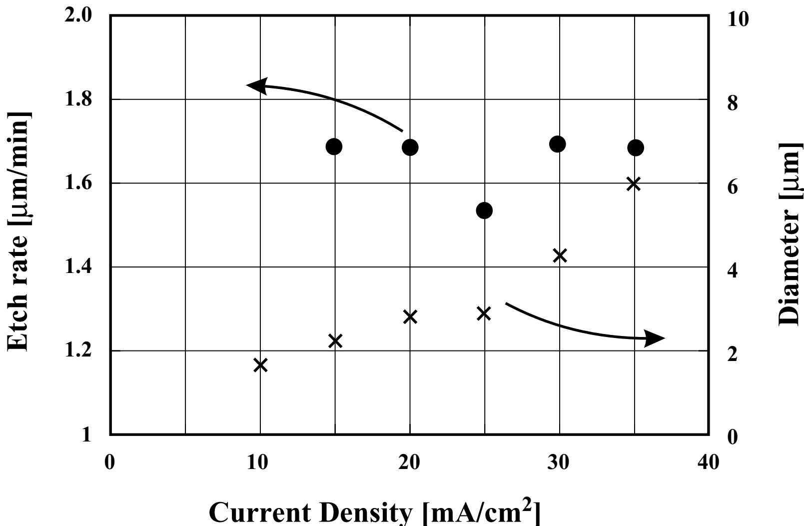



FIGURE 9.14. Etch rate and pore diameter as a function of current density.

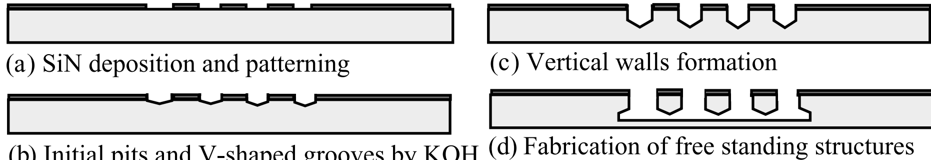



FIGURE 9.15. Adjusted macroporous silicon process for 3D structures.

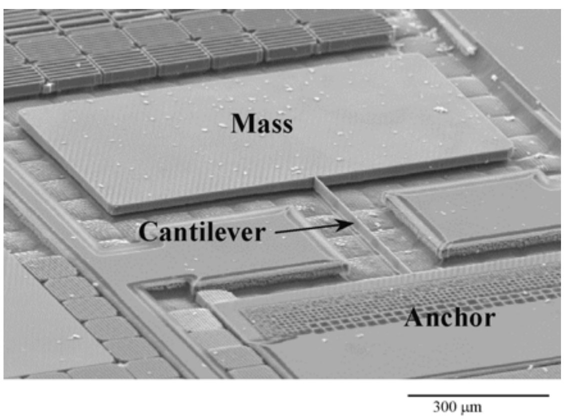



FIGURE 9.16. Free-standing structure fabricated using macroporous silicon micromachining [7].

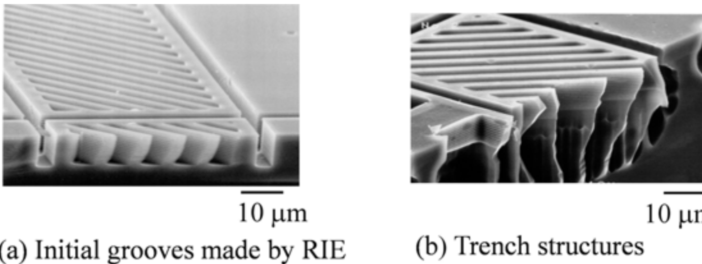



FIGURE 9.17. Structures fabricated using RIE starting point.

Macroporous silicon in p-type silicon is more difficult than n-type. Initially, using HF, only micropores were formed on p-type silicon substrate und thus trenches could not be achieved. Recently, in order to form macropores in p-type silicon, a new etchant, DMF, has been proposed [10]. The basic constituents of this etchant are: 4% HF (50%), 8% tetrabutylammonium perchlorate (TBAP), 4% $H_2O$ and the rest was dimethyl-formamide [25,26]. Being p-type silicon, with an abundance of holes, no light is required to achieve etching. However, it has also been shown that accurate control of the pore width cannot be achieved through current density, although micromachining can be performed using a switch between porous formation and electropolishing. SEM micrographs of etched surface as a function of current density for 20 minutes etch time are given in Figures 9.18a–c. In the case of lower current density, the whole area has been etched down uniformly and thus the initial grooves can be seen after electrochemical etching (Figure 9.18a). On the other hand, smooth etched surface was obtained due to electropolishing as shown in Figure 9.18c. Trench structures can be seen with the current density of 20 $mA/cm^2$ in Figure 9.18b although the etched surface was slightly rough. A close-up view of the trench structures is given in Figure 9.19. In order to fabricate free-standing beams, the current density increased after making the trench structures. For example, a current density of 20 $mA/cm^2$ can be used to obtain trenches followed by a current density of 30 $mA/cm^2$ to connect the trenches [10]. Free-standing beams can be achieved with this etching technique as shown in Figure 9.19. Clear gap between the beam and the substrate can be seen.

The DMF etchant is more difficult to control but in some cases it may be an advantage that the etch rate of oxide is low. The etch rate of oxide in HF and DMF is shown in Table 9.1. Thermally grown oxide can be seen to be a suitable mask with this etchant.

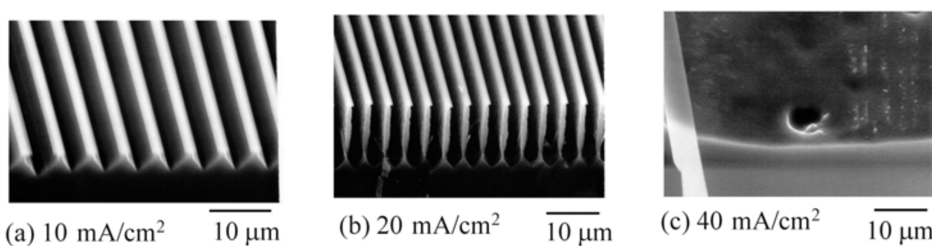



FIGURE 9.18. Etch results for three currents.

TABLE 9.1. Comparision of $H_2O$-based etchant with DMF-based etchant with etch rates of various masking materials. Both etchant contains 5 wt % HF. All etch rates are in Å/min.

| | $H_2O$-based HF (5 wt.%) etchant | DMF-based HF (5 wt.%) etchant |
|---|---|---|
| Thermally grown $SiO_2$ | 260 | 8 |
| PECVD-TEOS | 220 | 7 |
| PECVD-SiN | 95 | 6 |
| Sputtered SiN | 39 | 1.4 |
| LPCVD-SiN | 12 | 1.4 |

Further studies have been performed to use DMF for an n-type material. As in the case of HF, light is used to control the current. However, unlike HF, this cannot be used to control the pore diameter, as shown in Figure 9.20.

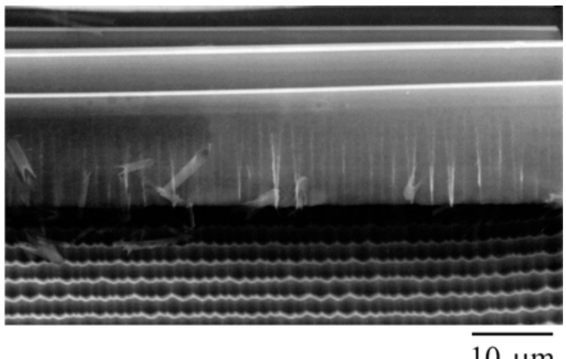



FIGURE 9.19. Close-up view of micromachined beams showing the air gap.

One of the problems with this etchant is its low conductivity. Therefore, the current, which is searching for the lowest resistive path is more likely to travel through the silicon between pores causing side branching. Tetrabutylammonium perchlorate (TBAP) powder was added to this etchant to control conductivity of etchant. As shown in Figure 9.21, increasing levels of TBAP leads to increased conductivity and smoother walls.

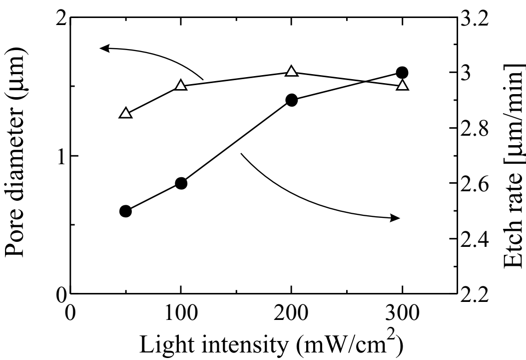
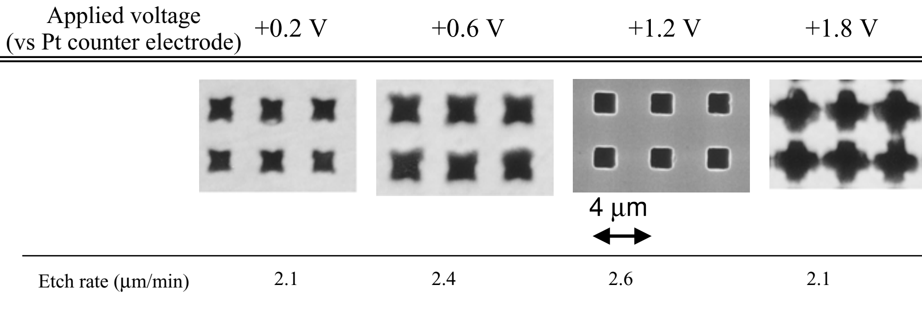



FIGURE 9.20. Effects of light intensity on pore diameter and etch rate. Applied voltage was set at +1.2 V.

| | Without TBAP | 10g TBAP | 20g TBAP | 30g TBAP |
|---|---|---|---|---|
| Cross-section view of etched pore (Magnification is 3500) | | | | |
| Conductivity of etchant | 4 mS/cm | 22 mS/cm | 29 mS/cm | 33 mS/cm |
| Etch rate of pore | 0.4 μm/min | 1.8 μm/min | 2.2 μm/min | 2.6 μm/min |

FIGURE 9.21. Effect of TBAP on the conductivity of etchant and the quality of pores.

| Applied voltage (vs Pt counter electrode) | +0.2 V | +0.6 V | +1.2 V | +1.8 V |
|---|---|---|---|---|




| Etch rate (μm/min) | 2.1 | 2.4 | 2.6 | 2.1 |
|---|---|---|---|---|

FIGURE 9.22. Plain view of pore morphology and etch rate influenced by the applied voltage, for etching n-type material. The light intensity was 100 mW/cm$^2$. The etchant composition was 270 g DMF, 15 g HF, 15 g $H_2O$, and 30 g TBAP. The etching was performed for 30 minutes.

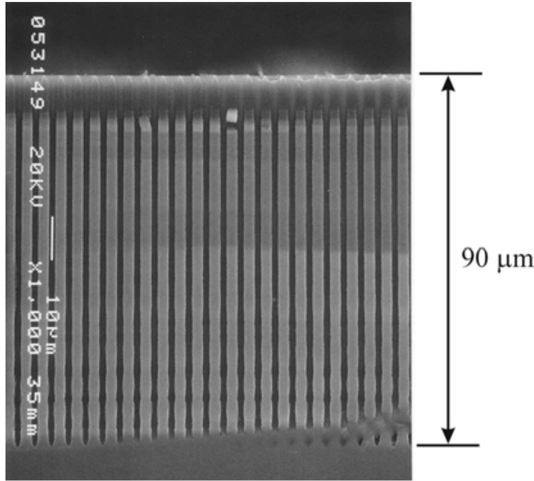



FIGURE 9.23. Cross-sectional view of pores, etched, using: light intensity 300 mW/cm$^2$, applied voltage 1.2 V; etchant: DMF 270 g, HF 15 g, $H_2O$ 15 g and TBAP 30 g.

There also appears to be some crystal dependence which can change with applied voltage. Etched samples were mechanically polished for a depth of 10 μm to observe the plain view of etched sample. At applied voltage of +0.2 V, pore shape is like star shape that has (110) preferred crystal orientation. At higher voltage of +1.8 V, pore shape becomes the cross shape that has (100) preferred crystal orientation. The pore wall exhibits a preferred crystal orientation, which is strongly affected by applied voltage. This is illustrated in Figure 9.22.

Electropolishing, in which etched surface becomes smooth, is not observed in DMF-based HF etchant, which is different from $H_2O$-based HF etchant. By optimizing the etching parameters, high aspect ratio pores can be achieved. This is illustrated in Figure 9.23.

## 9.3. APPLICATIONS

### *9.3.1. Sealed Cavity Devices*

One important difference in the sacrificial porous silicon technique compared to wet chemical etching is that the pores grow from the tips of the pores and therefore changes in the etch parameters will only affect the new porous regions and not those already formed. This feature has been used to form cavities by Anderson *et al*. [27]. In this case, the mechanical layer used was silicon nitride and the sacrificial layer was polysilicon. The resulting structure is shown in Figure 9.24. To fabricate this structure three steps were used. The first step, using 5% HF and 5 V dynamic hydrogen electrode (DHE), removed the first part of the cavity. This was followed by a high HF concentration step (49% HF) at 0 V DHE, which formed the porous plug. Finally, 10% HF at 5 V DHE was used to form the inner cavity.

### *9.3.2. Free-Standing Porous Structures*

In most micromachining processes, the porous silicon is used as a sacrificial layer. However, it can also be used as a mechanical structure. In Figure 9.23, an example regarding this is given [28]. In the first part of the process, first a porous layer is made in the substrate and once the desired depth is reached the current is increased to switch to electropolishing (Figure 9.25a). This structure is held in place due to the porous formation under the mask. Removal of the mask then releases the porous structure. This

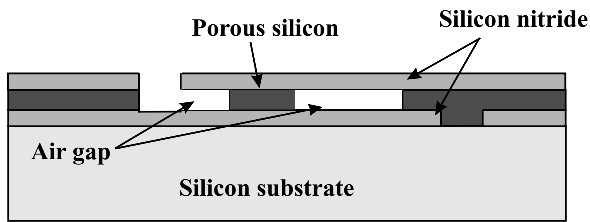



FIGURE 9.24. Cross-section of the sealed cavity fabricated using porous the formation of polysilicon [27].

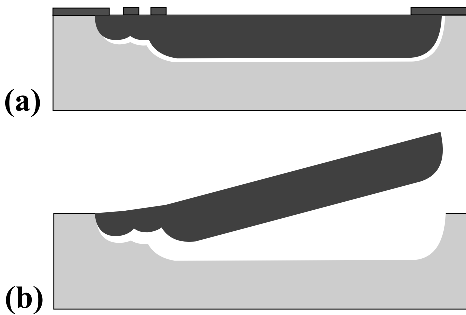



FIGURE 9.25. Process sequence: (a) after double porous formation process and (b) after full release [28].

release is performed using dry etching in an oxygen plasma. This has the advantage of avoiding stiction. It also causes a partial oxidation of the pores and through this produces a compressive stress. This is the reason for the lifting up of the mechanical structures (Figure 9.25b).

### *9.3.3. Isolated Structures*

Polysilicon bridges constructed using porous silicon as a sacrificial layer have been fabricated for various sensor applications. Porous silicon formation and removal release the bridges, forming flow channels beneath them (Figure 9.26). Bridges constructed of thin films have small cross sections that allow small time constants and very high speed sensing. This type of structure can be used in fabricating devices such as flow sensors, vacuum sensors, hot-wire anemometers and gas sensors [29].

A similar structure was presented for a flow sensor using a broader bridge enabling the integration of thermopiles. In this case, the flow is over the top surface of the chip [30].

A thin-film bolometer, consisting of a thin metal resistor on the top of a silicon carbide membrane, has also been fabricated using porous silicon as the sacrificial material [4]. The large separation between the membrane and the substrate that is possible using

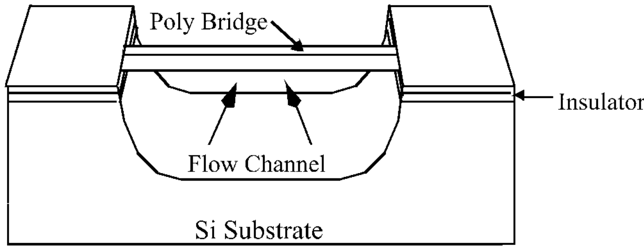



FIGURE 9.26. An example of a polysilicon bridge that could be used as a flow or other type of sensor. The flow channel beneath the bridge is formed by making part of the substrate porous, then removing the porous material in a hydroxide solution. Taken from [4].

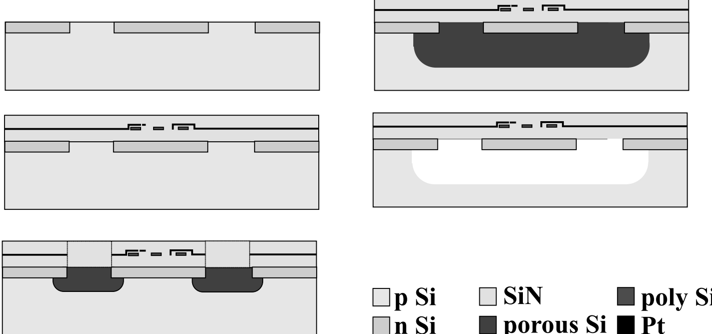



FIGURE 9.27. Process sequence of the bulk micromachined micro hotplate. Redrawn from [31].

this technique allows for high device sensitivity and thermal isolation. The larger the separation distance, the higher the thermal resistivity between the membrane and the substrate, resulted in reduced parasitic heat transfer and increased thermal sensitivity. A further example of such an application is given in Figure 9.27.

Removal of the porous silicon creates free-standing structures for thermal isolation. Alternatively, the porous silicon can be left as porous silicon or oxidized to make a thick oxide. The thermal conductivity of silicon is of the order of 156 W/(m K). Porous silicon, on the other hand, has a thermal conductivity in the range of 0.1–2 W/(m K), depending on the porous structure, which can be improved slightly with oxidation [32].

The above structures used sacrificial porous silicon for thermal isolation. It can also be used for mechanical isolation to improve $Q$-factors for resonators. Figure 9.28 shows

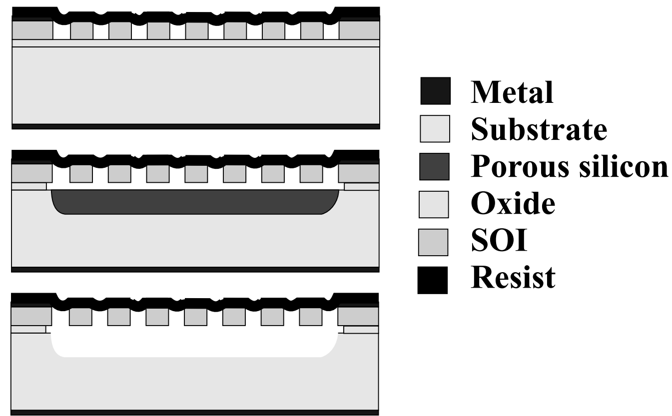



FIGURE 9.28. Process flow for a resonating structure with an increase in $Q$-factor using sacrificial porous silicon. Taken from [33].

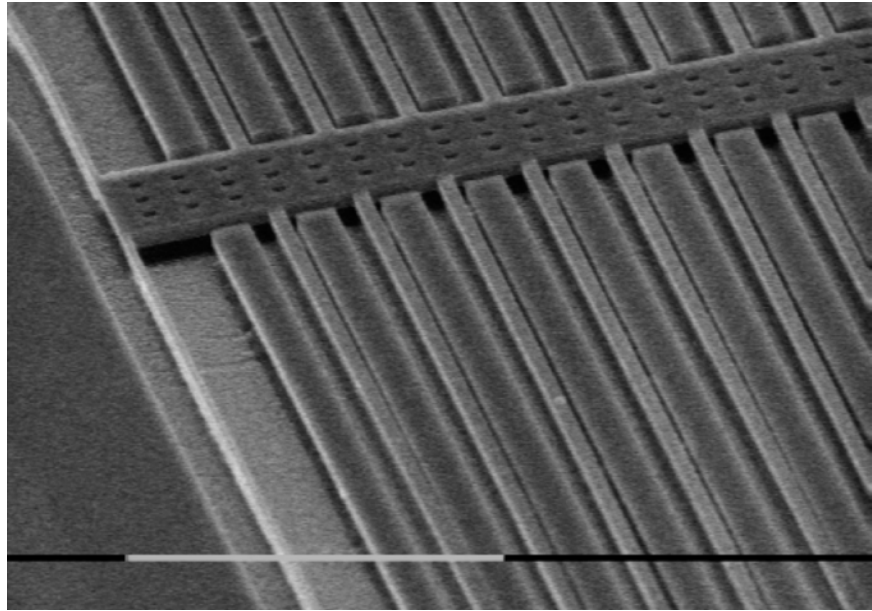


FIGURE 9.29. An example of an accelerometer fabricated using selective sacrificial porous silicon [22].

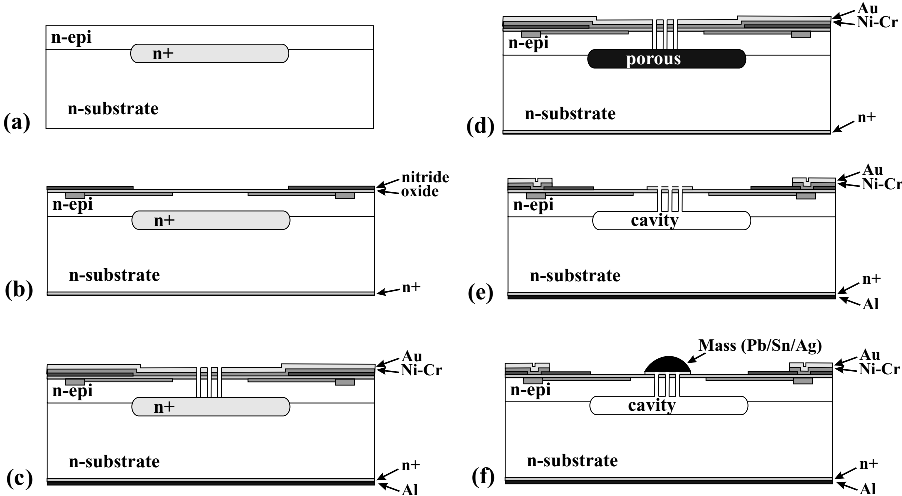



FIGURE 9.30. Fabrication process for an accelerometer. Redrawn from [33].

an example of a process flow [33]. Without sacrificial porous silicon, the final air gap would be limited to the oxide thickness. The porous silicon technique enables this gap to be significantly increased. In this case, air gap of 80 μm was achieved. An increase in air gap from 2 μm to 30 μm yielded an increase in $Q$-factor of 100%.

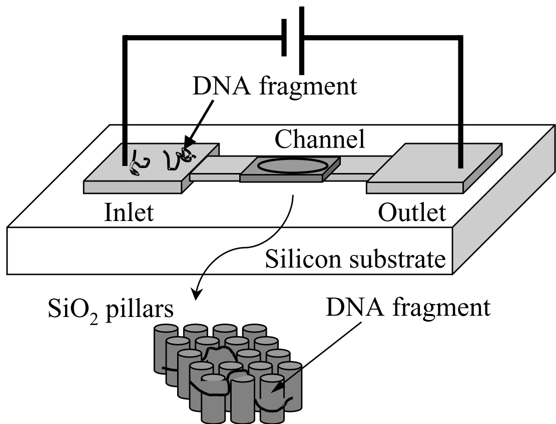



FIGURE 9.31. Basic structure of the DNA separation chip. Taken from [34].

### 9.3.4. *Accelerometer*

A number of processes have been proposed for the fabrication of accelerometers using both micro and macroporous silicon. A lateral accelerometer has been fabricated using an n-type epi as the mechanical material and the p-type substrate as the sacrificial layer [22]. An example of one of these structures is given in Figure 9.29. Macroporous silicon has also been applied, as shown in Figure 9.16.

A process using an n+ buried layer as a sacrificial layer is given in Figure 9.30 [34]. The relative etch rate of n+- and n-type silicon was given in Figure 9.2.

The mass is supported by eight cantilevers and the output through four Wheatstone bridges. Using an amplifier with amplification of 200, the accelerometer yields an output of approximately 0.24 V/g using all four bridges. The resonant frequency has been measured at 2.82 kHz.

### 9.3.5. *DNA Separation Chip*

Macroporous silicon can be used to make oxide pillars suitable for a DNA separation chip. The pillars need to be in a channel and an electric field is placed between the ends of the channel to pull the DNA through. The structure of this device is given in Figure 9.31 [35]. The basic process sequence is shown in Figure 9.32. Firstly, straight holes are etched using the macroporous silicon process described above (Figure 9.32a). Leaving the nitride mask in place the inside of the pores are oxidized (Figure 9.32b). The nitride mask is then removed and the silicon etched back using TMAH, which does not etch the oxide (Figure 9.32d). The advantage of this approach is that the spacing between the resulting pillars can be accurately controlled by the oxidation and reduced to well below the lithography resolution. The resulting pillar structure is given in Figure 9.33.

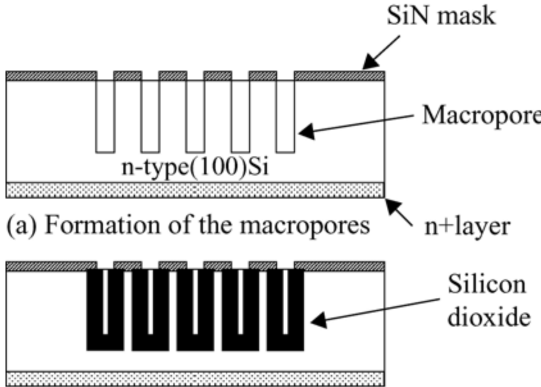


FIGURE 9.32. DNA separation chip process.

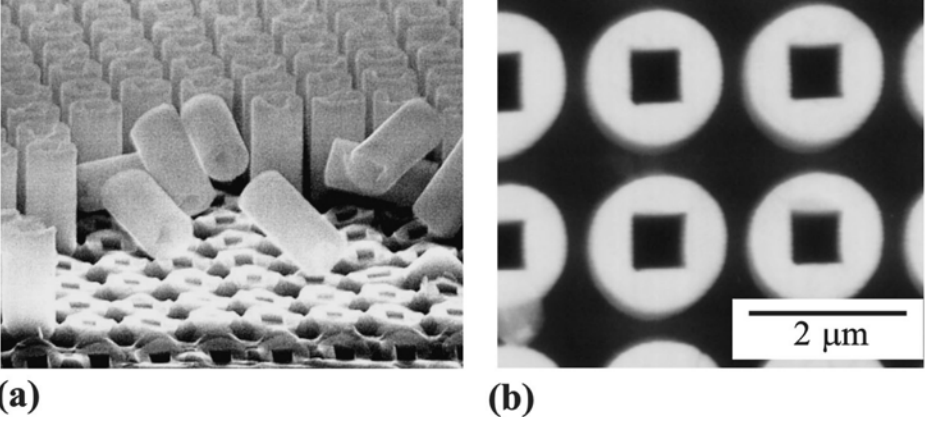



FIGURE 9.33. Pillar structure: (a) SEM photographs of pillars and (b) optical photograph illustrating the distance between the pillars.

## 9.4. CONCLUSIONS

Porous silicon was first observed during electropolishing when the current density was too low for a given HF concentration. Interest was evoked in the early 1990s with the discovery of photoluminescence and the potential for micromachining. Since these early investigations, both macroporous and microporous silicon have been shown to be valuable tools for micromachining.

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