Chapter 13

Microfabrication of Piezoelectric MEMS

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In this chapter an overview of processes for fabrication of MEMS using piezoelectric thin films as active layer in planar structures is presented. These structures are used in cantilever-like and membrane configurations for sensing and actuation. Key issues consist in findings of a compatible dry etching sequence for piezoelectric layer, electrodes and silicon. The method of compensation of the gradient of mechanical stresses in the thin films in order to obtain flat multilayer structures is demonstrated. Membrane thickness definition and liberation are obtained by DRIE of silicon on insulator (SOI) substrates or by surface micromachining. The platinum bottom electrode turned out to be a useful mask for deep silicon etching of narrow grooves. The complete process has successfully been used to fabricate flat cantilevers, ultrasonic transducers and pressure sensors. Excellent permittivity and transverse piezoelectric coefficient of PZT and AlN have been obtained with complete devices. Several examples of piezoelectric devices (ultrasonic transducers, acoustic sensor, damping control, RF switches) presented in this paper have been developed during the last years. It has been demonstrated that the microfabrication of piezoelectric MEMS based on PZT or AlN thin films is the versatile and reliable technology. Most of the developments are based on PZT sol-gel textured films, however some efforts have been done for integration of AlN for piezoelectric MEMS. In this context, the advantage of AlN is the low thermal budget processing and the possibility of post-CMOS above-IC integration. Other examples of application like ferroelectric memories, nanopatterning and local growth of PZT are presented as well.

1. Introduction

Piezoelectric thin film are useful in various actuation and sensing devices requiring large output signals, low noise, or high frequency operation (see [1], [2] for a review). An important advantage lies in the fact that a planar structure is able to give excursion and strain detection in the out-of-plane direction, which is very useful for instance in scanning probe techniques [3]. Today, there is a growing interest in the field of micro-electro-mechanical systems (MEMS) for the integration of smart materials with good actuation and/or sensing capabilities. In particular, $Pb(Zr_xTi_{1-x})O_3$ (PZT) and AlN thin films are of primary interest [4].

Piezoelectric Micro-Electro-Mechanical Systems (pMEMS) contain at least two elements: bulk silicon frame and built on it a piezoelectric deflection element with its electrodes. Micromachining of silicon, which refers to the fashioning of microscopic mechanical parts out of a silicon substrate, has emerged as an extension of IC's fabrication technology [5], [6]. During the last 25 years, it has been successfully employed to produce a variety of mechanical microstructures of a great diversity (beams, diaphragms, grooves, orifices, sealed cavities, pyramids and needles) and has driven the rapid progress of MEMS. However, the silicon substrate represents often only the **structural** element defining the mechanical properties of the device and, usually, a specific functionality needs to be added. It is the role of **functional materials** such as piezoelectric thin films to provide a direct transformation between a driving signal or a read-out signal and a sensor or an actuator parameter. The basics of silicon MEMS microfabrication technologies such as photolithography, pattern transfer with dry and wet etching techniques, and common thin films deposition (SiO_2, Si_3N_4, poly-Si, Al, Cr, Ni, Au) have been described extensively in the literature [7]. The microfabrication of piezoelectric MEMS suffers from inadequate micromachining processes and very few references have been published on the subject [8], [9], [10]. The integration of piezoelectric thin films like PZT or AlN, and "exotic materials" used as diffusion barrier (TiO_2), electrodes (Pt) or seed layers ($PbTiO_3$) requires new and specific micromachining processes that are not available in standard IC's processing.

The critical tasks, the dry etching of PZT, AlN and electrode thin films are, not trivial as the volatility of their reactive by-products is low or very different for each compound (e.g. the boiling point of: $PbCl_2$: 950 °C, PbF_2 : 1290 °C, $TiCl_4$: 136 °C, TiF_4: 284 °C, $ZrCl_4$: 334 °C, ZrF_4: 600 °C [11]). There is thus a need for new patterning processes to afford micro scale resolution at reasonable etching rates and to find a process flow that avoids any degradation of the piezoelectric film. Another critical issue is the above-IC integration of piezoelectric MEMS. This can be solved by using low temperature (<450 °C) post-CMOS process for deposition and patterning of the piezoelectric layer (e.g. AlN).

The aims of this paper are as follow:

- To provide an overview of micromachining tools developed to produce piezoelectric MEMS with microscale features,
- To highlight key issues such as stress compensation, process flow, advanced SOI substrates,
- To demonstrate the fabrication and some properties of PZT/Si microdevices.

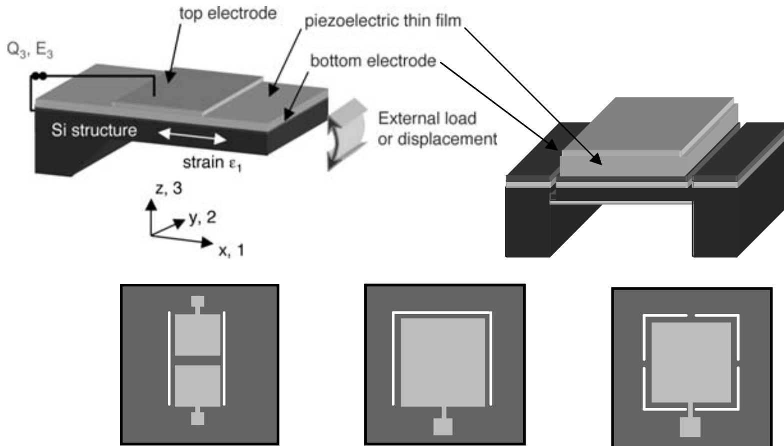


Fig. 1. Laminated piezoelectric layer—silicon deflecting structures used in MEMS: bridge, cantilever and suspended membrane.

2. Materials and Substrates for pMEMS

Most piezoelectric devices are based on laminated PZT/Si planar structures, which are defined as a flexible supporting silicon structure (5–20 μm thick) coated with a piezoelectric thin film (see Figure 1). Depending on applications, various geometry and clamping conditions can be considered: from the very simple cantilever to a fully clamped membrane or any partially clamped diaphragms (for instance, membrane fixed to the frame by few bridges). The electromechanical coupling is provided by the transverse piezoelectric coefficient $e_{31,f}$.

To succeed in the microfabrication of such 3D device, a number of important issues have to be addressed:

- the deposition of uniform, high quality PZT or AlN and electrode thin films directly on a wafer has to be solved,
- specific micromachining methods and process flow have to be developed,
- the mechanical stress through the structure need to be compensated to avoid any residual bending,
- the thickness of the supporting Si structural membrane should be uniform and the border conditions defined precisely.

Two different techniques have been used to fabricate devices based on planar PZT/Si structures. First, surface micromachining has been mainly employed to make simple accelerometers [12] (ZnO), [13] (PZT). One advantage of this method is that e.g. the poly-silicon layer can be used to define precisely the thickness of the supporting structure. However, the etching of the sacrificial layer (PSG) in HF solution often destroys the PZT thin film. Even with a silicon nitride encapsulation, pinholes occurred and the film was damaged. It has been also observed that the roughness of the poly-silicon layer disturbs strongly the growth of the PZT film resulting in low piezoelectric

Table 1. Typical materials used in piezoelectrically actuated Si based deflecting structures

Materials	Growth methods	Thickness	Typical stress (MPa)	Patterning methods
Silicon wafer/ SOI	Czochralski/bonding and polishing	390 micron; 1 to 50 μm of device Si on burried SiO_2		DRIE; wet etching (KOH, TMAH)
Amorphous SiO_2	Thermal wet oxidation	max. 2000 nm	-300 ± 5	ICP plasma etching; wet etching (BHF)
Si_3N_4	LPCVD	max. 200 nm	0 to +700	ICP plasma etching
Pt bottom and top electrode	PVD sputtering	100 to 300 nm	+550	ICP plasma etching
PZT 53/47 {100}	PVD Sputtering or CSD sol-gel	500 to 4000 nm	+110 (*unpoled*) +180 (*poled*)	ECR/RF plasma etching; wet etching (HCl/HF)
AlN	PVD Sputtering	500 to 2000 nm	−200 to +220	ICP plasma etching; wet etching (H_3PO_4)
Au/Cr top electrode	PVD evaporation	100 nm/10 nm	+280	lift-off

coefficients. Finally, the geometries and size of surface micromachined piezoelectric devices are limited by the rate of the lateral etching of the sacrificial layer. Beams larger than 50 μm are difficult to release. The second technique is based on classical silicon bulk micromachining. Among reported devices, one can point out micromotors [14], [15] (PZT), [16] (ZnO), accelerometers, [17], [18] (PZT), audio microphone and microspeakers [19] (ZnO), 2-D scanners [20] (PZT), AFM tips [21], [3] (PZT) and ultrasonic transducers [22], [23] (PZT). Here, the limiting factor is a uniformity of the silicon structure obtained with standard wafers. In order to obtain the uniform thickness of a thin Si structure, silicon on insulator wafers (SOI) need to be used. Membranes in thickness range from 0.5 to 50 microns with tolerances better than 1% can be fabricated by DRIE using the buried oxide as etch stop layer. The inconvenience in this type of substrate is the unknown value of the stress in the buried SiO_2.

Films in laminated structures exhibit a mechanical stress (tensile or compressive), which is function of materials and deposition methods. The stress gradient in the thin film induces bending to the freestanding structure or buckling to the clamped structures. If the overall residual stress is non zero, a residual bending occurs that can reduce or even destroy the device sensitivity. The stress in piezoelectric PZT thin films depends on composition, texture, thickness and poling [10]. To achieve precise stress compensation, the effect of poling has to be considered as well. Due to the re-orientation of c-domains along the poling field (z-axis), the tensile stress increases further. Table 1 shows that the film stresses of a laminated PZT/Si structure are all tensile except the thermal SiO_2, which is compressive (−300 MPa). Stress compensation is achieved by adjusting the thickness of thermal SiO_2 to about 1000 to 1200 nm, depending on thickness of PZT (Figure 2).

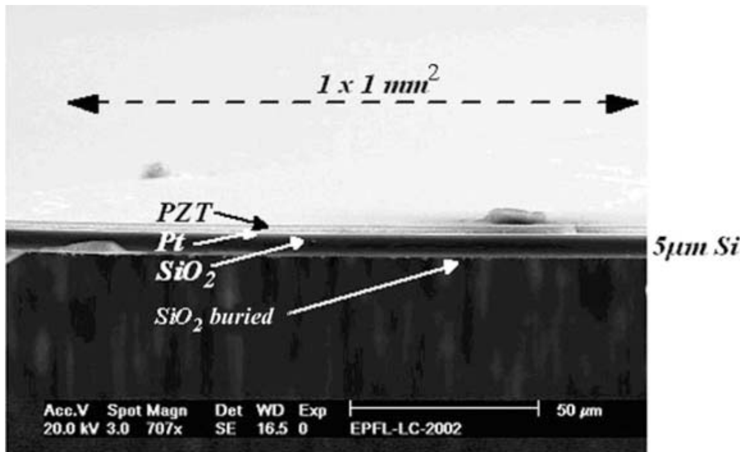


Fig. 2. SEM cross-section of flat PZT/Pt/SiO_2/Si square membrane (7 micron thick and 1 × 1 mm^2 large).

3. Processes and Tools for Patterning of pMEMS

3.1. Process flow for the microfabrication of PZT/Si planar structures

Like any IC's classic process flow, the microfabrication of planar PZT/Si deflecting structure is based on several iterations of film deposition—photolithography—etching [7]. Figure 3 shows the generic process flow for the microfabrication of planar cantilever structures based on SOI substrate and AlN as active layer. In general, starting with double side polished and oxidized silicon based substrate (Si wafer, SOI, polySi on SiO_2/Si), an adhesion layer (e.g. Ti/TiO_2), a bottom electrode (e.g. Pt, Ir, IrO_2, RuO_2) and eventually a seed layer (e.g. $PbTiO_3$, TiO_2) are deposited by PVD sputtering [24, 25]. On top of electrode or of seed layer, the piezoelectric thin film is deposited by sol-gel CSD [10] or by sputtering [26]. Top electrode is deposited and patterned either by lift-off (Au/Cr) or by plasma dry etching (Pt, Al). To give access to the bottom electrode, vias are opened through the piezoelectric film by wet or dry etching. The frontside shape of the structure (the grooves or gap surrounding the membrane) is then patterned through the piezoelectric layer/electrode/SiO_2 stack and through Si defining the depth of grooves. Bulk silicon micromachining from the wafer's backside is then performed to define the thickness of the structure (usually between 5 and 20 μm). The process is either dry (deep silicon etching in a plasma reactor) or wet in KOH solution (see [6] for review). The definition of precise and uniform silicon thickness (for example: 10 ± 1 μm thick silicon cantilever out of a 390 μm thick wafer) is of primary importance as the device sensitivity is usually a function of 1/thickness^2. In order to increase the precision of membrane thickness definition several solutions are proposed:

- accurate etching time measurement supposing constant process conditions,
- etch-stop obtained on n-doped epi-layer [27]
- Silicon-On-Insulator (SOI) used as substrate [23].

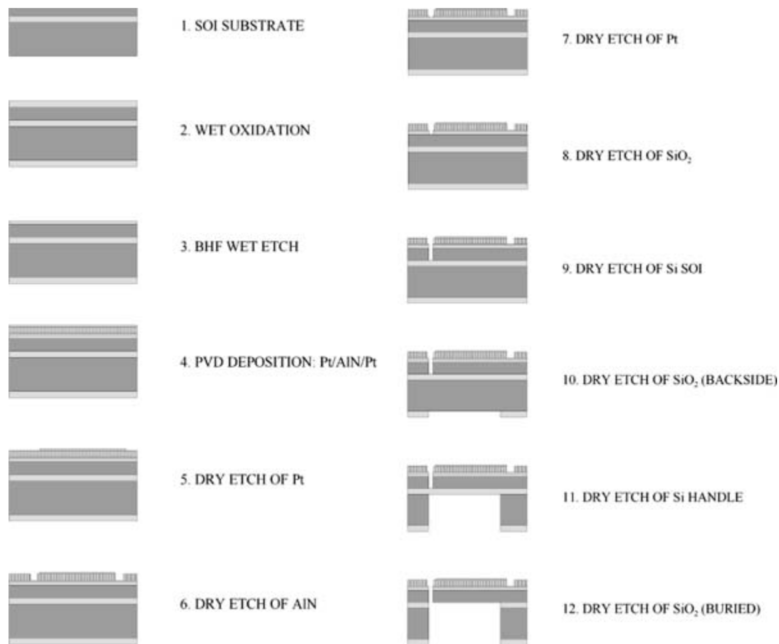


Fig. 3. Generic process flow for the microfabrication of piezoelectric actuated Si-based cantilever (cross section).

The micromachining steps of this process flow use many individual deposition and patterning processes. Details on general issues such as photolithography or silicon thermal oxidation can be found in [7] or in the process book of the Center of Microtechnology (CMI)—EPFL [28]. However, some of the processes are specific for microfabrication of piezoelectric MEMS and are described below.

3.2. Basics of patterning

Dry etching using reactive plasma has spread widely throughout the VLSI processing field because of its ability to fabricate fine-line semiconductor devices. However, the resolution of conventional RIE when decreasing the size of patterns is limited, because the operation pressure of RIE is too high to etch these patterns anisotropically. Moreover it is difficult to obtain a high etch rate because the plasma density of conventional RIE is limited. In case of piezoelectric MEMS the additional difficulty is related to the patterning of noble metals or refractory oxides, both exhibiting very low volatility. To overcome at least partially limitations of patterning such structures, a new process using high density plasma with low ion energy (to avoid damage of the piezoelectric layer and of the photoresist) and operating at lower pressure (lower backscattering, no fencing) is required. The most popular are actually inductively coupled plasma (ICP) sources (see [29] for review). However, other type of reactors like Helicon Wave Plasma (HWP), planar Electron Cyclotron Resonance

(ECR) or Multifrequency Reactors (ECR/RF, RF/HF) have been extensively studied for laboratory and industrial applications [30], [31], [32]. Recently the possibility of high anisotropic etching of submicron Ir/PZT/Ir ferroelectric capacitors by using a Dual Frequency High Density reactor operating at 380 °C has been reported [33], [34]. PZT piezoelectric MEMS microfabrication requires many different thin film patterning processes as well as silicon bulk micromachining. In following sections, selected topics that are specific to the microfabrication of piezoelectric devices will be presented:

- Top electrodes patterning,
- Wet and dry methods for patterning of thin (PZT, AlN) and thick (PMN-PT) films,
- Dry etching of bottom electrodes (platinum, RuO_2, iridium),
- Silicon bulk and surface micromachining.

3.3. Patterning of top electrodes

To collect the electrical charges on the PZT film different types of electrodes need to be deposited and patterned (Au/Cr, Pt).

Compared to platinum, Au/Cr top electrodes have two advantages:

- the patterning of Au/Cr top electrodes does not require plasma methods, as lift-off process is very versatile and offers sufficient resolution (micron scale) for MEMS applications,
- Au/Cr top electrodes do not need post-deposition annealing.

Au/Cr top electrodes are deposited by Joule effect (Au) and e-beam source (Cr) in common evaporator and patterned by lift-off using a negative photoresist. Figure 4 illustrates the 100 nm thick Au/Cr top electrode obtained by lift-off on top of the 50 μm × 1000 μm cantilever. The lateral resolution is only limited by the resolution of the mask and the thickness can reach few hundreds of nanometers.

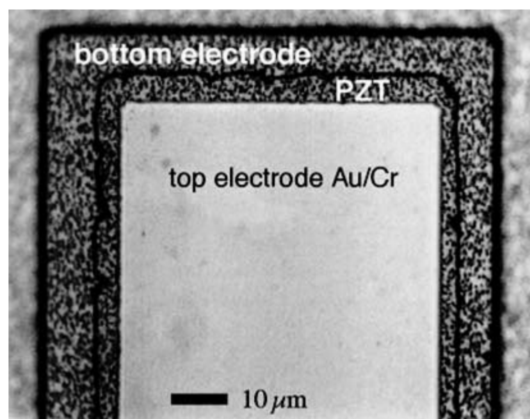


Fig. 4. Optical image of top view of the tip of a 100 × 500 μm^2 PZT/Si cantilever.

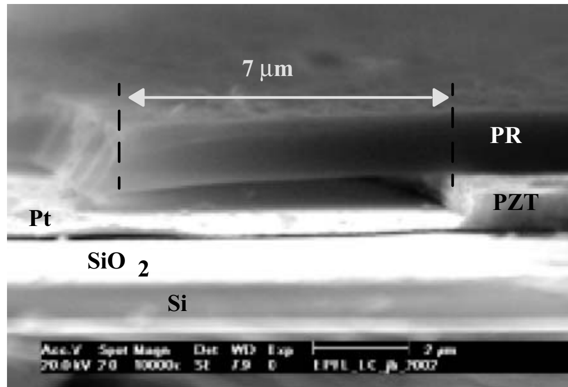


Fig. 5. SEM image cross-section of photoresist/PZT after wet etching of PZT (lateral underetch is 7 μm for 1 μm thick PZT layer).

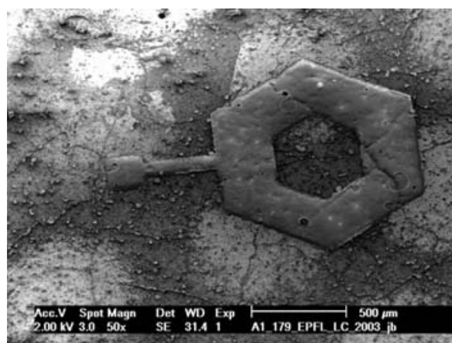
As for platinum top electrode, it is obtained in three steps:

- PVD deposition of 50 to 200 nm Pt at room temperature,
- High temperature annealing to increase the adhesion, to restore the interface Pt/PZT and to recrystallize Pt
- Photolithography and dry etching to shape the top electrode (effective size of device).

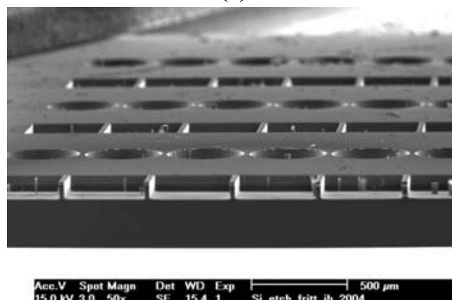
With PVD deposited platinum, the PZT surface is damaged by the ions bombardment as well during deposition and etching. Thermal annealing is then required to restore the interface [35]. The maximum thickness is limited by the selectivity between platinum and photoresist mask during the dry etching.

3.4. Wet etching of piezoelectric thin films

The wet patterning of PZT thin films is a critical point in piezoelectric MEMS microfabrication. Despite the lack of etch rate control and photoresist undercut, the wet etching of PZT films remains a very versatile, fast and cheap method to open large areas ($> 50 \times 50\ \mu m^2$) like vias, with rather poor lateral resolution control. Because of high concentrations of hydrofluoric acid (HF), most of etch recipes are not selective to SiO_2 and to the TiO_2 (adhesion layer of the platinum bottom electrode). Delaminating of the structure can thus occur. In terms of etching rate, HCl solutions are very effective and selective etchants [36]. In our works, the standard solution of 30 ml of concentrated HCl (37%), 70 ml of water and 0.2 ml of HF has been used. At 56 °C, the etching rate is about 50–100 nm/s. Figure 4 shows the top view of a $500 \times 100\ \mu m^2$ micro cantilever where the 1 μm PZT film has been patterned by wet etching. Underetching and profile irregularities as large as 5–10 μm can be observed which give a masks design rule (geometry tolerance) of about 10 times the PZT thickness (Figure 5). Under these conditions wet etching of narrow patterns (e.g. grooves of width 3–10 μm, capacitors below 25 μm^2) is thus impossible and dry etching techniques should be employed.



(a)



(b)

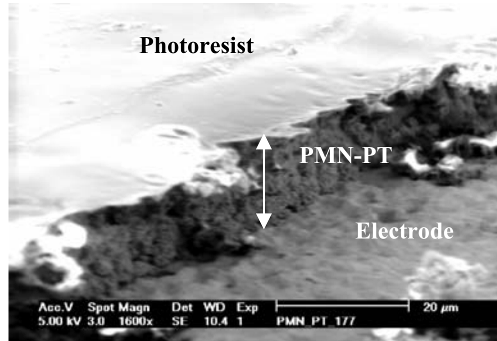
Fig. 6. (a) SEM top view of wet etched 10 micron PMN-PT thick film on Si substrate. (b) SEM view of backside of partially etched Si from wafer after the firing of PMN-PT film.

AlN sputtered thin films can be patterned in pure H_3PO_4 acid at 80 to 100 °C. The method is not isotropic and the etching rate depends on crystallographic orientation. Typically the etch rate is between 30 and 100 nm/sec.

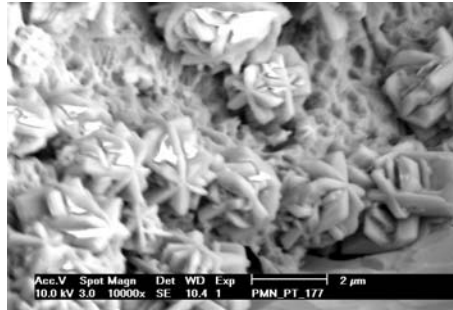
Recently the integration of dense PMN-PT thick films on Si substrate has been attempted. The device fabrication requires patterning of up to 20 μm thick PMN-PT layer. Standard photoresist (Shipley 1818, 3.6 μm thick) could be applied because of the limited porosity in the sintered layer. Wet etching with a HF/HCl solution at 55 °C enables the patterning of relatively large devices (larger than $100 \times 100\ \mu m^2$, Figure 6). The anisotropy of patterns is satisfying and almost vertical sidewalls were observed. Some residues (Figure 7) visible at the pattern sidewalls and on the substrate can act as the etch stop layer preserving from larger underetch.

3.5. Dry etching of piezoelectric thin films

As the size of MEMS critical features shrank below 10 μm, the dry etching of PZT or AlN becomes mandatory to obtain a high degree of anisotropy, smoothness and preserved shape of profiles. The principal requirements for a dry etching process of piezoelectric films are:



(a)



(b)

Fig. 7. (a) SEM side view image of of wet etched 10 micron PMN-PT thick film, (b) details of the sidewall of etched film.

- Sufficient selectivity to the photoresist (higher than 0.5) and with respect to the bottom electrode (Pt),
- High anisotropy to define precise micron-scale geometries (e.g. grooves, capacitors),
- High etching rate,
- No damage to the piezoelectric films and no patterning residue.

The dry etching of PZT films is not obvious as there is no common halogenous gas that forms volatile compounds with all three elements (Pb, Zr, Ti) to guarantee the residue free removal of film. The volatility of the reactive etch by-products of Pb, Zr and Ti is variable and limited [37] and energetic ion bombardment is often required to obtain the uniform removal of PZT layer. First developed processes used pure argon ion milling or Reactive Ion Etching (RIE) in simple parallel plate or inductively coupled plasma (ICP) reactor. Zeto [38] demonstrated etch rate up to 100–250 nm/min with argon ion milling. However, sloped walls (35°–70°), low selectivity to the platinum bottom electrode and photoresist mask as well as material redeposition on the sidewalls were the limiting factors. To overcome these drawbacks, Reactive Ion Etching (RIE) with halogenous gases should be employed. Chlorinated plasmas were generally employed because of the low melting point of metal chlorides with respect to the equivalent metal fluorides (e.g. $PbCl_3$, PbF_4). However, fluorine ion bombardment (CF_4, SF_6, C_2F_4) was shown to be more selective with respect to the platinum electrodes.

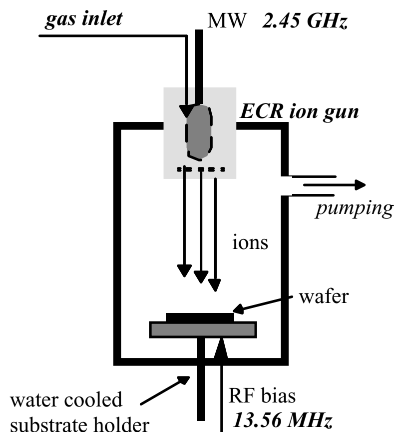


Fig. 8. Schema of dual frequency ECR/RF RIBE reactor [44, 45].

Etch rate of PZT has been increased up to 100 nm/min with monochlorotetrafluoroethane (HC_2ClF_4) as etch gas and 500 W RF power in a standard parallel plate reactor [38], but in this case, the stability of the photoresist was the limiting factor. For films thicker than 250 nm, the RF power has to be dramatically reduced down to 150 W to keep the photoresist mask removable. At such power level, the etching rate is only 13 nm/min. This example is representative of the problems occurring in RIE of PZT films. It is very difficult to find a trade-off between: reasonable PZT etch rate, photoresist dimensional stability and removability. Other studies gives similar results in term of etching rates (10 to 40 nm/min) in HC_2ClF_4 [39], in C_2F_6/Cl_2 [40] or in CF_4/Cl_2 [41] gases. Recently, Chung et al. [42] reported the etching process of PZT using ICP reactor and HBr/Ar gas mixture. An etch rate of 90 nm/min and a steep etch profile of 70° has been achieved.

Reactive Ion Beam Etching (RIBE) in a dual frequency ECR/RF reactor [43], [41], [44], [45] allows much lower working pressure than the RIE/ICP process (1 to 10 mPa compared to 1–10 Pa). The risk of material redeposition is reduced and the verticality of the sidewalls is improved thanks to the directionality of the bombarding ion beam. The bombardment of a reactive ion beam with gases such as SF_6, CF_4 or CCl_4 is very favorable to reduce the level of energy needed for the etching process and thus to obtain better trade-off between photoresist stability and etching rate.

The homemade reactor we used was based on a commercial ECR ion gun [44] as illustrate in Figure 8. The capacitive coupling of the substrate holder to a 13.56 MHz RF power supply contributes to the acceleration of the ions bombarding the substrate (negative bias voltage).

For RIBE of PZT films, a process with low ion energy ions and low operating pressure (see Table 2) has been developed. Best results were obtained by mixing both chlorine and fluorine gases and light Ar ion bombardment [45]. Photoresist stability was improved by hard baking at 150 °C in air and by keeping the moderate ion bombardment (<0.75 W/cm^2) during the process.

Dense, up to 2 μm thick PZT films have been etched with anisotropy close to 90°, without residue (Figure 9) and without degradation of PZT structure. Higher

Table 2. Process characteristics for etching of PZT and Pt with ECR/RF ion gun [30, 45]

	PZT Etch Process	Platinum Etch Process
Gases	40% CCl_4 / 40% CF_4 / 20% Ar	85% CCl_4 / 15% Ar
Pressure	10 mPa	5 mPa
RF bias	60 W (max. 0.75 W/cm^2)	50 W (max. 0.65 W/cm^2)
Etch rate	max. 70 nm/min	max. 45 nm/min
Selectivity	0.5 to photoresist, 1.5 to Pt	0.75 to photoresist, 2.5 to PZT
Mask	Shipley 1818, 2.3 μm, hard bake at 150 °C, 30 min, air oven	Shipley 1805, 1.5 μm, hard bake at 150 °C, 30 min, air oven

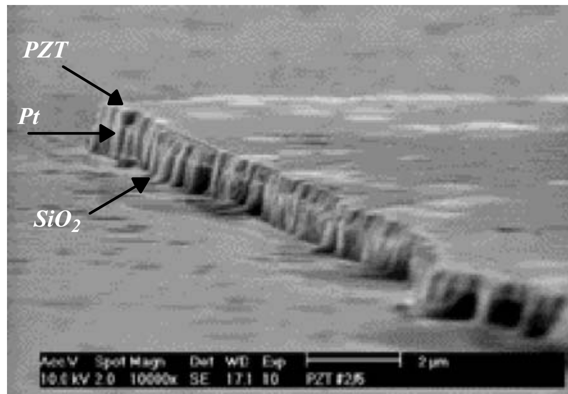


Fig. 9. SEM side view image of patterned PZT thin film, working pressure = 0.01 Pa, 60 W RF bias, optimized etching chemistry. Photoresist mask removed [45].

working pressure (> 0.5 Pa) or higher RF bias (> 100W) lead to destroying of PZT film (Figure 10).

As demonstrated for patterning of PZT for FERAMs cells the ferroelectric properties could be preserved during patterning processes. The impact of patterning process (plasma etching in ECR/RF RIBE) on properties of ferroelectric capacitors has been investigated. Properties of Pt/PZT/IrO_2-Ir capacitors have been monitored after all possible process steps:

- after top electrode etching (Figure 11a),
- after PZT dry etch (Figure 11b),
- after IrO_2/Ir/TiN dry etch (Figure 11c).

In contrast to most of literature data related to patterning of ferroelectric capacitors, here no degradation of PZT ferroelectric properties at different steps of patterning sequences was observed. Remanent polarization of 13 μC/cm^2 and maximum electric field of 400 kV/cm have been measured during all fabrication process and before final annealing in oxygen. This fact can be attributed to the patterning process (ECR RIBE) operating at very low working pressure (10 mPa) and using low energy ion bombardment (< 25V) in comparison to major ICP plasma reactors [46], [47].

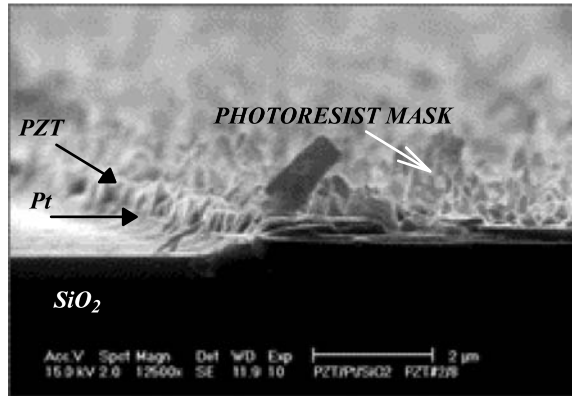


Fig. 10. SEM side view image of patterned PZT thin film, working pressure = 0.5 Pa, 120 W RF bias, optimized etching chemistry.

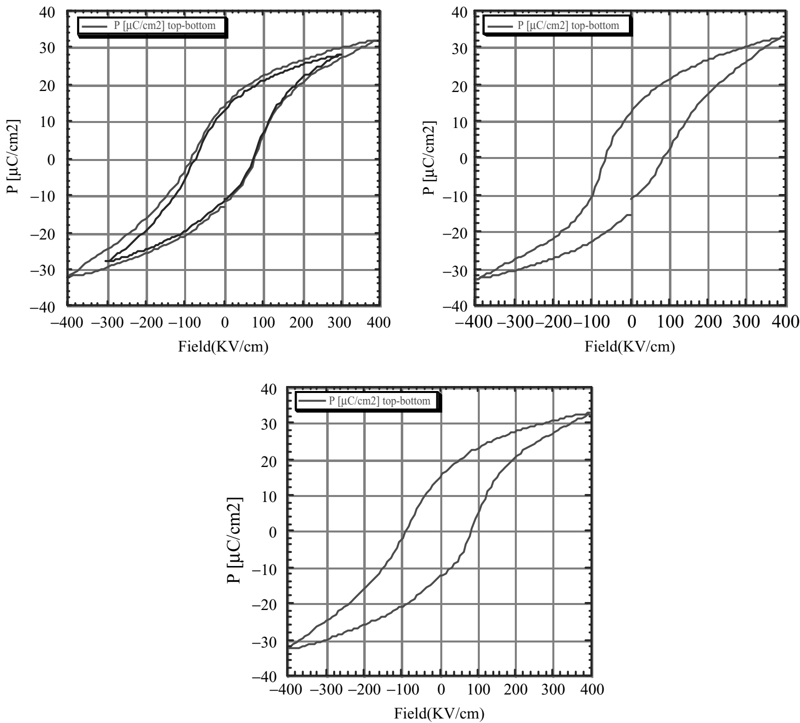


Fig. 11. Ferroelectric loops measured on Pt/PZT/IrO_2/Ir stack: (a) after Pt top electrode etching, (b) after PZT dry etching, (c) after IrO_2/Ir dry etching.

Dry etching of AlN is based on ICP process. Typically Ar/Cl_2 flux ratio is 1/3, the process pressure 8 mTorr and bias RF Power of 150W is applied. The etching rate yields 200 to 330 nm/min but it strongly depends on the morphology of AlN layer. Selectivity to Pt is 1:10 and to photoresist mask 1:0.5. When using a standard photolithography

process, the AlN used to be attacked by basic solution of the developer. This increases the roughness of AlN and leads to some alteration of the etching rate, micromasking and residues formation.

3.6. Dry etching of bottom electrodes

3.6.1. Platinum

Ferroelectric thin films for MEMS or memory applications require noble metal (platinum, iridium) or conductive metal oxide (RuO_2, IrO_2) electrodes. Due to their chemical inertness, the patterning of these materials is a difficult task. The platinum thin films can be patterned by wet etching: aqua regia [48] or electrochemical wet etching in concentrated HCl [49] are the most known methods. However, these recipes do not work with very thin structures (below 10 μm), are very sensitive to the platinum surface contamination, are often subject to underetching of the adhesion layer and, the selectivity to PZT is very low.

For piezoelectric MEMS, HDP dry etching techniques have to be chosen. There is only a small number of volatile compounds that can be formed with platinum (e.g. $PtCl_3$ decomposes at 370 °C in Cl_2, PtI_2 decomposes at 270 °C). In fact, the etching mechanisms are much more physical (ion bombardment) than chemical (formation of volatile reaction products). Most of recent developed methods have used RIE/ICP (Reactive Ion Etching with Inductive Coupled Plasma reactors), simple Ar ion milling or ECR/RIBE. In all cases [50], [51] several common limitations have been observed:

- Selectivity problems with photoresist
- Hard masks (TiN, SiO_2) masks are not common to use in presence of PZT,
- Metal residues on the sidewalls lead to fencing,
- Poor patterns anisotropy with ion milling,
- Due to the strong ion bombardment photoresist mask gets harder and after stripping the organic residues remain.

In our studies, chlorine based RIBE process with dual-frequency ECR/RF plasma [30], [31] (see Table 2). Figure 12 shows a SEM image cross-section of the edge of 100 nm thick Pt film deposited on Si_3N_4/SiO_2 membrane. The anisotropy of the pattern is close to 90° and the selectivity to Si_3N_4 is excellent (no overetch into Si_3N_4). With a RIE/ICP reactor from STS, best results have been obtained with Cl_2 flow rate of 20 sccm, Ar flow rate of 70 sccm, working pressure of 1 Pa, RF plasma power of 800 W and RF substrate bias power of 150 W. The etching rate was lower (32 nm/min) than the one obtained by RIBE and the selectivity was 0.35 and 0.5 with respect to standard photoresist (Shipley 1805) and SiO_2 respectively. Figure 13 shows the profile of Pt/SiO_2 after ICP etching at 1 Pa. The curved shape of the photoresist and the thin film is typical of highly physical dry etching process. However, any redeposition of the metal on the mask sidewalls has not been observed. Both processes for Pt etching (RIBE/ECR and RIE/ICP) offer a good selectivity to PZT (> 2) and have been successfully applied for the patterning of platinum top electrodes. The photoresist mask is striped in Shipley Microposit Remover 1165 at 70 °C followed by low power ashing in plasma oxygen [10].

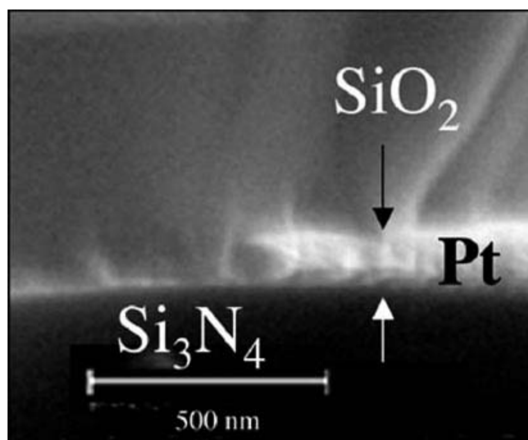


Fig. 12. SEM image cross-section of ECR dry etched Pt on Si_3N_4 membrane.

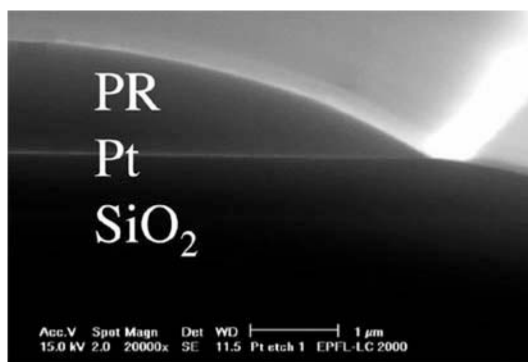


Fig. 13. SEM image cross-section of ICP dry etched Pt film.

3.6.2. Iridium

The patterning of Ir electrode is mostly related to fabrication of FeRAMs capacitors [52], [53]. RIE/ICP etching of iridium has been related by several groups [54], [55], [56], [57]. Chung et al. has used a hard mask (TiO_2) [54] or photoresist mask [55] testing chlorine, bromide and fluorine chemistries ($Cl_2/O_2/Ar$; $HBr/O_2/Ar$; $C_2F_6/O_2/Ar$, $C_2F_6/Cl_2/Ar$). Etch rates 40 to 60 nm/min has been obtained with chlorine. Clean profiles with Cl_2 and HBr when using a hard mask and with fluorine when using the photoresist were observed. Residue-free patterns, 50° sidewalls with fluorine-chlorine gases and Ar addition have been finally obtained. Chongying Xu et al. [56] have established the process for etching of Ir electrical contacts. By using XeF_2, in presence of Si source a good selectivity to IrO_2 and Pt has been achieved and Ir/PZT/Ir capacitors remained non-affected. Chiang et al. [57] has employed the $Ar/O_2/BCl_3$ gas mixture and TiN hard mask. The selectivity Ir/TiN up to 10, the Ir etch rate up to 66 nm/min (60%Ar/20%O_2/20%BCl_3, 1500W bias), fence free patterns and vertical ($>70°$) sidewalls were observed. Patterning of Ir/IrO_2/PZT submicron, ferroelectric stack has been

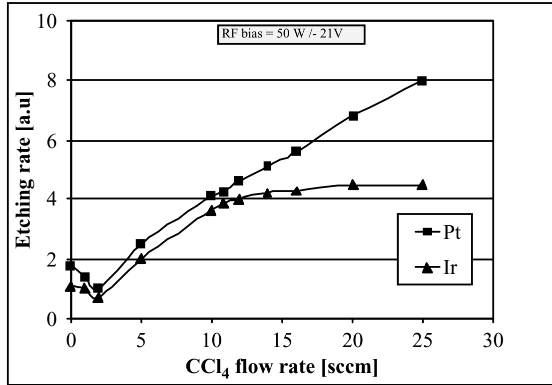


Fig. 14. Comparison of etching rates of Pt and Ir as function of CCl_4 percentage in Ar/CCl_4 mixture when using ECR/RF RIBE [10].

demonstrated and commercialized by Tegal [33]. Using the double frequency HDPe reactor operating at 380 °C the etching rate of Ir up to 100 nm/min with the sidewall profile better the 85° have been obtained.

Etching of Ir/IrO_2 stack for FeRAM applications was done with ECR/RF Ion Gun [10]. The 100 nm iridium bottom electrode was etched in $80\%CCl_4/20\%Ar$ mixture. Increasing of CCl_4 rate flow induces some enhancement of etching, however, a saturation of removal rate occurs when limited by formation of $IrCl_4$ product (Figure 14). Despite, the etch rate of Ir can be stimulated by RF substrate bombardment, the maximum etch rate 15 to 20 nm/min was obtained. Micron-scale resolution patterns without any impact on properties of ferroelectric capacitor or transistors have been performed (Figure 15).

3.6.3. Ruthenium oxide

For RuO_2 it has been reported that the etching in oxygen plasma is effectuated by the formation of volatile RuO_4 [58] and this process can be catalyzed by small addition

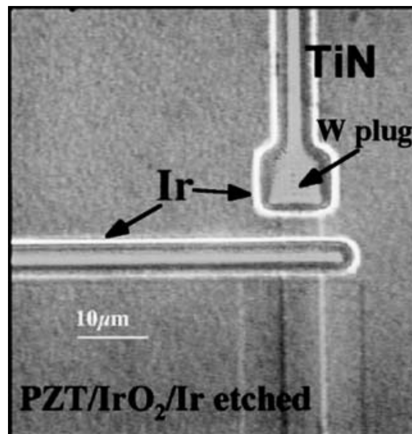


Fig. 15. Top view of $PZT/IrO_2/Ir$ stack etched with ECR/RF RIBE.

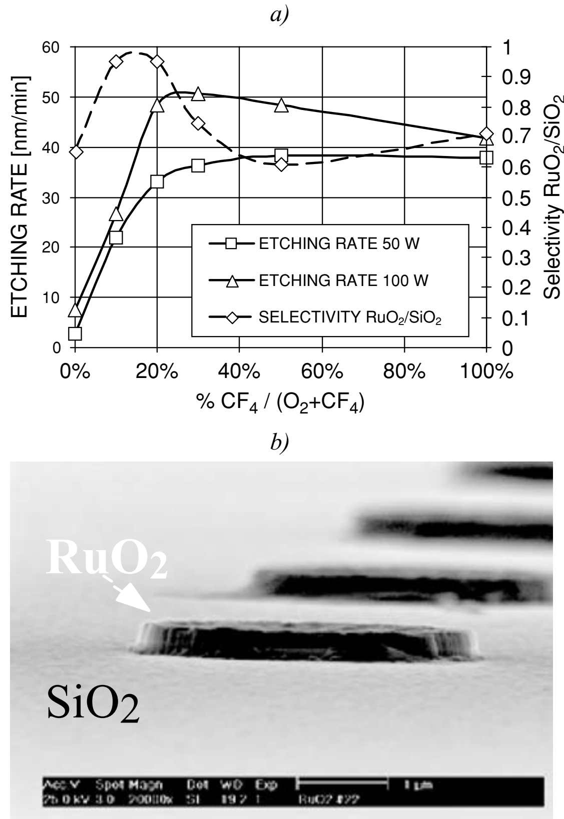


Fig. 16. Etching of RuO_2: a) effect of CF_4 concentration on etching rate of RuO_2 and the selectivity SiO_2/RuO_2, b) 3×3 micron^2 patterns obtained with ECR/RF RIBE [31].

of Cl- or F-based gas to O_2 plasma [59]. Most of these experiments were carried out in RIE/ICP systems where independent control of the energy and flux of the reaction species is not easy. Moreover, the working pressure range is usually about several Pa reducing the anisotropy and creating the polymer like residues. Unlike Lee [58], a very low etch rate with Cl was obtained even if O_2 was added. Only fluorine-containing gases provides reasonable etch rates [31]. As suggested by Desu [59] a small addition of fluorine gas to oxygen increases significantly the etching rate. When the CF_4/O_2 is used, the addition of 25% of CF_4 induces the increase of etching rate from 10 to 50 nm/min at 100W RF bias and from 7 to 35 nm/min at 50W RF bias. An interesting correlation with the selectivity to SiO_2 occurs—for low quantity of CF_4 the selectivity is poor because of low etching rate of RuO_2. On the other hand, the high (above 50%) proportion of CF_4 induces higher etch rate of SiO_2 which reduces the selectivity again. Finally, an optimal proportion of 20% CF_4/O_2 allows to achieve both high etching rate and good selectivity to SiO_2 underlayer. As shown in Figure 16 the 2×2 μm^2 patterns through 300 nm thick RuO_2 can be obtained with anisotropy higher than 80°. Smooth SiO_2 substrate surface is visible and no polymer-like residue due to decomposition of

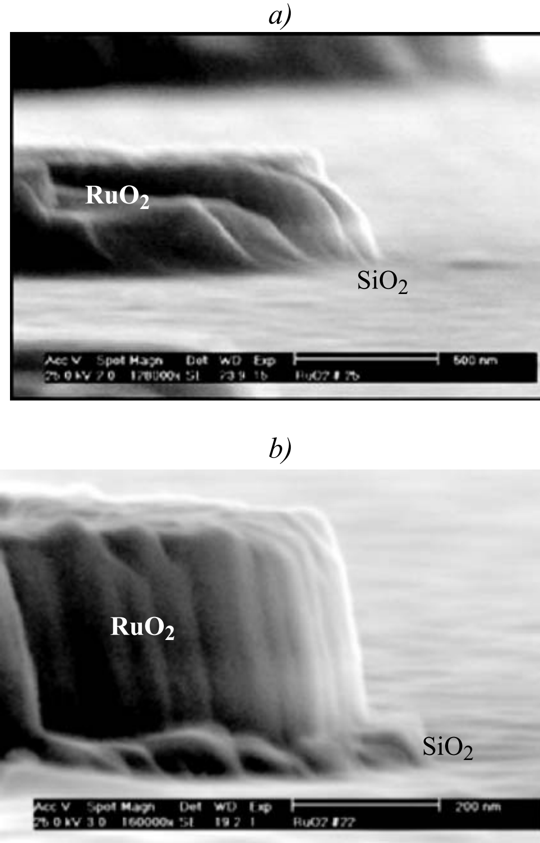


Fig. 17. Profiles of RuO_2 patterns obtained with a) SF_6/O_2, b) CF_4/O_2 mixture.

CF_4 [58] was observed; this fact is due principally to a low working pressure (typically 10 mPa) in ECR/RF system. Figure 17 shows the difference in etched profiles of RuO_2 when using a) SF_6/O_2 and b) CF_4/O_2 mixture; for the same process conditions the etch rates were similar, but etching in SF_6/O_2 results in lower anisotropy of patterns and lower selectivity to SiO_2.

3.7. Silicon bulk micromachining

To produce thin silicon supporting structures like beams or diaphragms, bulk silicon has to be etched in a uniform way, down to the desired thickness (usually thinner than 20 μm). As the sensitivity of a sensor based on a cantilever is proportional to 1/(silicon thickness)^2, precise control of the silicon thickness has a direct influence on the production of uniform and homogenous devices. To control accurately the thickness of the silicon structures, many wet-etching methods (KOH, TMAH) using an etch-stop on a very well defined n-doped epi [27] or highly p-implanted silicon layers have been developed [6]. However, these methods suffer from difficult and complicated process

implementation and stress non-uniformity. Despite a very low running cost, bulk silicon micromachining in KOH has important drawbacks:

- the shapes of the structures are restricted by the etching anisotropy (for example, V-grooves of 10 μm wide cannot achieve a depth larger than 7 μm due to the lower etching rate of the (111) planes),
- the etch rate in KOH depends not only on solution concentration and temperature, but also on impurity presence in Si wafer,
- the KOH is very aggressive against the PZT, AlN, and electrodes,
- the uniformity is limited to about ± 10–15 μm after etching 380 μm of silicon.

The dry and anisotropic plasma etching process offers much more flexibility in terms of design and is the solution of choice to define accurately small structure like very narrow gaps, grooves and even large surface in case of membrane patterning. The most commonly used process for deep silicon etching is the so-called "Bosch process" patented by Lärmer and Schilp [60]. By sequentially alternating etching steps (with SF_6 chemistry) and passivation steps (polymerization of the sidewall with C_4F_8), a deep anisotropic etching can be obtained on feature sizes ranging from submicron to several millimeters [61]. High etching rate of 7–10 μm/min enables a rapid fabrication of deep trenches and membranes. Figure 18 a) shows a SEM cross-section of a 2 × 30 μm

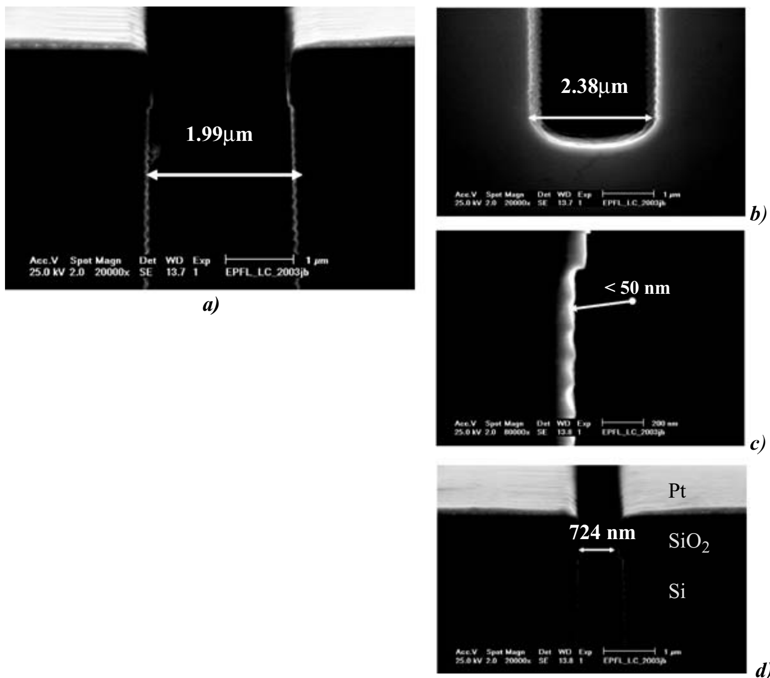


Fig. 18. SEM images cross section of 2 × 30 μm (AR = 15) groove etched through Pt/Ti/SiO_2/Si, and details of bottom and sidewalls of the slit (b,c). Pt has been used as a hard mask [10]. Submicron slit obtained by this method (d).

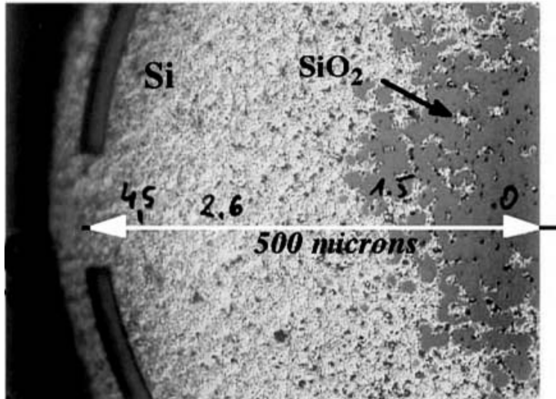


Fig. 19. Non uniformity of Si thickness at the bottom of 1 mm^2 large silicon membrane.

trench. Vertical sidewalls with aspect ratio of 1:15 have been obtained when using Pt bottom electrode as a hard mask even for submicron trenches (Figure 18 b, d) [10]. However, defining precise and uniform membrane thickness all over a wafer by deep silicon etching is a difficult task. It can be observed on Figure 18 c) that the bottom of the etched cavity is neither flat nor perpendicular to the sidewalls. This phenomenon can be explained by the ion scattering effect at the sidewalls and creates a non-uniformity of the membrane thickness (thicker near the clamping point) that can amount to several microns. As Figure 19 shows, the non uniformity of Si thickness at the bottom of 1 mm large membrane [9] is important. The Si thickness increases from 10 μm at the membrane outskirts to zero in the membrane centre, where the underlying SiO_2 layer is clearly visible. This difficulty in removing of Si near the clamping point or in the corners, where the ion bombardment is reduced, is critical issue, even if SOI substrates are used (Figure 20). For presented here $1000 \times 1000 \times 10$ μm bridge the nominal thickness of 10 μm could be achieved but the complete release requires longer etching time and precise wafer inspection. Furthermore, on the wafer level, a depth uniformity of about 3% (±5 μm in 380 μm deep cavities or 10 μm thick membranes) is typical even with well-tuned process. This leads to the quite large disparity of membrane properties and performances across the same wafer. To overcome, at least partially, these limitations, an etch-stop on a buried silicon oxide layer may offer an interesting solution.

The combination of short time isotropic and anisotropic plasma etching of Si using photoresist/SiO_2 mask is demonstrated in Figure 21. These methods are basically used for sharpening of AFM tips, micro-needles arrays or for surface micromachining dry release.

3.8. Integration of PZT films on SOI and polysilicon substrates

Silicon-on-Insulator (SOI) or polysilicon coated SiO_2/Si substrates can be used to improve the uniformity of the structure thickness on the wafer scale. These two substrates use mono- or polycrystalline silicon layer deposited on insulating and amorphous SiO_2 thin film; the latter acts as an etch-stop during the bulk silicon micromachining (DRIE) or can be used as sacrificial layer for surface micromachining.

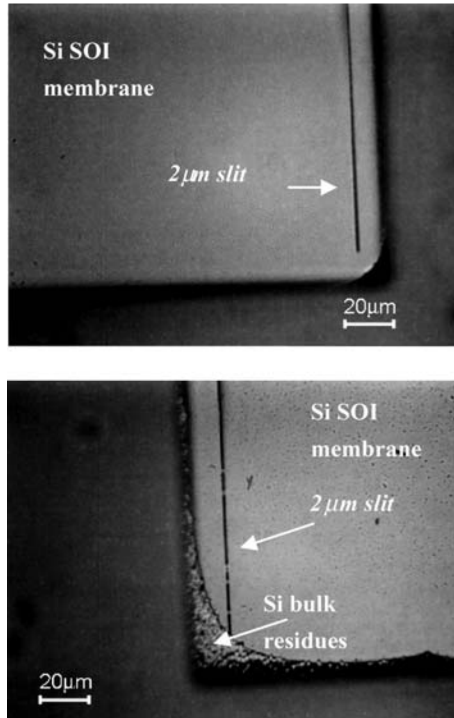


Fig. 20. Uniformly etched Si 5 μm thick SOI membrane (backside view).

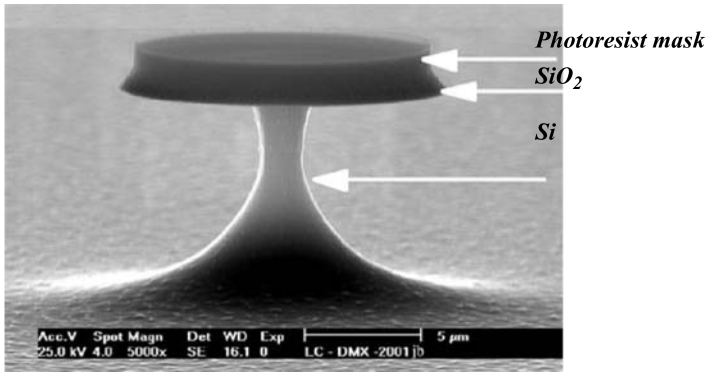


Fig. 21. SEM view of feature obtained by combined anisotropic and isotropic DRIE of silicon.

In SOI wafers, the device silicon thickness (top silicon layer) is usually ranging from 0.2 μm to several hundreds of microns and the deposition of PZT films and process flow do not differ from processing on classical silicon substrates. Figure 22 illustrates example of so fabricated PZT/SOI 5 μm thick membrane surrounded by the 20 × 4 μm grooves [9]. When using thick polysilicon layer (up to 4 microns typically), additional processing steps are required as the roughness of the film is high (∼300 nm RMS)

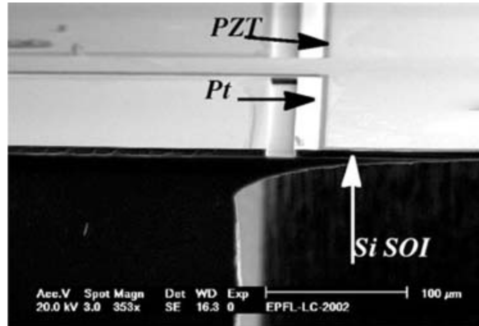


Fig. 22. SEM view of grooved membrane near the clamping point (2 μm PZT on 5 μm SOI substrate) [9].

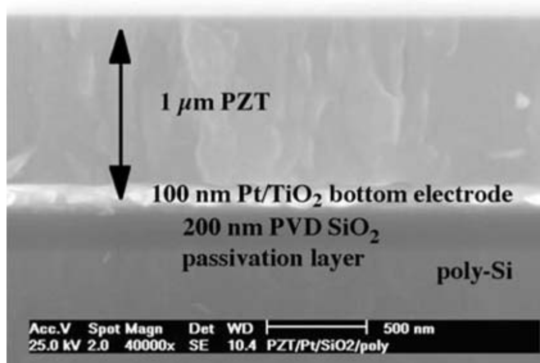


Fig. 23. SEM images cross-section of 1 μm PZT 53/47 {100}-textured thin film deposited on CMP-polished 4 μm poly-silicon layer.

after deposition by LPCVD. This roughness introduces random crystallization of PZT. To recover the surface state of polished silicon wafer, Chemical-Mechanical-Polishing (CMP) [62] of polysilicon has been used and 200 nm SiO_2 passivation layer have been then deposited by PVD.

Figure 23 shows SEM image of the cross section of 1 μm PZT 53/47 {100}-textured deposited on $PbTiO_3/Pt/TiO_2/SiO_2$/poly-Si/SiO_2/Si substrate. No cracks and no delaminating have been observed showing the excellent stability of the PVD SiO_2/poly-silicon structure during the processing of PZT and excellent functional properties have been also obtained: $e_{31,f} = -11$ C/m^2, $\varepsilon = 1000$, $\tan\delta = 0.05$. Integration of PZT thin films on polysilicon substrate has been demonstrated and offers a valuable alternative to SOI wafers.

3.9. Surface Micromachining for pMEMS

Bulk micromachining means that 3-D features are etched into the bulk of crystalline and noncrystalline materials. In contrast, surface micromachined features are built up, layer by layer, on the surface of the substrate (e.g. a single crystal silicon wafer). Dry

etching defines the surface features in the x, y plane and wet etching releases them from the plane by undercutting. The overview of traditional processes, materials and developed devices can be found in literature (e.g. [5], [7] for overview).

Recently, the surface micromachining has been used for fabrication of capacitive Micromachined Ultrasonic Transducers (cMUTs) [63], [64]. The feasibility of surface micromachining of Al/AlN/Pt TFBARs has been demonstrated by using PSG as sacrificial layer and Silox as removal agent.

However, there are still a lot of limitations concerning the compatibility of processes used for etching of the sacrificial layers with piezoelectric stack. Percin [65] has demonstrated the fabrication of piezoelectric (ZnO) ultrasonic transducer arrays by using the surface micromachining with low temperature oxide (LTO) as sacrificial layer. An interesting alternative to wet etching methods can be the new silicon sacrificial layer dry etching (SSLDE) for free-standing RF MEMS architectures [66]. This technique uses sputtered amorphous or LPCVD polycrystalline silicon as sacrificial layers and a dry fluorine-based (SF_6) plasma chemistry as releasing process. The process is capable of various applications in surface micromachining process, and can be applied in fabricating RF MEMS switches, tunable capacitors, high-Q suspended inductors and suspended-gate MOSFETs. It has been demonstrated that the SSLDE process can release metal suspended beams and membranes with excellent performance in terms of etch rate (up to 15 μm/min), Si:SiO_2 selectivity and is fully compatible with standard MEMS processing equipment and CMOS post-processing.

4. Examples of Fabricated Piezoelectric MEMS

4.1. Clamped-free and clamped-clamped cantilevers

Arrays of clamped-free micro cantilevers (10 to 100 μm in width, 50 to 1000 μm in length, nominal thicknesses of 5 and 10 microns) were fabricated using PZT on SOI processing (Figure 24). Clamped-clamped cantilevers with 2 micron of PZT built on 50 microns SOI were fabricated with different configuration of electrodes for simultaneous actuation and sensing (Figure 26). Electro-mechanical properties of piezoelectric micro cantilevers have been studied at the resonance in air and in vacuum (Figure 25) and under quasistatic excitations. FEM simulations have shown excellent agreements with respect to measured resonance frequencies and coupling factor (about few %) [67]. Whatever the geometry used (test samples on thick Si or micro cantilevers), highly reproducible $e_{31,f}$ values of -10 to -12 C/m^2 have been obtained with PZT 53/47 {100}-textured thin films [68]. Perfect accordance between the theoretical (calculated) and measured resonance frequency, as well very good uniphormity have been obtained for clamped-clamped cantilever. For the first resonance mode at 13.8 kHz, the deviation is lower than 1% (Figure 26).

4.2. Piezoelectric Ultrasonic Transducers (pMUTs)

The fabrication of piezoelectric micromachined ultrasonic transducers (pMUTs) with SOI wafers makes possible the formation of thin (2 to 50 μm) and uniform silicon diaphragm as well for single devices, 1D and 2D arrays. Suspended membranes down

Fig. 24. Array of PZT/SOI microcantilevers. Backside view before the final release—etching of the buried SiO_2.

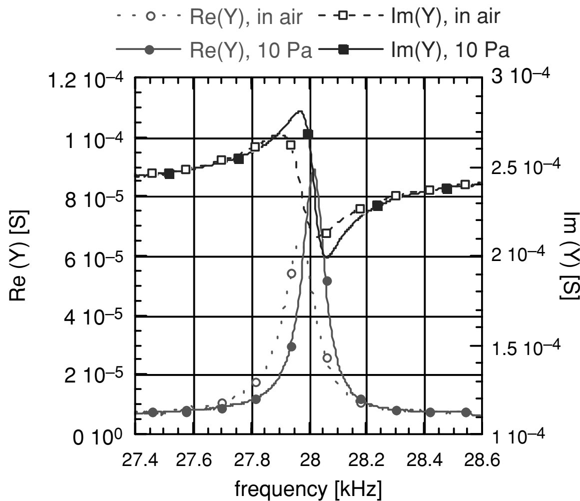


Fig. 25. Admittance curves of 1 mm × 100 μm large and 12 μm thick cantilever measured at atmospheric pressure and at 10 Pa.

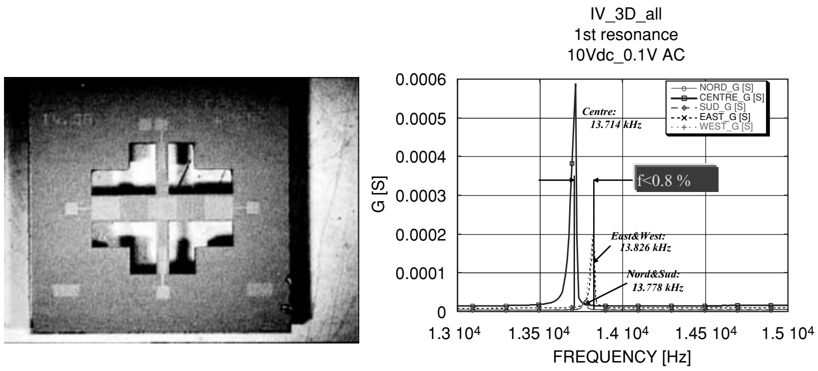


Fig. 26. Example of clamped-clamped cantilevers with multielectrode acting-sensing system. Admittance curves of 50 μm thick cantilever.

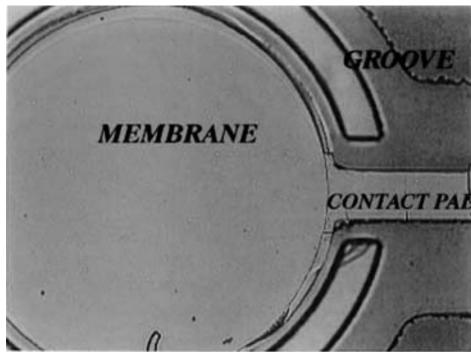


Fig. 27. Top view of 300 μm suspended membrane operating at 750 kHz [9].

Fig. 28. SEM close-view of bridge and membrane of MUT operating at 100 kHz (2 μm PZT on 20 μm Si) [10].

to 300 μm pitch have been fabricated to achieve resonance frequencies in the 0.05 to 1 MHz range (Figure 27 and Figure 28). Values of the coupling factors k^2 as high as 6% have been measured with dc bias larger than 75 kV/cm for 300 μm large membrane at 750 kHz [9].

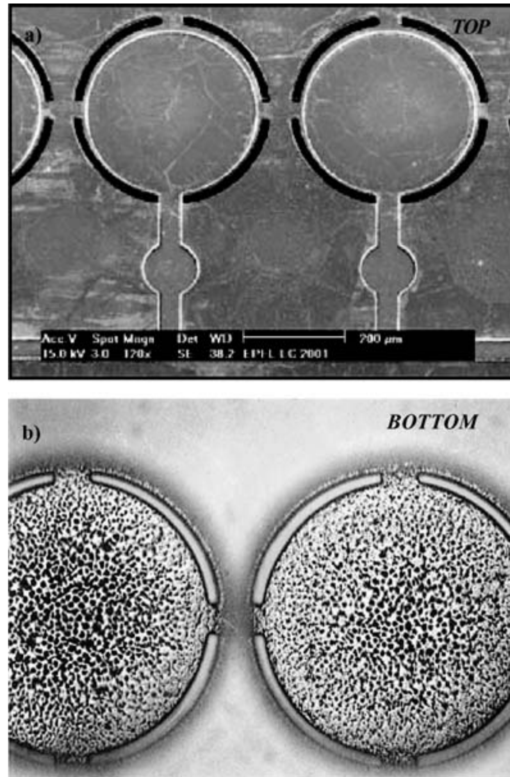


Fig. 29. Frontside and backside view of 450 micron pitch 1D array operating at 950 kHz (fully suspended membrane).

For applications as 1D (Figure 29a [9]) or 2D arrays it is crucial to have all the frequencies in a narrow range. Ideally, the scattering of frequencies should not be larger than the peak width of the resonances enabling the tuning. For the devices with the same geometry and boundary conditions the resonance frequency is defined by the thickness of Si membrane. Thus, the distribution of resonance frequencies is determined by the uniformity of etching of membranes (Figure 29 b). This was almost met with fabricated pMUT arrays. Figure 30 gives the frequency scattering within a 16 element linear array showing deviations within $+/-2.5$ %.

4.3. Pressure sensor and microphone

Piezoelectric cantilever and bridge acoustic sensors have been fabricated using the micromachining processes presented above. Two types of devices have been fabricated: cantilever and bridge structures (Figure 31 and 33). The thickness of membrane was 10 micron ($+/-2$ microns when standard Si substrate is used). To address the air leakage at low frequency, very narrow slits (3–5 µm) with very smooth and residue free sidewalls have been patterned around the structures through Pt/SiO_2/Si (Figure 32,

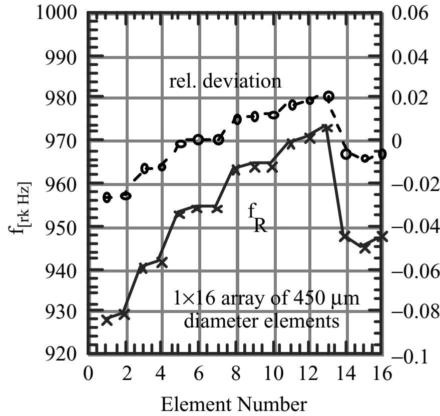


Fig. 30. Resonance frequency distribution of the 16 elements of a 1x16 array (450 μm diameter) measured in air.

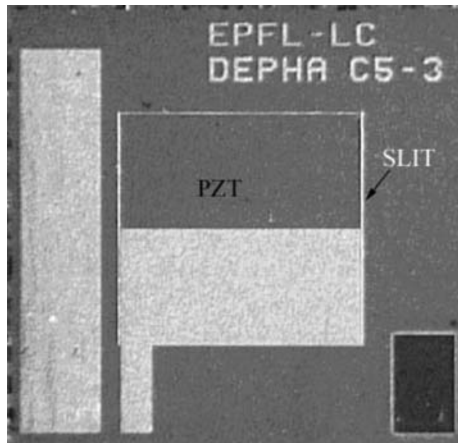


Fig. 31. Cantilever acoustic sensor, 1 micron of PZT, slit 5 μm [10].

34 [10]). It was thus possible to take advantage of the high sensitivity of cantilever structures to design acoustic sensors working at low frequencies (10 to 30 Hz). It has been found also that the slit conductance depends on many experimental factors such as its exact geometry, the surface roughness within of the walls or the presence of microfabrication residues. The integration of PZT/Si cantilever microphone into the photoacoustic gas detector has been demonstrated. Concentration of CO_2 down to 330 ppm (air) has been detected using miniaturized photoacoustic gas detector.

Recently, the acoustic sensor has been fabricated using sputtered Pt/AlN/Pt/Ti stack on thin SOI membranes (5 and 10 micron thick). Stress gradient compensation has been obtained for 2 micron thick AlN deposited on $1000 \times 1000 \times 10$ μm SOI membrane. For thinner, 5 μm thick SOI membranes the distribution of tensile and compressive stresses is not uniform, inducing strong deflection and buckling of structures.

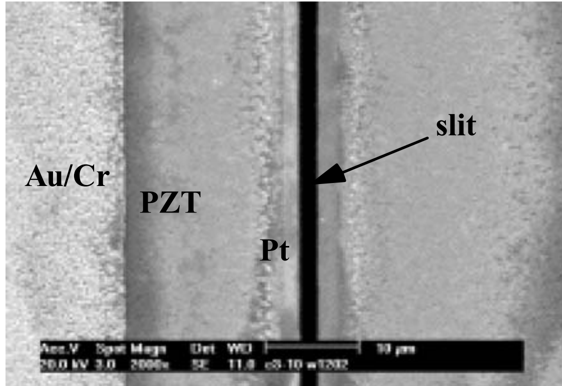


Fig. 32. SEM top view image of a patterned PZT/Pt/SiO_2/Si. Slit width = 2 μm [9,10].

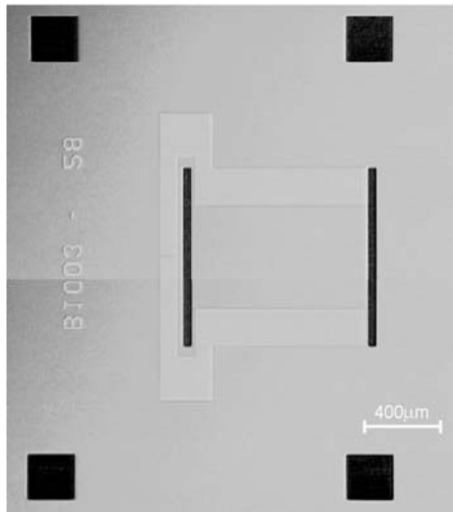


Fig. 33. Bridge acoustic sensor, based on 1.5 micron of AlN with surrounding slit of 1,2 or 3 μm.

The acoustical characterization reveals the sensitivities of 40 to 70 μV/Pa for frequencies from 10Hz to 200Hz (the targeted range of application). The 10 μm deep and 2 μm wide slits (Figure 34), guaranties low air conductance and high sensitivity. All the process steps were conducted under 400 °C guarantying the post-CMOS compatibility.

4.4. RF Switches

MEMS switch have demonstrated useful performance at microwave frequencies using cantilever, rotary and membrane structures, because of their low insertion loss, high isolation, and ultra high linearity [69]. In general terms, cantilevered and multiple-supported surface micromachined electrostatic switches or relays are by far the most

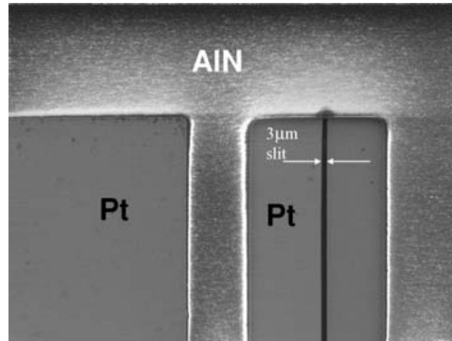


Fig. 34. SEM top view of patterned $AlN/Pt/SiO_2/Si$. Slit width = 3 μm.

widely studied devices to date. The need for low actuation voltage in MEMS switches (<15 V) has often caused excessive design and fabrication complexity as well as increase in the size of the device. The possible solution is to use the piezoelectric actuation for contact or shunt switches. There are two examples of recently developed switches using a piezoelectric actuation:

- capacitive switch developed by LG [70]; it uses a 4-arms piezoelectrically (PZT) activated movable membrane (LPCVD low stress SiN); in this configuration the required operating voltage is only 5 V,
- metal contact switches—one example uses the piezoelectric PZT actuation and is still under development at Penn State University [71]. A PZT unimorph cantilever actuator, fabricated on a sacrificial polysilicon layer and released using a xenon di-fluoride dry etch, was used to realize the switch. The PZT thin film was poled and driven with interdigitated electrodes to exploit the d_{33} coefficient for switching actuation. The actuation voltage is about 40 V for 1 micron deflection. Accelerometer using the same type of actuation/detection (IDT and d_{33} mode) has been developed recently by the same group [72].

4.5. Other devices (non mechanical-devices)

4.5.1. FeRams

High density—low power memories, which are to be used in RF-ID cards, still represent a challenge for the semiconductor industry. The integration of ferroelectric thin films in CMOS technology represents one of the most important steps for the realization of such memories. We have investigated the complete integration of ferroelectric thin films (PZT) on W-plug in a standard 0.5 μm CMOS technology [73]. A special process flow compatible between ferroelectrics and CMOS integrations has been designed. Sputtered $IrO_2/Ir/TiN$ electrode has been used as well as barrier and seeding layer for growth of textured PZT. As barrier layer, it protects the W-plugs contacts against oxidation during the PZT deposition process up to 650 °C. Another important task was to observe the impact of patterning process (plasma etching in ECR/RF RIBE) on properties of ferroelectric capacitors. As shown in Figure 11, no alteration of ferroelectric properties has been measured [74].

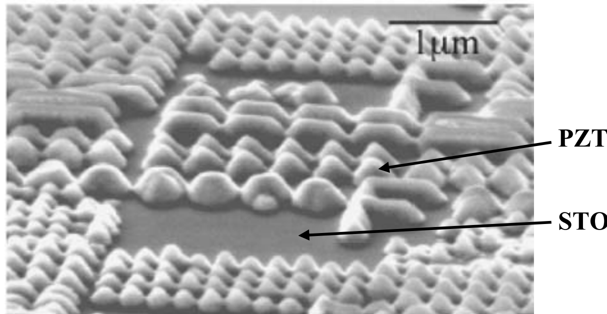


Fig. 35. SEM view of nanopatterned PZT features on STO [74].

4.6. Nanopatterning of PZT

Downscaling is an important step to achieve very high-density memories. Bühlmann et al., [75] have reported on nanopatterning of an epitaxial 200 nm thick film of $Pb(Zr_{0.40}Ti_{0.60})O_3$ (PZT) grown on conductive Nb-doped $SrTiO_3$ (100). Patterning of PZT has been done by e-beam lithography using PMMA (poly-methylmethacrylate) resist, Cr as hard and sacrificial mask and ECR/RF RIBE etching. For lithography, a 150 nm thick PMMA film was deposited. Patterns with lateral dimension between 50 and 200 nm were written by an e-beam. After the development, noncontact atomic force microscopy scans on the PMMA showed that holes down to 50 nm were obtained. A 75 nm thin Cr masking layer was evaporated onto the developed PMMA and the lift off was performed in acetone. Scanning electron microscopy observations on the Cr patterns showed that the patterning worked for all features with lateral dimensions larger than 50 nm. The PZT film and Cr sacrificial mask were then etched in a dual frequency ECR/RF reactor using a CF_4, CCl_4 and Are gas mixture at a low pressure of 10 mPa. This process assures a good balance between chemical and physical etching. Ion energies have been kept small. A small rf self-bias of only 25 V was applied to the substrate. The ions leaving the ECR ion gun had energies in the range of 200 to 300 eV at maximum.

The etching rate was found to be 10 nm/min for PZT and 3 nm/min for Cr. The remaining Cr was removed in an aqueous solution of ceric ammonium nitrate and perchloric acid. In contrast to Ar ion milling [76], this etching process did not leave any redeposited PZT. The dry etching process leads to rounded PZT patterns caused by a continuous reduction of the thinner border of the Cr-mask (Figure 35). The smallest items achieved had a lateral dimension of 100 nm. Piezoelectric sensitive scanning force microscopy in the contact mode revealed a strong increase of the piezoelectric response for feature sizes with lateral dimensions below 200 nm.

4.7. Local growth and crystallization of piezoelectric films

Piezoelectric and pyroelectric films of perovskite materials need high processing temperatures of more than 600 °C. This may damage the rest of the device and is especially critical for monolithic integration together with the read-out or driving circuit.

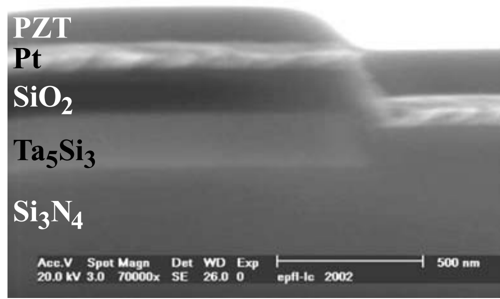


Fig. 36. SEM cross section view of pyrolized PZT grown locally on TaSi microhotplate [76].

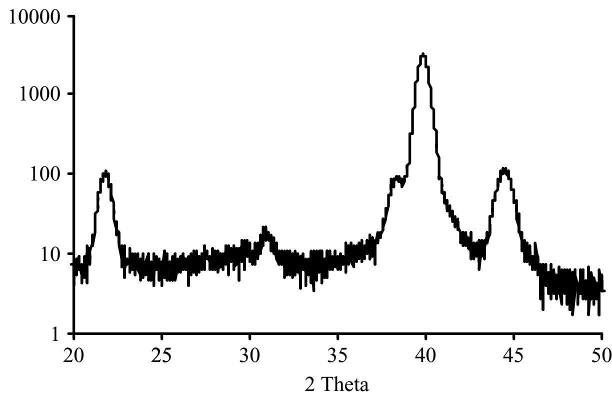


Fig. 37. XRD spectra showing the (100), (110), (111) and (200) orientation of PZT grown on the TaSi/SiN microhotplate.

In our studies, PZT ($PbZr_xTi_{1-x}O_3$) thin films have been locally grown by means of sol-gel deposition and local anneals on micro hotplate integrated in the substrate [77]. The micro hotplate was based on a tantalum silicide filament (Ta_5Si_3 [78]) formed on stress compensated SiN/SiO_2 membrane. On this filament, a passivation layer of SiO_2, a layer of Ti/TiO_2 and a bottom electrode of Pt were deposited by sputtering. After deposition of PZT sol-gel solution, the film is pyrolised and crystallized by applying the electrical power to the hot-plate (Figure 36). Due to the low heat conductivity of the membrane, crystallization of the PZT film occurs exactly ($+/-1$ μm) on the resistor filament. The formation of crystalline, i.e. perovskite PZT was verified by means of X-ray diffraction (Figure 37). A random PZT texture has been observed.

5. Final Remarks

In this chapter, critical issues for microfabrication of piezoelectric MEMS have been discussed. To overcome resolution problems in complex device structures, wet etching of PZT, AlN films and platinum bottom electrodes have been replaced by high density

plasma dry etching methods. Micron scale patterns have been obtained using high density plasma (HDP ICP) or reactive ion beam etching (ECR/RF RIBE) processes. The developed processes exhibited reasonable etching rates and better results in term of anisotropy, photoresist stability and residues.

These new processes have been successfully integrated into a standard microfabrication sequence that fully preserves the functionality of piezoelectric thin films. For example for PZT based devices, at the end of the micromachining sequence, transverse piezoelectric coefficient $e_{31,f}$ of -12 C/m^2, dielectric permittivity ε of 1100 and loss factor $\tan\delta$ of 0.03 (at 1 kHz) have been measured on test samples with 1 μm PZT 53/47 $\{100\}$-textured thin film.

In-plane laminated PZT/Si and AlN/Si structures have been obtained by compensating the tensile stress of electrodes and piezoelectric films with compressive SiO_2 thermal oxide.

Finally, the surface micromachining for integration of PZT or AlN thin films on thin suspended membranes is under development. In this case SOI/SiO_2 or polysilicon/amorphous Si as combination of structural/sacrificial layers are widely investigated.

Several examples of piezoelectric devices (ultrasonic transducers, acoustic sensor, damping control, RF switches) presented in this paper have been developed during the last years. It has been demonstrated that the microfabrication of piezoelectric MEMS based on PZT or AlN thin films is the versatile and reliable technology. Most of the developments are based on PZT sol-gel textured films, however some efforts have been done for integration of AlN for piezoelectric MEMS. In this context, the main advantage of AlN is the low thermal budget processing and the possibility of post-CMOS above-IC integration.

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