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60 GHz Common-Gate Single-Stage Current Reuse Cascode LNA Topology for High-Data-Rate Applications

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In the design of complementary metal oxide semiconductor (CMOS) radio-frequency (RF) components, power dissipation and speed are the two important and conflicting factors which lay stringent requirements on RF design. In this work, a low-noise amplifier (LNA) is designed by using common-gate (CG–CG) current reuse topology and a cascode amplifier with current mirror feedback. The CG–CG low-noise amplifier with current reuse topology attains maximum forward gain of 11 dB and minimum noise figure of 3.2 dB at the desired 60 GHz using 90-nm CMOS virtuoso cadence technique. The designed LNA gives both input and output matching < -10 dB at 60 GHz and a power dissipation of 7.5 mW.

Key words: CG, CMOS, current reuse, LNA

INTRODUCTION

Wireless communication systems play an important role today in everyone's lives. The data rates of these wireless systems vary from a few kilobits per second (kbps) to gigabits per second (Gbps), and the distance of communication supported by these technologies varies from a few meters to kilometers. To meet the ever-rising demand for high data rates, wireless technologies are entering the millimeter-wave technology domain, which supports transmission data rates up to Gbps over small distances. Gbps transmission involves the transfer of huge data between different devices such as high-definition (HD) video cameras, smartphones, HD set-top boxes, HD[1] DVD players and high-definition printers. To achieve Gbps transmission, the operating frequency should be several tens of GHz to hundreds of GHz.

A low-noise amplifier (LNA) is one of the key components of radio-frequency (RF) receivers. The designed LNA must meet several specifications such as high power gain, reduced noise figure, wideband input matching and increased linearity. Reduced power dissipation and small die area are also important requirements in design. The most popular topologies used for LNA design at 60 GHz are transformer feedback, cascode (CAS) and current reuse. In transformer feedback[2] topology, reduced input matching increases power dissipation and enlarges the chip area. However, the power dissipation can be addressed by using current reuse for transformer feedback topology, but it suffers from matching and large chip area. Current reuse topology[3,4] requires a high supply voltage and the addition of one on-chip inductor depending on the architecture used, which leads to additional chip area. The main objective of this work is to design current reuse CG–CG LNA architecture in a 90-nm Cadence virtuoso simulator. The common-gate LNA enhances the noise figure and reverse isolation with the expense of gain. The common-source (CS) LNA enhances forward gain at the cost of noise figure. The proposed LNA combines the advantages of both architectures.

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PROPOSED METHODOLOGY FOR CG–CG CURRENT REUSE LNA TOPOLOGY

The circuit diagram of the proposed CG–CG LNA is depicted in Fig. 1. The proposed design uses a common-gate current reuse[3,5] topology. A common-gate topology[4,5] is adopted for design as it can produce wideband input matching, high reverse isolation, and it is more linear compared to other configurations. The main issue associated with CG topology is that it suffers from reduced power gain. In the proposed design, the power gain issue is addressed by using a current reuse (pseudo-CS) circuit in the second stage. The modification may be achieved by connecting a bypass capacitor at the source of the second stage. Connecting a bypass capacitor at the source in turn depicts a source connected to an ac ground. At the same time, the signal out of the first stage is coupled to the gate of the second stage by pseudo-CS topology. Pseudo-CS topology is achieved at the desired frequency by creating a minimum impedance path between the drain of M1 and the gate of M2 and a high impedance path between the drain of M1 and source of M2. The reduced forward gain of CG architecture is compensated by the use of CS topology in the second stage. The use of current reuse topology reduces the power dissipation by using the same

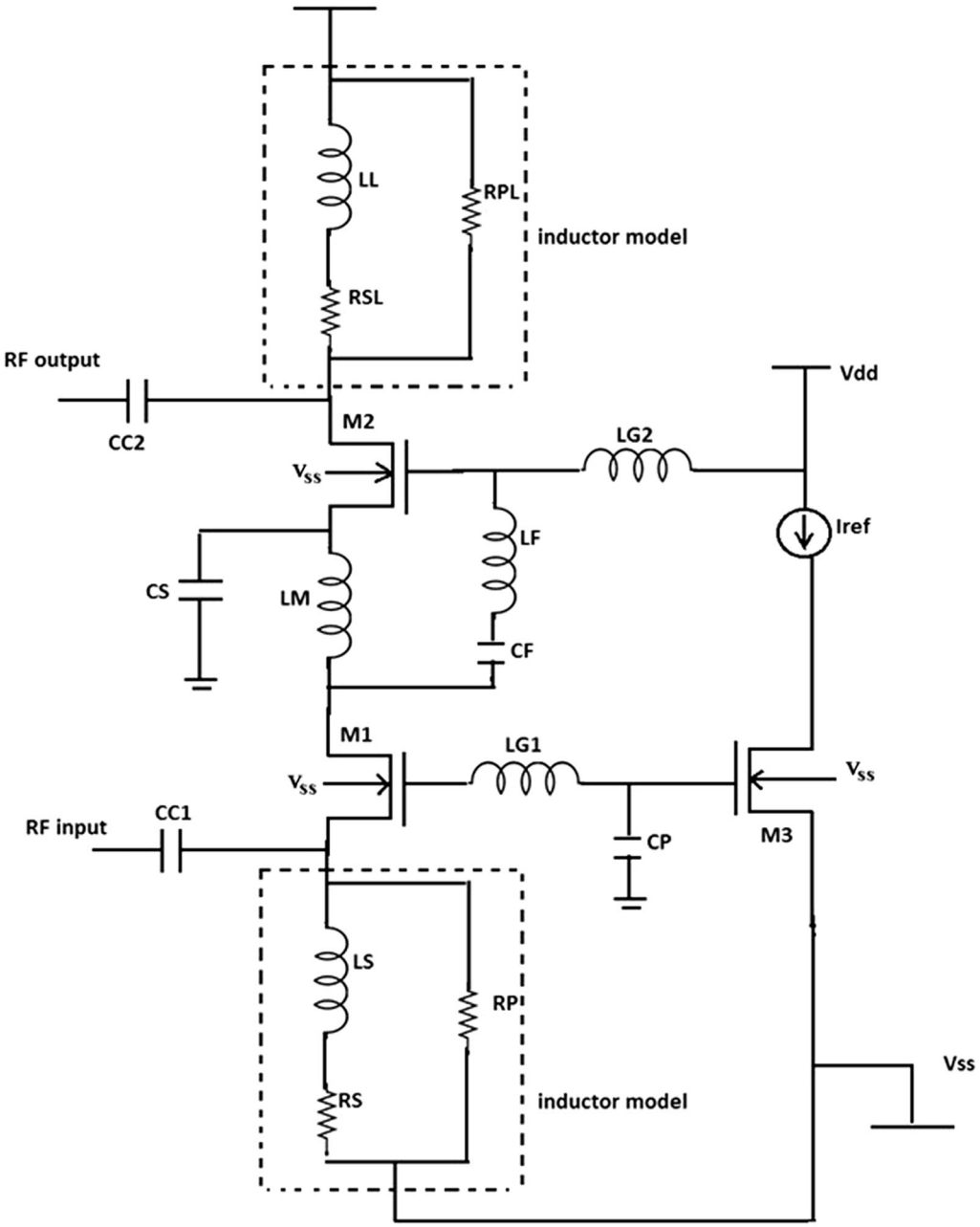

Fig. 1. Proposed CG–CG current reuse topology.

bias current as that of M1. The use of pseudo-CS topology increases the forward power gain.

To match input impedance of 50 Ω in common-gate topology, g_m of the first stage is selected as 20 mA/V. Power gain, input matching bandwidth, noise figure and power of the design need to be traded with g_m. For a g_m of 20 mA/V, the input matching is done by sacrificing power gain. As g_m is increased, power gain can be enhanced at the expense of matching and increased power consumption. In order to select the traded g_m for the design, the plots of transconductance g_m and unity gain frequency f_t of an N-channel metal oxide semiconductor transistor for a given width W_o as a function of drain current I_d are considered. These simulation plots are depicted in Figs. 2 and 3. To avoid higher power consumption, drain current is selected as 80–90% of saturated g_m.[2] The selected drain current is optimum in terms of speed and power consumption.

From the simulation results, g_m is selected as 27 mA/V with a transition frequency of 110 GHz for a reference current of 5 mA[6,7] and gate width of 25 μm. This metal–oxide–semiconductor field-effect transistor (MOSFET) characterization yields dc power dissipation of 12 mW. From Figs. 4 and 5, to attain the designed bias current of 5 mA, biasing voltages are selected as V_{gs} = 600 mV and V_{ds} = 1.25 V. From Fig. 6, the effective gate capacitance[8] is taken as (40 fF + 30 fF), where 40 fF is the approximate gate-source capacitance and 30 fF is the pad capacitance at the gate terminal. With this effective capacitance, the inductor L_s is designed to be 100 pH at the desired frequency. The second CS stage uses a simple series peaking technique[9] to bias transistor M_2. The components in the second stage are transistor M_2, load inductance L_L and resistance R_l. The purpose of the second stage is to enhance the power gain at the desired frequency band. To achieve maximum gain, the width of the second stage M_2 is selected[6] as 30 μm which is the maximum permitted width in the selected technology. For the designed width M_2 of the MOS, the effective drain capacitance is approximately 20 fF, extracted from Fig. 7. Therefore, inductance of 300 pH is selected at the load to nullify the parasitic capacitance at the drain. The loss of the inductor is represented by a series resistance R_{sl}. When an

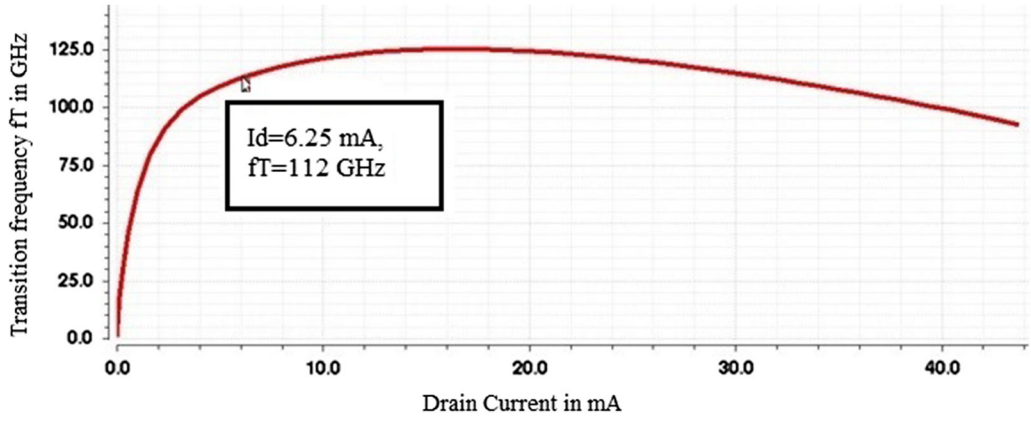

Fig. 2. Transition frequency as a function of I_d.

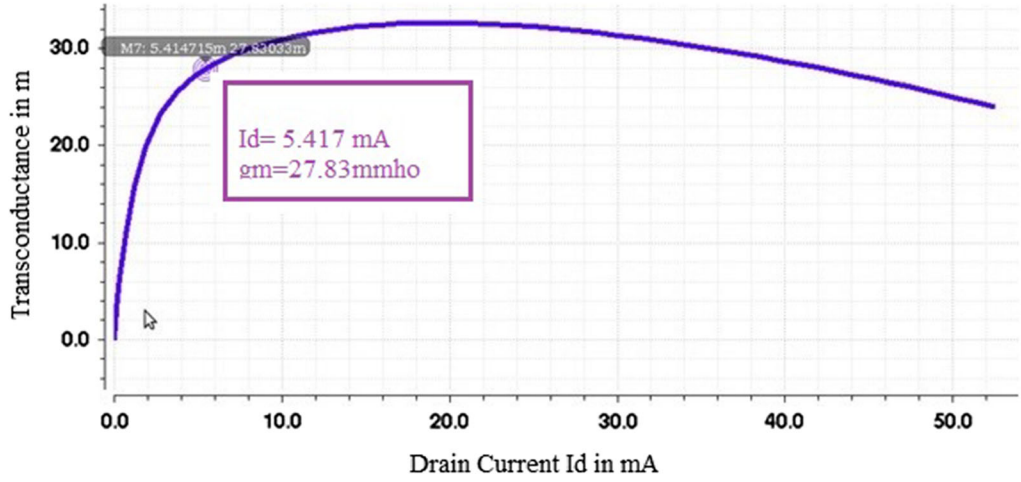

Fig. 3. g_m as a function of I_d.

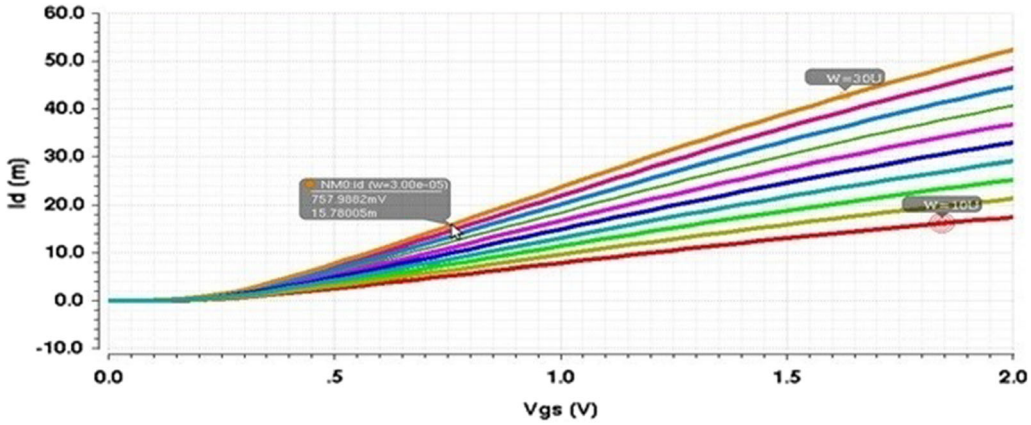

Fig. 4. I_d–V_{gs} characteristics.

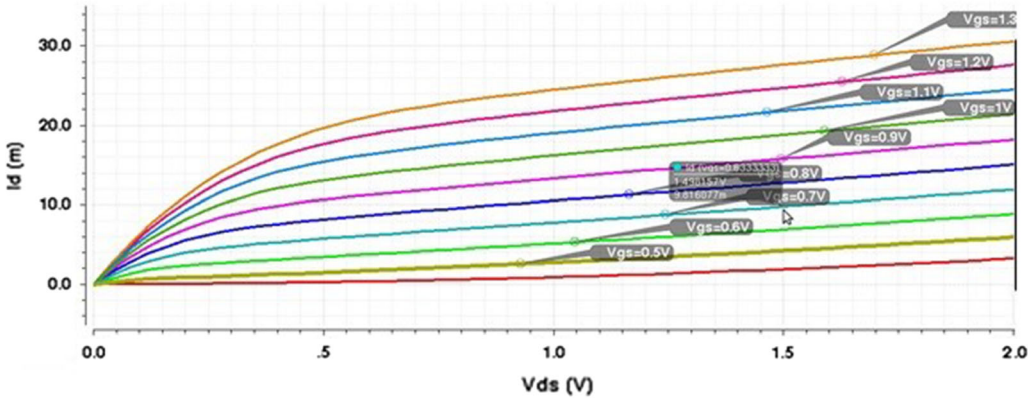

Fig. 5. I_d–V_{ds} characteristics.

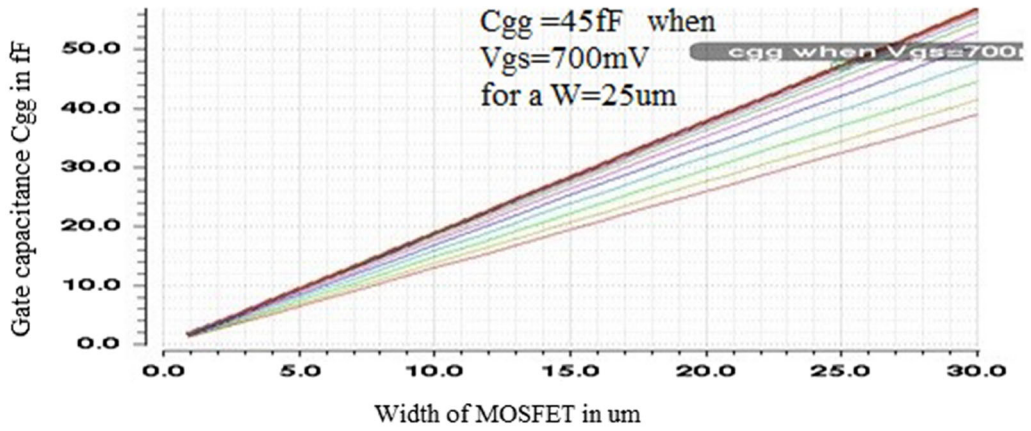

Fig. 6. C_{gg} as a function of W.

inductor L_1 and parasitic capacitance at drain resonates, the effective resistance at the drain should match with the input impedance of the next stage. Inductors L_M and L_F and capacitors C_f and C_s form the current reuse topology to reduce the power dissipation.[10] Here, L_M = 80 pH, L_f = 100 pH and C_f = 380 fF, and finally, the bypass capacitor C_s = 13 fF is selected to achieve high input matching.[3] The variation of input matching as a function of bypass capacitor is depicted in Fig. 8. The graph depicts that the bypass capacitor is inversely proportional to matching.

Input Matching

The analogous circuit of the proposed design is depicted in Fig. 9. The source of M_2 is directly connected to ground because of bypass capacitor C_s. The small-signal equivalent of the proposed design is as shown in Fig. 10.

From the small-signal model depicted in Fig. 10, the various impedances are expressed by Eqs. 1–6.

$$Z_1 = s(L_{G1} + L_S)||\frac{1}{sC_y} \tag{1}$$

$$Z_2 = sL_M||\frac{1}{sC_x} \tag{2}$$

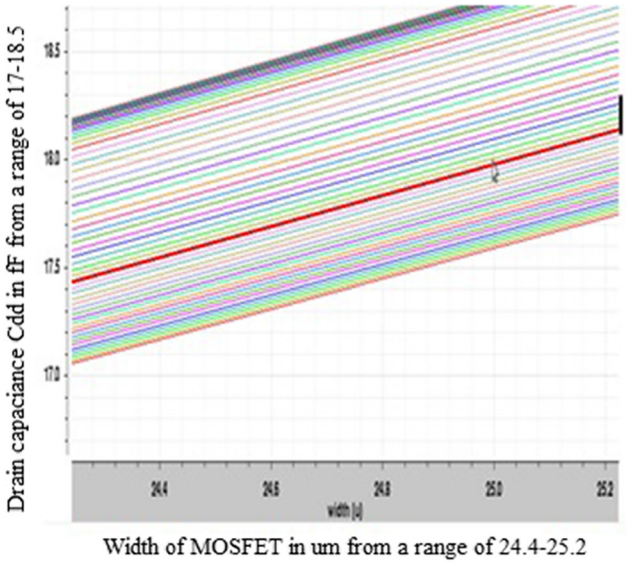

Fig. 7. C_{dd} as a function of W.

$$Z_3 = sL_f + \frac{1}{sC_f} \tag{3}$$

$$Z_4 = sL_{G2}||\frac{1}{sC_z} \tag{4}$$

$$Z_l = (R + sL_l)||\frac{1}{sC_w} \tag{5}$$

$$Z_d = Z_2|||Z_3 + Z_4] \tag{6}$$

where C_w is the effective capacitance at the drain of M_2, C_x is the effective capacitance at the drain of M_1, C_y is the effective capacitance at the source of M_1 and C_Z is the effective capacitance at the gate of M_2.

To find the input impedance of the proposed LNA, the small-signal model of the first stage is redrawn and is depicted in Fig. 11.

From Fig. 12, the input impedance of the LNA is given by:

$$Z_{in} = \frac{1}{SC_Y}||S(L_{G1} + L_S)||Z' \tag{7}$$

By computing the value of Z', the final input impedance is given by Eq. 8.

$$Z_{in} = \frac{1}{SC_Y}||S(L_{G1} + L_S)||\frac{1}{g_{m1}}\left[\frac{Z_D}{r_{ds1}} + 1\right] \tag{8}$$

To achieve input matching at the desired frequency, parasitic capacitance C_Y and effective inductance should resonate. This indicates Z_{in} is

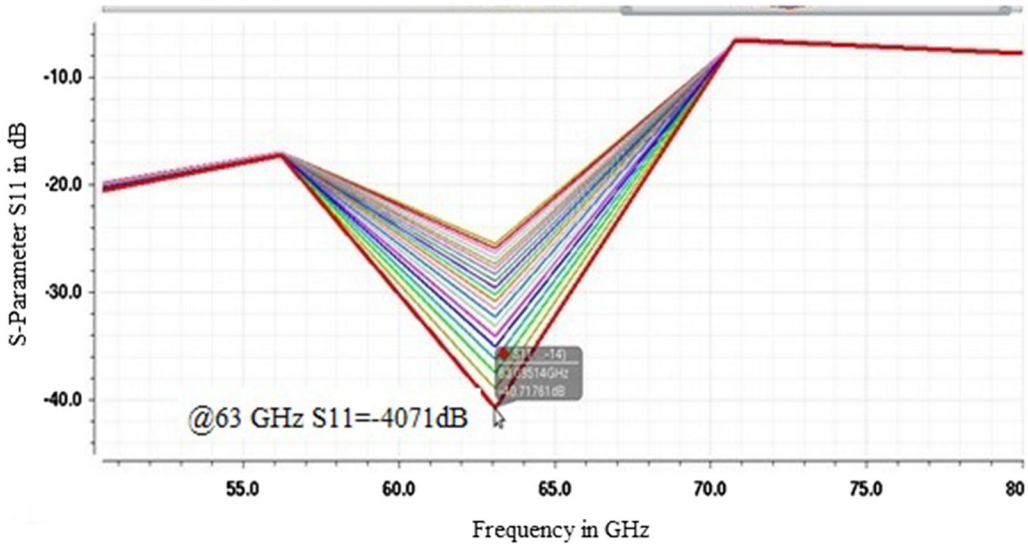

Fig. 8. S_{11} as function of Cs.

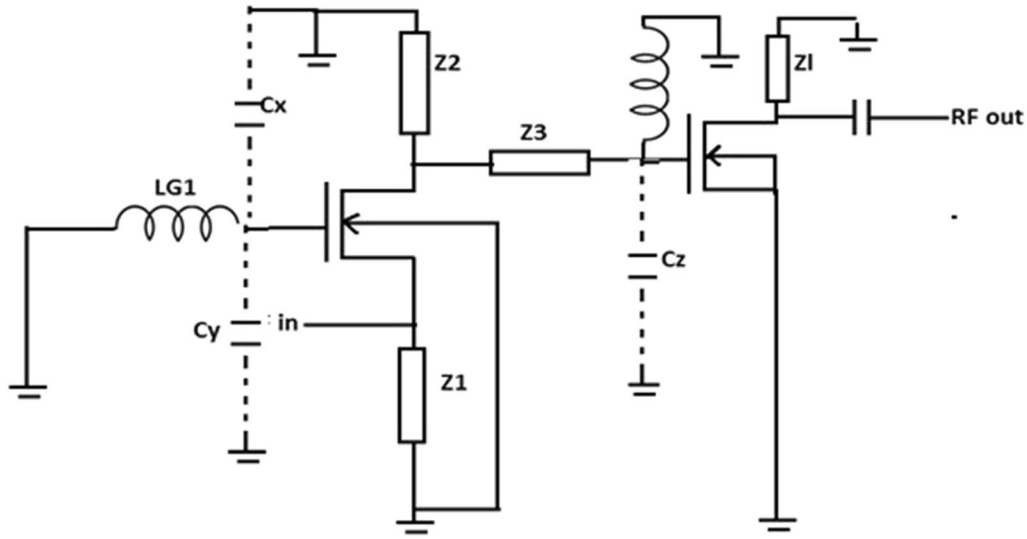

Fig. 9. Equivalent circuit of the proposed design.

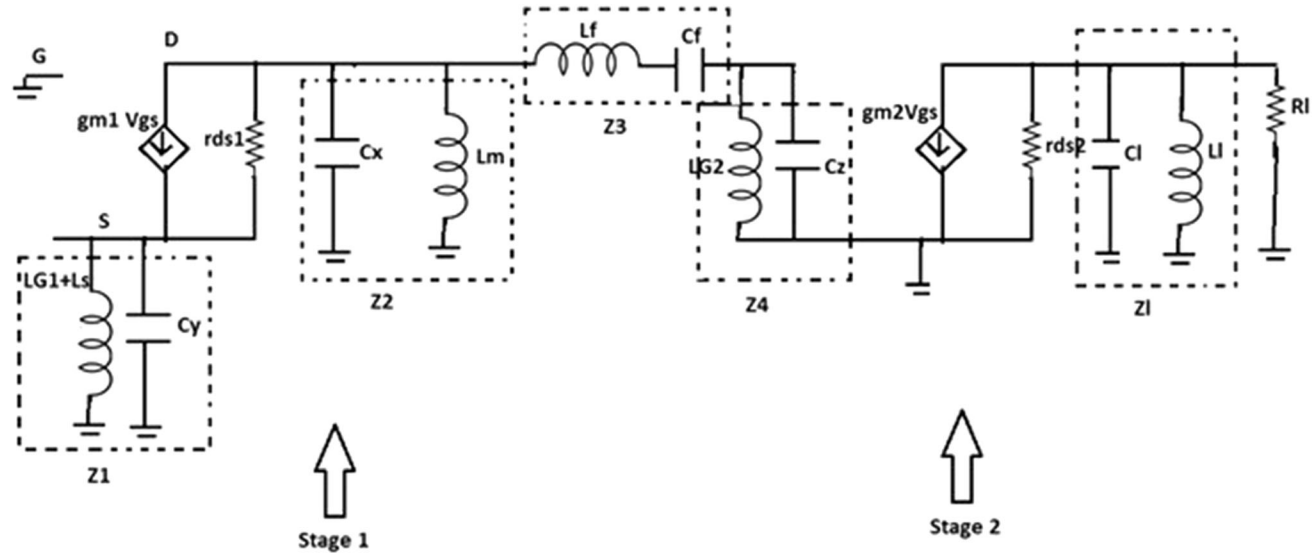

Fig. 10. Small-signal model of the proposed design.

the stronger function of Z_D. Here, g_{m1} and r_{ds1} are the transconductance and output resistance of the first stage, respectively. For the designed values, Z_{in} is nearly 45 Ω.

Output Impedance

Output impedance is given by Eq. 9.

$$Z_{out} = Z_l || r_{ds2} \tag{9}$$

where $Z_l = (R + sL_l) || \frac{1}{sC_w}$

Here, g_{m2} and r_{ds2} are the transconductance and output resistance of the second stage. For proper output matching, r_{ds2} needs to be matched with R_L. For the designed values, output impedance is nearly 70 Ω.

Gain Analysis

The gain analysis[5] of the proposed design is divided into two sections.

Stage I

The input of the first stage is assumed as V_{in}, and the output of the first stage is V_x.

For the first stage, gain is given by Eq. 10:

$$A_{V1} = \frac{V_x}{V_{in}} \tag{10}$$

From Fig. 11, the output voltage V_x of the first stage is given by Eq. 11:

$$\left[-\frac{V_x}{Z_D} - g_{m1}V_{gs}\right] r_{ds1} + \left[-\frac{V_x}{Z_D} Z_1\right] + V_{in} = V_x \tag{11}$$

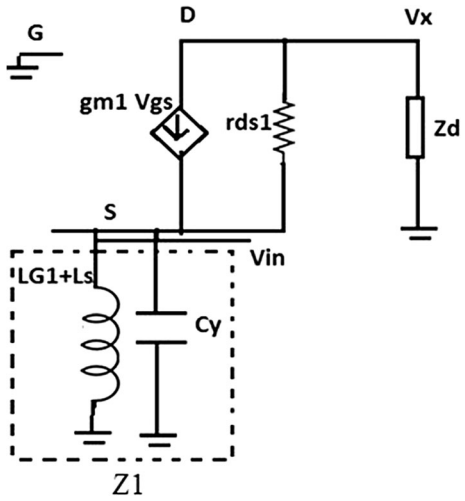

Fig. 11. Small-signal model of stage I.

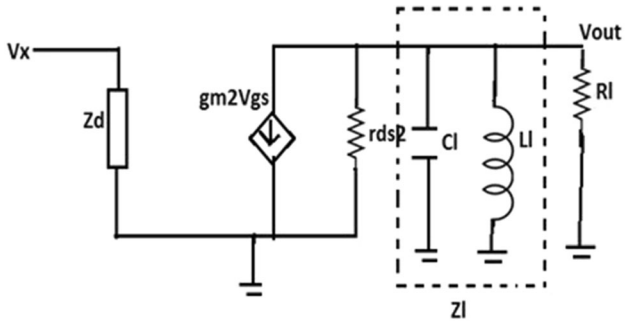

Fig. 12. Small-signal model of the proposed design of stage II.

From Eq. 11, the gate-to-source voltage V_{gs} is given by Eq. 12:

$$V_{gs} = \frac{V_x}{Z_D} Z_1 - V_{in} \tag{12}$$

Substituting Eq. 12 in Eq. 11, Eq. 11 is simplified as in Eq. 13:

$$-\frac{V_x}{Z_D} r_{ds1} - g_{m1} r_{ds1} \frac{V_x}{Z_D} Z_1 + g_{m1} r_{ds1} V_{in} - \frac{V_x}{Z_D} Z_1 + V_{in} = V_x \tag{13}$$

Finally, the gain of the first stage A_{V1} is given by Eq. 14:

$$\frac{V_x}{V_{in}} = \frac{g_{m1} r_{ds1} Z_D}{Z_D + r_{ds1} + Z_1(1 + g_{m1} r_{ds1})} \tag{14}$$

Stage II

The input to the second stage is voltage V_x, and the output of this stage is V_{out}.

The second stage gain is depicted in Eq. 15:

$$A_{V2} = \frac{V_{out}}{V_x} \tag{15}$$

From Fig. 12, the second stage gain is derived and presented in Eq. 16:

$$A_{V2} = \frac{V_{out}}{V_x} = -\frac{g_{m2} Z_{out}}{1 + SC_{cc2}} \tag{16}$$

where

$$Z_{out} = Z_l || r_{ds2}$$

The total gain of the proposed circuit is represented in Eq. 17:

$$A_V = \frac{V_{out}}{V_{in}} = -\frac{g_{m1} r_{ds1} Z_D}{Z_D + r_{ds1} + Z_1(1 + g_{m1} r_{ds1})} \frac{g_{m2} Z_{out}}{(1 + SC_{cc2})} \tag{17}$$

The gains at the output of stage 1 and stage 2 are shown in Fig. 13 which depicts that the design achieves highest gain at the desired frequency. Theoretically, gain is derived as 12 dB.

The G_P, G_A and G as a function of frequency are plotted in Fig. 14. Available power from the source is always larger than power input to the LNA; i.e. ($G_P > G_T$). If G_P and G_T are closer to one another, then input matching will be appreciated. In the same manner, power available from LNA is always larger than power delivered to the load, i.e. $G_A > G_P$. If G_A and G_P are closer to one another, then output matching will be appreciated.

Noise Analysis

The key issue in designing the LNA is to attain minimum noise figure, because it is the front-end component of the receiver chain. In a circuit, the dominant noise components are thermal noise and flicker noise. The thermal noise[3] is contributed by the resistor, MOSFET and parasitic resistors of capacitors and inductors. Flicker noise is considered at low frequency. Since the LNA is designed at 60 GHz, flicker noise is totally disregarded. In thermal noise, the contribution of the resistor and MOSFET noise is dominated by parasitic resistors of capacitors and inductors. Henceforth, noise analysis of the proposed LNA is mainly on resistor noise and MOSFET channel noise. The noise model of the proposed design is shown in Figs. 15 and 16.

The noise factor F is given by Eq. 18.

$$F = \frac{V_{nout}^2}{A_v^2} \frac{1}{V_{ns}^2} \tag{18}$$

where A_v = voltage gain of the amplifier, V_{nout}^2 = noise voltage at the output and V_{ns}^2 = noise voltage at the source.

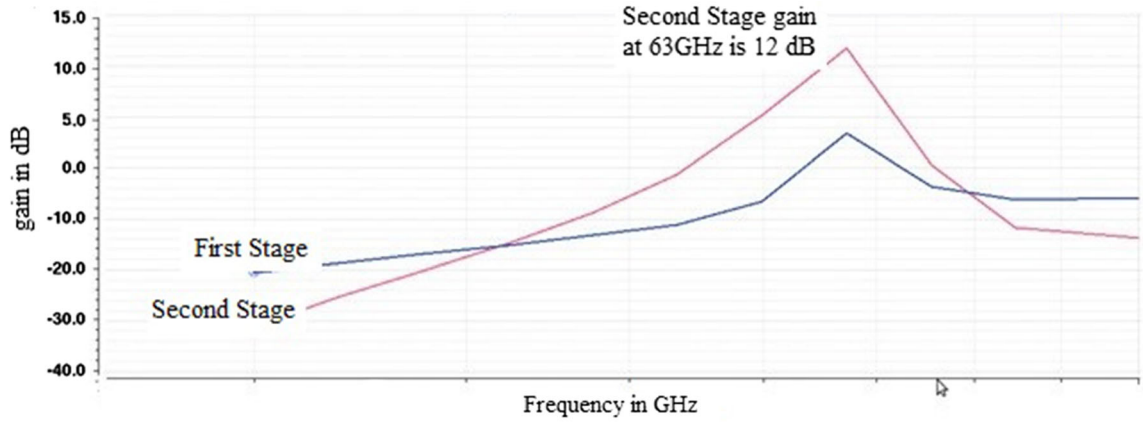

Fig. 13. Gain of stage I and stage II.

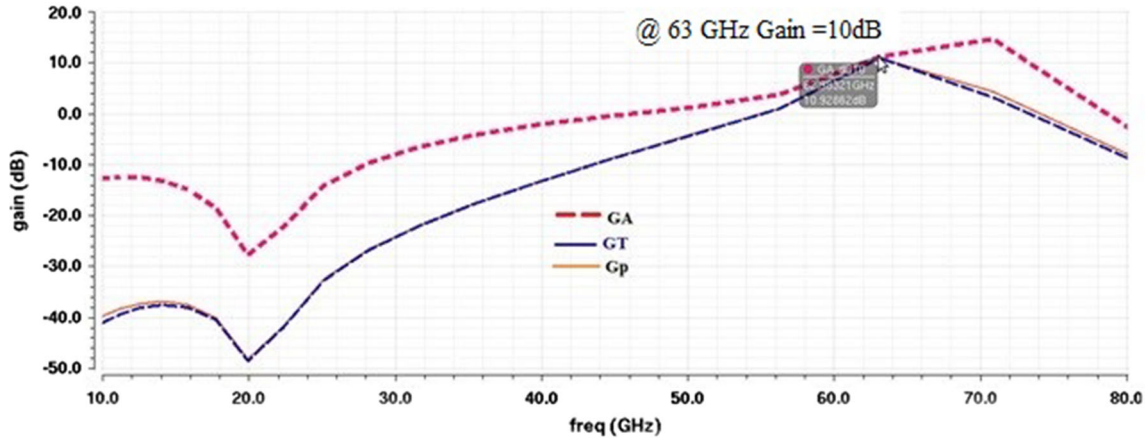

Fig. 14. G_A, G_T and G_P.

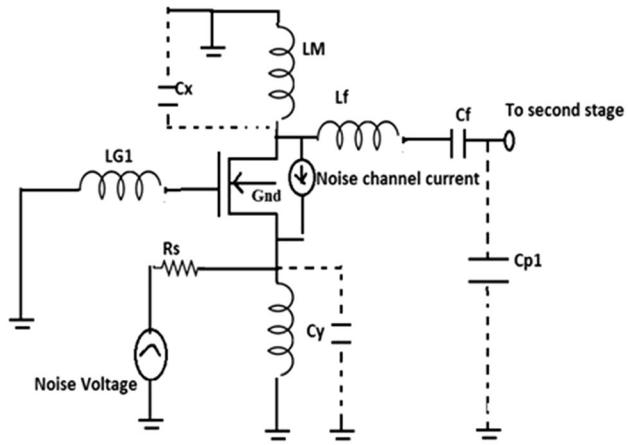

Fig. 15. Noise model of first stage.

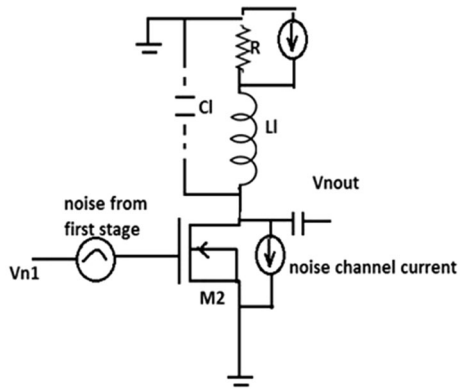

Fig. 16. Noise model of second stage.

If noise factor F is expressed in dB, it is called the noise figure (NF). The noise voltage of the proposed design in shown in Eq. 19:

$$V_{\text{nout}}^2 = A_{\text{V2}}^2 X \left(\left[\frac{g_{\text{m1}} r_{\text{ds1}} Z_{\text{D}}}{Z_{\text{D}} + r_{\text{ds1}} + Z_1(1 + g_{\text{m1}} r_{\text{ds1}})} \right]^2 X \frac{1}{4KTR_{\text{s}}} + \frac{4KT\gamma}{g_{\text{m1}}} \left[\frac{Z_{\text{D}}}{\frac{1}{g_{\text{m1}}} + (Z_1 || R_{\text{S}})} \right]^2 \right) + \frac{4KT\gamma}{g_{\text{m2}}} \left[\frac{Z_{\text{L}}}{\frac{1}{g_{\text{m2}}} + (Z_{\text{D}} || r_{\text{ds1}})} \right]^2 + \frac{V_{\text{n}}^2}{R_1^2} \left[\frac{Z_{\text{L}}}{\frac{1}{g_{\text{m2}}} + (Z_{\text{D}} || r_{\text{ds1}})} \right]^2 \quad (19)$$

RESULTS OF THE PROPOSED CG–CG CURRENT REUSE LNA

The proposed circuit is simulated in Generic Process Design Kit (GPDK) 90-nm CMOS technology using Cadence Virtuoso with an FF (fast–fast) process corner operating at 25°. The various analyses related to the LNA have been carried out, and results are listed as follows.

S-Parameter Analysis

The S-parameter analysis of proposed LNA is shown in Fig. 17. S-parameter analysis of the LNA is carried out to determine S_{11} for input matching, S_{21} forward gain, S_{22} for output matching and S_{12} for reverse isolation. The designed LNA reports a maximum forward gain (S_{21}) of 10.74 dB at 63 GHz. The design has a 3-dB bandwidth of 8 GHz. The design offers maximum matching of −38 dB at a design frequency of 63 GHz. It offers a wideband matching of < -10 dB from 40 GHz to 70 GHz. The design reports a reverse isolation S_{12} of −25 dB at the desired frequency. The measured S_{22} is better than −10 dB, from 55 GHz to 67 GHz.

Noise Figure and NF_{min}

The minimum noise figure (NF_{min}) and noise figure (NF) are plotted as a function of frequency in Fig. 18. At the desired frequency, the minimum noise figure is 2.56 dB and the attained noise figure is 3.2 dB. The minimum noise figure is attained at the cost of input matching. The noise figure is further improved by increasing S_{21}. To increase S_{21}, transconductance needs to be improved. This can be attained at the expense of power dissipation. Figure 19 shows the noise resistance for a range of different frequencies. From Fig. 19, it is clear that noise resistance r_{n} at 63 GHz is 15 Ω.

Figure 20 depicts the noise circle (NC) and NF measurement at the desired frequency. In the designed circuit, the noise circles are drawn from 3 dB to 4 dB at a step size of 0.2 dB at 63 GHz. From the graph it is clear that the NC near the origin[9] is 3.2 dB. The origin or center of the circle is selected as reference point for minimum reflection. The noise figure is reported as 3.2 dB at 63 GHz. The minimum noise figure is reported at 65 GHz as 3.15 dB.

Stability

The stability of the design is calculated by using Eq. 20:

$$K = \frac{1 - |S_{11}^2| - |S_{22}^2| + |\Delta^2|}{2|S_{21}S_{12}|} \quad (20)$$

If $K > 1$ at the desired frequency, the system is stable,

where $\Delta = S_{11}S_{22} - S_{21}S_{12}$

For a stable network, $\Delta < 1$. Figure 21 shows the stability K for different frequencies. At the desired frequency, K = 2.77, which indicates the stability of the system. At 63 GHz, the S-parameters are S_{11} = 1.74 − j1.725, S_{21} = 0.197 + j1.042, S_{12} = −1.028 ×

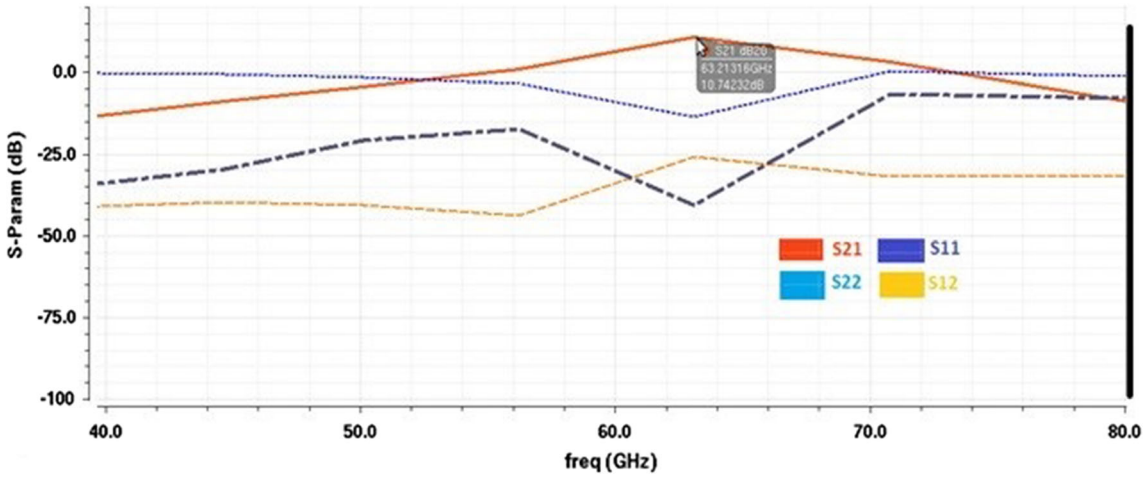

Fig. 17. *S*-parameter analysis.

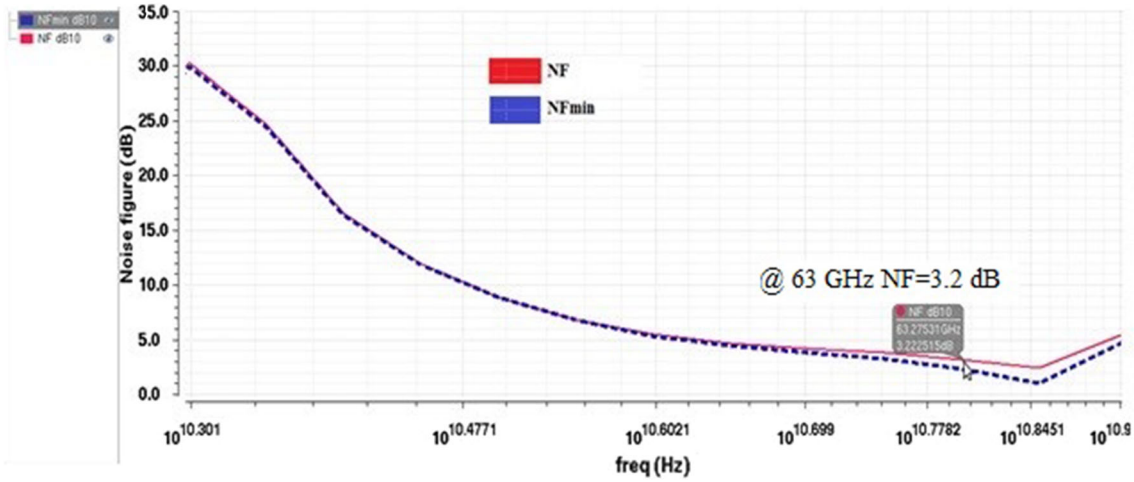

Fig. 18. Noise figure and NF_{min} of the proposed design.

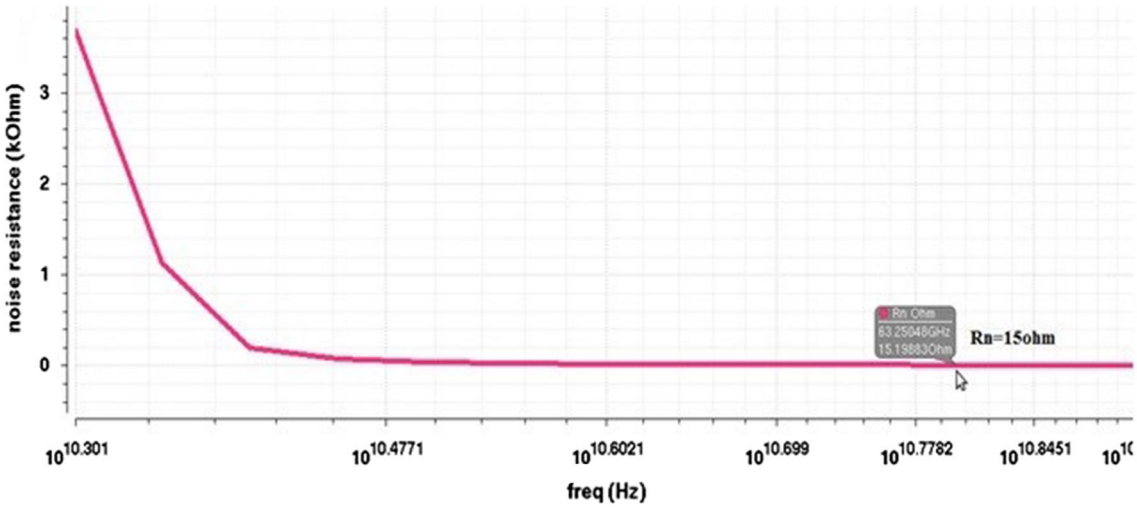

Fig. 19. Noise resistance.

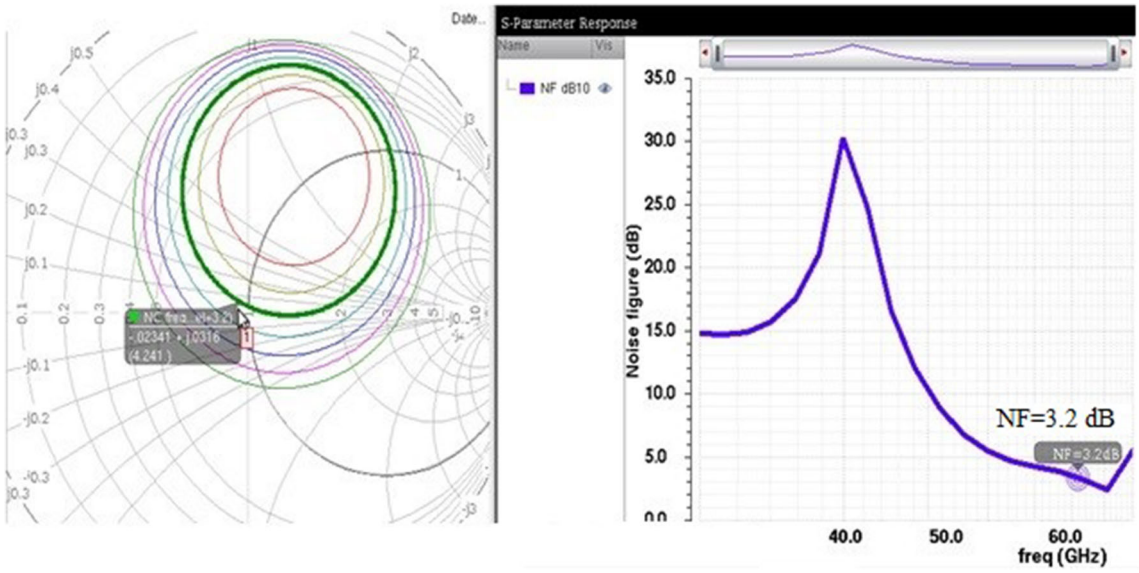

Fig. 20. NC and NF measurement at the desired frequency.

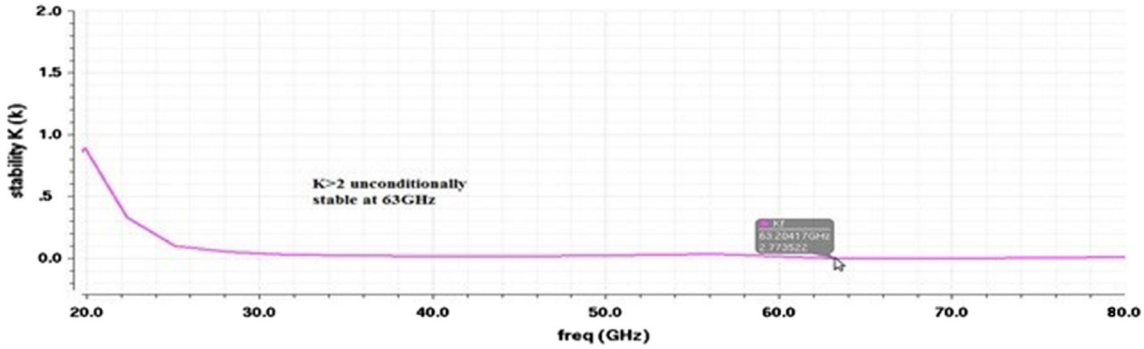

Fig. 21. Stability factor K for different frequencies.

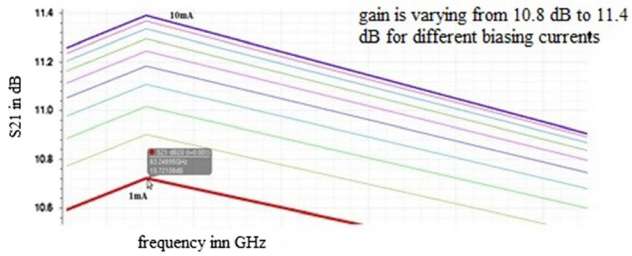

Fig. 22. S_{22} as a function of biasing current.

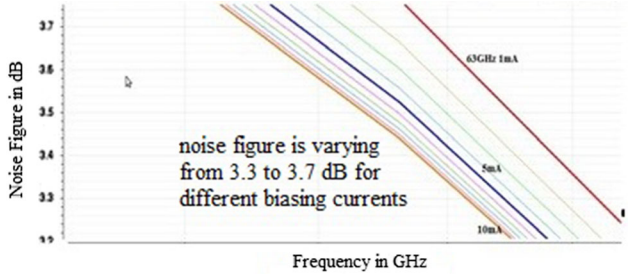

Fig. 23. S_{21} as a function of biasing current.

$10^{-3} - j0.199$ and $S_{22} = 0.58 - j4.636$. This yields the value of $K = 2.69$ and $\Delta = 0.457$, indicating the stability[7] of the system.

One more constraint of the LNA design is power consumption of the designed circuit. In the design, since V_{dd} is fixed, the biasing current can be altered to match the power specification of the design. Simulation is carried out for analyzing gain (S_{21}), matching (S_{11}, S_{22}) and noise figure (NF) for various dc values from 1 mA to 10 mA. Figure 22 depicts the variation of gain against reference current I_d. Figure 23 infers that maximum gain can be achieved with the highest reference current of 10 mA. Similarly, analysis is carried out for noise figure for variable reference current. Figure 24 depicts the noise figure variation as a function of different biasing currents. It indicates that both noise figure and gain performance can be enhanced by increasing the reference current. On the other hand, variation of input and output matching as a function of reference bias current is shown in Fig. 25. It clearly indicates that gain and noise figure performance improves with the reference current and that the input and output matching worsen with the reference current. In all the analysis, current is varied from 1 mA to 10 mA, which varies the power consumption of the circuit from 2.4 mW to 24 mW. The supply voltage is selected as $V_{dd} = 1.2$ V and $V_{ss} = -1.2$ V. To obtain better performance, an average value of 5 mA for the reference current is selected as a trade-off between gain matching the power consumption and noise figure. The power consumption of the proposed LNA is 12 mW at 5 mA of biasing current.

Layout

The layout of the proposed circuit is drawn by using the Cadence Virtuoso layout editor. The circuit basically uses six inductors which consume a major share of the total area. The layout of the proposed circuit is indicated in Fig. 25. The layout of the proposed circuit is 0.1075 μm^2. The comparison between targeted and achieved specifications of the proposed CG–CG current reuse architecture is given in Table I.

CONCLUSION

This paper presents the design of a CG–CG LNA using current reuse topology with a GPDK 180-nm CMOS process. It consists of a common gate in the first stage to achieve wideband input matching. The current reuse structure increases the gain of the two stages. By employing the inductive degeneration, a wide range of input matching can be achieved. The proposed topology attains maximum forward gain of 11 dB and a minimum noise figure of 3.2 dB at the desired 60 GHz using the 90-nm CMOS Cadence Virtuoso technique. It can give both input and output matching < -10 dB at 60 GHz and a power dissipation of 12 mW. The obtained results show that the proposed LNA is a suitable choice at 60 GHz. In the future, this can be designed using a minimum number of inductors.

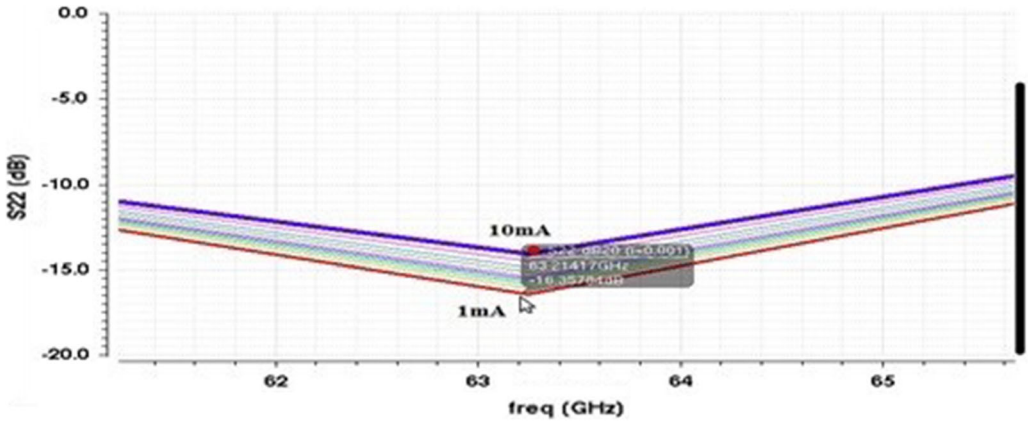

Fig. 24. NF as a function of biasing current.

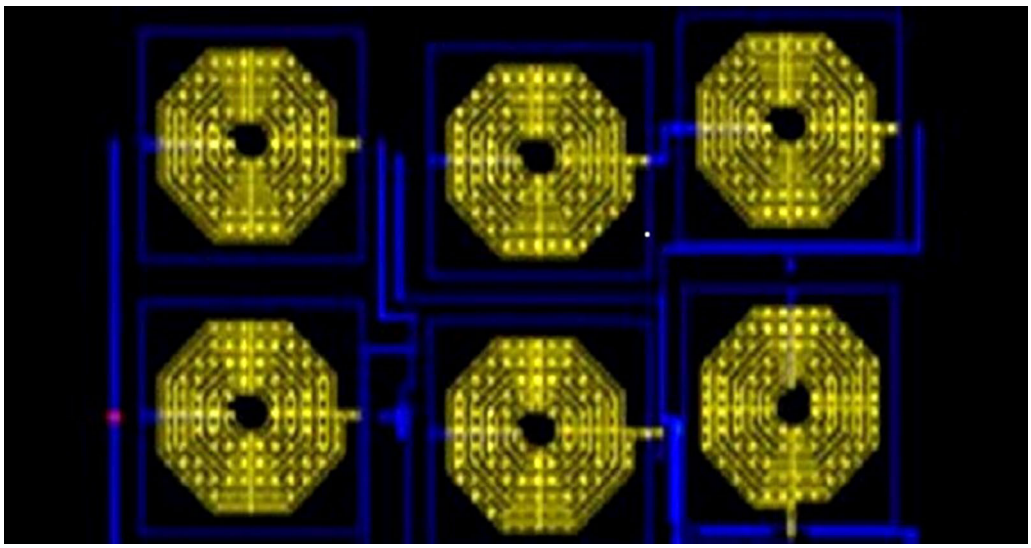

Fig. 25. Layout of the proposed circuit.

Table I. Comparison between targeted and achieved specifications of the proposed CG–CG current reuse architecture

Parameter	Desired specifications	Attained specification
Frequency	60 GHz	63 GHz
Input matching	< -10 dB	< -10 dB
Gain	10 dB	10.7 dB
Noise figure	3 dB	3.2 dB

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

REFERENCES

1. J. Lee, H. Park, H. Chang, and T. Yun, in *IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (2012), pp. 33–36.
2. H.-W. Chiu, S.-S. Lu, and Y.-S. Lin, *IEEE Trans. Microw. Theory Techn.* 53, 813 (2005).
3. J.Y. Lee, H.K. Park, H.J. Chang, and T.Y. Yun, *IET Microw Antennas Propag* 6, 793 (2012).
4. Y. Lin, S.S.H. Hsu, J. Jin, and C.Y. Chan, *IEEE Microw. Wirel. Compon. Lett.* 17, 232 (2007).
5. W. Hung, K. Lin, J. Hsieh, and S. Lu, in *2011 IEEE International Symposium of Circuits and Systems* (2011), pp. 1291–1294.
6. W. Lu, Q.Y. Pang, and S.Q. Liu, in *IEEE International Conference on Applied Superconductivity and Electromagnetic Devices* (2013), pp. 139–142.
7. C.W. Kim, M.S. Kang, P.T. Anh, H.T. Kim, and S.G. Lee, *IEEE J. Solid State Circuits* 40, 544 (2005).

8. J. Kaukovuori, M. Kaltiokallio, and J. Ryynanen, in *18th European Conference on Circuit Theory and Design, Seville* (2007), pp. 64–67.
9. S.B. Rashmi and S.S. Yellampalli, *Int. J. Innov. Technol. Explor. Eng.* 8, 249 (2019).
10. J.Y. Lee, J.H. Ham, Y.S. Lee, and T.Y. Yun, *IET Microw. Antennas Propag.* 4, 2155 (2010).