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Formation Mechanism of Atomically Flat Si(100) Surface by Annealing in Ar/H_2 Ambient

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In this study, the formation mechanism of an atomically flat Si(100) surface by annealing in Ar/4%H_2 ambient utilizing the quartz furnace and its effect on Hf-based Metal/Oxide/Nitride/Oxide/Si diodes were investigated. After the etching of the unintentional oxide layer formed by annealing at 1050–1100°C in Ar/4%H_2 ambient, the atomically flat p-Si(100) surface was obtained. Furthermore, it was found that the surface root mean square roughness was decreased with increasing the annealing duration. Finally, it was revealed that the *J*–*V* characteristics both of before and after 10^3 program/erase cycles of Al/$HfN_{0.5}$/HfO_2/$HfN_{1.0}$/HfO_2/p-Si(100) diodes were decreased one order of magnitude by a surface flattening process.

Key words: Atomically flat Si surface, atomic steps, annealing process, Ar/H_2 ambient, high-k gate insulator, Hf-based MONOS diodes

INTRODUCTION

To realize the high performance mobile electronics and internet of things (IoT) society, the nonvolatile memory (NVM) is one of the key technologies. However, the conventional floating gate (FG) type NVM is facing scaling limits in terms of coupling ratio, disturbance between the cells and so on.[1–4] The charge trapping (CT) type NVM such as Metal/Oxide/Nitride/Oxide/Si (MONOS) is one of the attractive candidates to realize further scaling down.[5,6] We have reported the excellent electrical characteristics of fully in situ formed Hf-based MONOS diodes by electron cyclotron resonance (ECR) plasm sputtering.[7]

However, it is necessary to reduce the operation voltage by scaling down vertically, even for the MONOS NVM with high-k gate insulator. As scaling down the gate insulator thickness, Si surface flattening technology would be one of the key factors to improve the data reliability and the operation speed. The roughness at the Si/SiO_2 and the gate electrode/SiO_2 interface significantly affected the device performance.[8–16] Even for high-k gate insulators, the roughness at the high-k/Si interface significantly affects the MISFET characteristics.[16–21]

It has been reported that the atomically flat Si(100) surface is able to be obtained by annealing in Ar, H_2 and O_2 ambient.[10–14,22–25] The atomically flat Si(100) surface consists of step and terrace structure, and the surface R_a roughness was approximately 0.03 nm on the terrace.[12] To realize the atomically flat surface by annealing in Ar ambient, an ultra clean annealing furnace and an ultra clean Ar gas supply system are necessary.[11,12,14] The O_2 and H_2O concentrations in the Ar gas were controlled to be less than 0.1 ppb and 0.2 ppb, respectively,[11] because the Si surface was affected by the small amount of O_2 and H_2O in the ambient.[26,27] On the other hand, there is the flammability limit in the case of H_2 annealing, especially for 4.0–75.0% hydrogen in the air. In the case of O_2 annealing, low O_2 pressure, especially less than 10^{-6} Torr, is necessary because the Si etching rate is influenced by O_2 pressure.[25]

We have investigated the flattening process for the Si(100) surface by annealing in Ar/H_2 ambient.[17–21,28,29] It has been revealed that the Si surface root mean square (RMS) roughness was reduced by annealing in Ar/4.9%H_2 ambient. However, the atomically flat surface has not been

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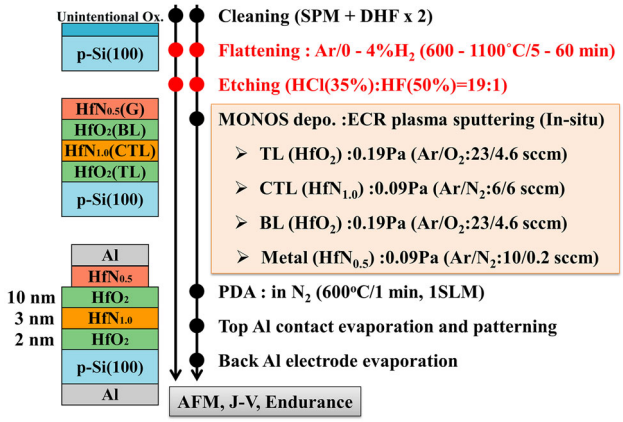

Fig. 1. Fabrication procedure.

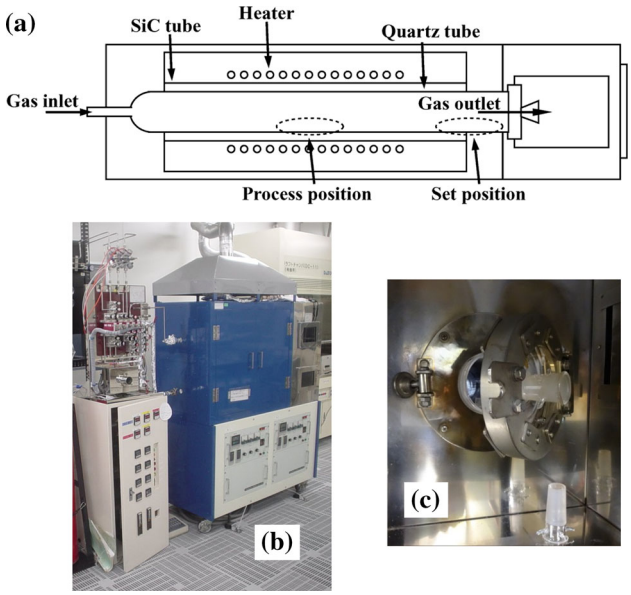

Fig. 2. (a) Schematic cross-section of furnace, and the pictures of (b) furnace and (c) loading part.

obtained by annealing in Ar/4.9%H_2 forming gas ambient utilizing the rapid thermal annealing (RTA) system probably because it is a cold wall system. To realize the atomically flat Si(100) surface by annealing in Ar and H_2 mixture ambient, the flattening mechanism should be clarified.

In this paper, we investigated the atomically flat Si(100) surface formation by annealing in Ar/4.0%H_2 ambient utilizing the quartz furnace, which is a hot wall system, and the Ar and H_2 flow rates are controlled by the mass flow controller independently. The electrical characteristics of Hf-based MONOS diodes were also examined.

EXPERIMENTAL PROCEDURE

Figure 1 shows the experimental procedure used in this research. The p-Si(100) substrates with off-angle of less than 1.0° were cleaned by sulfuric acid peroxide mixture (SPM, H_2SO_4:H_2O_2 = 4:1) and diluted hydrofluoric acid (DHF, HF:H_2O = 1:100) Then, the flattening process was carried out by annealing at 600–1100°C for 5–60 min in Ar/0–4%H_2 (3 SLM) ambient utilizing a quartz furnace as shown in Fig. 2. The purities of Ar and H_2 gases were 99.9999% and 99.99999%, which contained O_2 gas less than 100 ppb, respectively. The furnace has a SiC tube outside the quartz tube to prevent metal contamination from the heater during annealing.[10] Next, the unintentional oxide which was formed during the flattening process was removed by the wet etching using wet etchant of HF:HCl = 1:19.[30] $HfN_{0.5}$(M)/HfO_2(O)/$HfN_{1.0}$(N)/HfO_2(O) structure with thickness of 10/10/3/2 nm, respectively, that was in situ deposited on p-Si(100) by ECR plasma sputtering at room temperature (RT). The post-deposition annealing (PDA) was carried out at 600°C for 1 min in N_2 (1 SLM). After Al contacts evaporation, Al/$HfN_{0.5}$ metal layers were patterned to form MONOS diodes. Schematic band diagram of Hf-based MONOS structure is illustrated in Fig. 3.

The Si surface roughness was observed by non-contact mode atomic force microscopy (AFM,

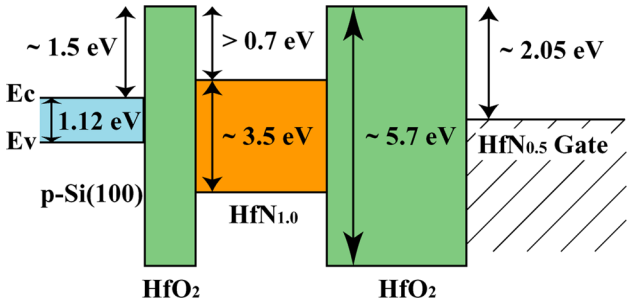

Fig. 3. Schematic energy band diagram of Hf-based MONOS diodes.

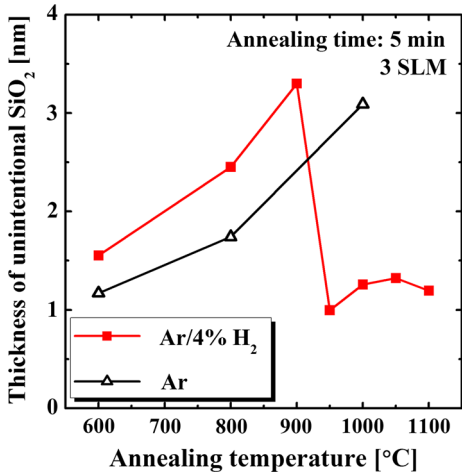

Fig. 4. Unintentional oxide layer thickness dependence on annealing condition.

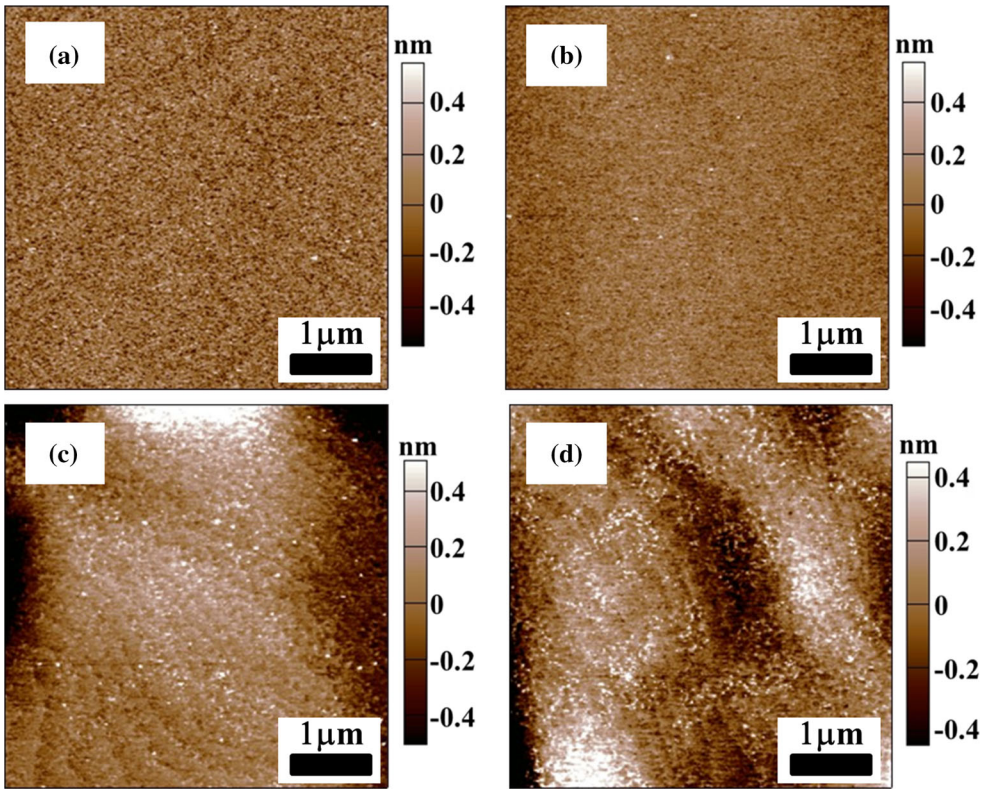

Fig. 5. AMF images of Si(100) surface after annealing in Ar/4.0%H_2 ambient. The temperature is (a) 950°C, (b) 1000°C, (c) 1050°C, and (d) 1100°C.

Cypher AFM). The unintentional oxide thicknesses were measured by ellipsometry (JASCO ELC-300). The electrical characteristics of MONOS diodes were evaluated by *J*–*V* measurements at RT using semiconductor parameter analyzer (Agilent 4156C).

RESULTS AND DISCUSSION

Annealing Temperature Dependence

Figure 4 shows the thickness of the unintentionally formed oxide layer during annealing at 600–1100°C for 5 min in Ar or Ar/4%H_2 ambient, respectively. In the case of annealing in Ar ambient, the thickness of the unintentional oxide layer was increased with increasing the annealing temperature. In our quartz furnace, the unexpected residual oxygen was induced by the back diffusion from the exhaust side during the loading and unloading process, which led to forming an unintentional oxide layer. Moreover, the thickness of the unintentional oxide layer was increased with increasing temperature in the case of annealing at 600–900°C for 5 min in Ar/4%H_2 ambient. However, in the case of annealing at 950–1100°C for 5 min in Ar/4%H_2 ambient, the thickness of the unintentional oxide was decreased to approximately 1 nm. This result indicated that hydrogen enhanced the formation of an unintentional oxide layer below 900°C. On the other hand, in the case of annealing at 950–1100°C, the unintentional oxide layer formed by the residual oxygen during the loading process was etched by the hydrogen, which was exposed to the Si surface during annealing. The unintentional oxide etching reaction is described as following equation.[31]

$$SiO_2[s] + H_2[g] \rightarrow SiO[g] + H_2O[g] \quad (1)$$

Figures 5 show the AFM images of Si(100) surface after the etching of the unintentional oxide layer formed by the annealing at 950–1100°C for 10 min in Ar/4%H_2 ambient. The scan size was 5 × 5 μm^2. The atomic steps were partially obtained in the case of annealing at 1050–1100°C for 10 min, while the surface roughness with a few micrometer period was formed simultaneously. However, in the case of annealing at 950–1000°C for 10 min, the atomic steps were not obtained. This result suggested that the migration of Si atoms was enhanced by the annealing at 1050–1100°C in Ar/4%H_2 ambient when the Si surface was exposed to annealing ambient. Finally, the atomic steps formation was realized partially by the annealing at 1050–1100°C for 10 min in Ar/4%H_2 ambient.

Annealing Duration Dependence

Figure 6 shows the scan size dependence of Si surface RMS roughness after annealing at 1050°C for 10 min in Ar/4%H_2 ambient. As shown in Fig. 6,

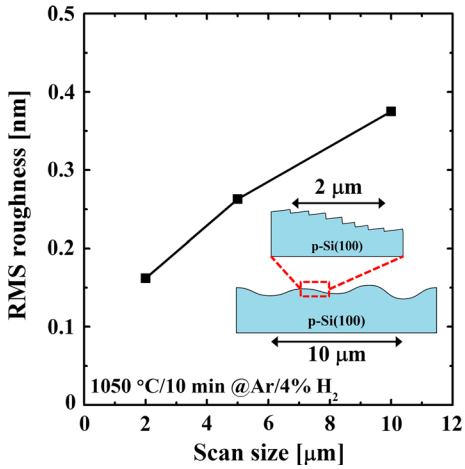

Fig. 6. Scan size dependence on Si surface RMS roughness and morphologies.

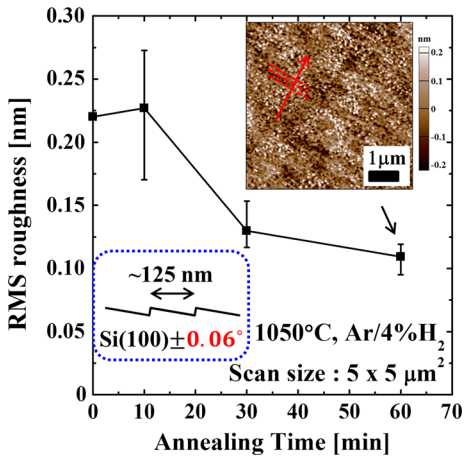

Fig. 7. Annealing duration dependence on Si surface RMS roughness and morphologies. Scan size is 5 × 5 μm^2.

it was found that the surface RMS roughness was increased with increasing the scan size of AFM measurements. This is caused by the surface roughness with a few micrometer period formed by the annealing in Ar/4%H_2 ambient, as shown in the inset of Fig. 6. It was reported that the pit defects were formed on the Si surface by annealing in pure H_2 ambient at the annealing temperature less than 1000°C, due to the fluctuations of the unintentionally formed SiO_2 thickness and the etching rate difference between Si and SiO_2.[32] It was speculated that the periodic Si surface roughness caused by the non-uniform SiO_2 formation which led to the local Si etching at the initial stage of flattening process in Ar/4%H_2 ambient. In order to form an ideal atomically flat surface, it is necessary to decrease the effect of this periodic roughness.

Figure 7 shows the annealing duration dependence on surface RMS roughness. The scan size was

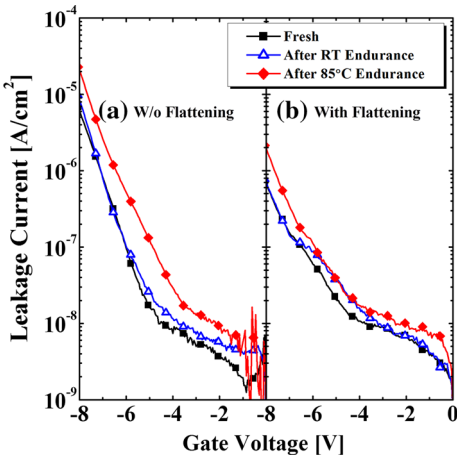

Fig. 8. *J–V* characteristics of Hf-based MONOS diodes after 10^3 P/E endurance. (a) W/o flattening, and (b) with flattening.

5 × 5 μm^2, which is enough size to evaluate both of the atomic steps and the periodic roughness. It was found that the surface RMS roughness was decreased with increasing annealing duration because of decreasing the periodic roughness. The obtained off angle from the AFM image by annealing at 1050°C for 60 min in Ar/4%H_2 ambient was 0.06° while the spec of Si wafer is the off angle below 1°.[10,11]

From these results, the formation mechanism of atomically flat Si(100) surface by annealing in Ar/H_2 ambient was considered as follows. During the loading process, the Si surface was slightly oxidized by the residual oxide. The unintentional oxide was etched by the reaction with hydrogen, and the bare Si surface was exposed. Then, Si atoms were migrated and decrease the periodic roughness and formed an atomically flat surface. Finally, the Si surface was re-oxidized by back diffusion during the unloading process.

Effects of Si Surface Flattening on Hf-Based MONOS

Figure 8 shows the *J–V* characteristics of Hf-based MONOS type diodes before and after the endurance with 10^3 program/erase (P/E) cycles measured at RT.[29] The endurance characteristic was measured at RT and 85°C with program voltage/time (V_{PGM}/t_{PGM}) of 10 V/1 s and erase voltage/time (V_{ERS}/t_{ERS}) of − 8 V/1 s, respectively. The gate leakage current after the P/E stress, such as stress induced leakage current (SILC), increased due to the increase of the trap state in the tunneling layer (TL), and it was further increased at high temperature.[33,34] The gate leakage current was measured at the negative bias voltage to investigate the reliability of gate stacks structure, and it decreased one order of magnitude by the surface flattening after the P/E cycles, especially for 85°C endurance as shown in Fig. 8. This is probably due

to the improvement of ONO layer reliability by the flattening process, especially for a 2 nm-thick HfO_2 tunneling layer (TL), which would suppress the degradation by the endurance.

CONCLUSIONS

We investigated the formation mechanism of an atomically flat Si(100) surface by annealing in Ar/H_2 ambient utilizing the quartz furnace, which is a hot wall system. The electrical characteristics of Hf-based MONOS type diodes were also examined. We have realized that both unintentional oxide etching and Si atoms migration were enhanced by annealing at 1050–1100°C. Furthermore, annealing duration of 60 min was able to decrease the surface RMS roughness, and form the atomically flat surface. Finally, the gate leakage currents of Hf-based MONOS type diodes before and after 10^3 P/E cycles were decreased one order of magnitude by the surface flattening process.

As a conclusion, it was revealed that an atomically flat Si(100) surface was able to be formed by annealing in Ar/H_2 ambient, and it was effective to improve the Hf-based NVM characteristics.

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REFERENCES

1. G. Zhang, X.-P. Wang, W.J. Yoo, and M.-F. Li, *IEEE Trans. Electron Devices* 54, 3317 (2007).
2. Y. Yamauchi, Y. Kamakura, and T. Matsuoka, *IEEE Trans. Electron Devices* 60, 2518 (2013).
3. C.-Y. Lu, K.-Y. Hsieh, and R. Liu, *Microelectron. Eng.* 86, 283 (2009).
4. C.Z. Zhao, J.F. Zhang, M.B. Zahidl, G. Groeseneken, R. Degraeve, and S. De Gendt, *Appl. Phys. Lett.* 89, 023507 (2006).
5. C. Zhao, C.Z. Zhao, S. Taylor, and P.R. Chalker, *Materials* 7, 5117 (2014).
6. S. Lee, Y.W. Jeon, T.-J.K. Liu, D.H. Kim, and D.M. Kim, *IEEE Trans. Electron Devices* 57, 1728 (2010).
7. S. Ohmi and Y. Liu, *IEICE Electron. Express* 12, 20150969 (2015).
8. T. Ohmi, K. Kotani, A. Teramoto, and M. Miyashita, *IEEE Electron Device Lett.* 12, 652 (1991).
9. T. Ohmi, A. Teramoto, R. Kuroda, and N. Miyamoto, *IEEE Trans. Electron Devices* 54, 1471 (2007).
10. X. Li, T. Suwa, A. Teramoto, R. Kuroda, S. Sugawa, and T. Ohmi, *ECS Trans.* 28, 299 (2010).
11. R. Kuroda, T. Suwa, A. Teramoto, R. Hasebe, S. Sugawa, and T. Ohmi, *IEEE Trans. Electron Devices* 56, 291 (2009).
12. R. Kuroda, A. Teramoto, S. Sugawa, and T. Ohmi, *Jpn. J. Appl. Phys.* 50, 04DC03 (2011).
13. W. Zhu, J.P. Han, and T.P. Ma, *IEEE Trans. Electron Devices* 51, 98 (2004).
14. T. Ohkawa, O. Nakamura, S. Sugawa, H. Aharoni, and T. Ohmi, *IEEE Trans. Electron Devices* 48, 2957 (2001).
15. S. Kudoh and S. Ohmi, *IEICE Trans. Electron.* E98-C, 402 (2015).
16. S. Kudoh and S. Ohmi, *IEICE Trans. Electron.* E99-C, 505 (2016).
17. S. Ohmi, *IEICE Electron. Express* 11, 20142006 (2014).
18. S. Ohmi, S. Kudoh, and N. Atthi, *IEEE Trans. Semicond. Manuf.* 28, 266 (2015).
19. D.H. Han, H.S. Han, and S. Ohmi, *IEICE Electron. Express* 10, 1 (2013).
20. D.H. Han and S. Ohmi, *IEICE Trans. Electron.* E96-C, 669 (2013).
21. D.H. Han, S. Ohmi, T. Suwa, P. Gaubert, and T. Ohmi, *IEICE Trans. Electron.* E97-C, 413 (2014).
22. K. Izunome, Y. Saito, and H. Kubota, *Jpn. J. Appl. Phys.* 30, L1277 (1992).
23. L. Zhong, R. Takeda, K. Izunome, Y. Matsushita, Y. Aiba, J. Matsushita, J. Yoshikawa, K. Hayashi, H. Shirai, and H. Saito, *Appl. Phys. Lett.* 68, 2349 (1996).
24. Y. Matsushita, H. Nagahama, R. Takeda, and M. Hirasawa, *ECS Trans.* 3, 159 (2006).
25. Y. Morita, T. Maeda, H. Ota, W. Mizubayashi, S. O'uchi, M. Masahara, T. Matsukawa, and K. Endo, in *IEEE International Electron Devices Meeting, Technical Digest* (2015), pp. 390–394.
26. M. Offenberg, M. Liehr, and G.W. Rubloff, *J. Vac. Sci. Technol., A* 9, 1058 (1991).
27. Y. Wei and R.M. Wallace, *J. Appl. Phys.* 8, 6415 (1997).
28. S. Kudoh and S. Ohmi, in *59th Electronic Materials Conference, Conference Digest* (2017), p. 57.
29. S. Kudoh and S. Ohmi, in *75th Device Research Conference, Conference Digest* (2017), pp. 119–120.
30. Y. Morita and H. Tokumoto, *Appl. Phys. Lett.* 67, 2654 (1995).
31. C.A. Schacht, *Refractories Handbook* (Boca Raton: CRC Press, 2004), p. 74.
32. H. Habuka, H. Tsunoda, M. Mayusumi, N. Tate, and M. Katayama, *J. Electrochem. Soc.* 142, 3092 (1995).
33. J. Kim and S.T. Ahn, *IEEE Electron Device Lett.* 18, 385 (1997).
34. S. Aritome, R. Shirota, G. Hemink, T. Endoh, and F. Masuoka, *Proc. IEEE* 81, 776 (1993).