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Electrical Characteristics of 10-kV 4H-SiC MPS Rectifiers with High Schottky Barrier Height

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This paper reports the study of the fabrication and characterization results of 10-kilo-volt (kV) 4H-SiC merged PiN/Schottky rectifiers. A metal contact process was developed to make the Schottky contact on *n*-type SiC and ohmic contact on *p*-type SiC at the same time. The diodes with different Schottky contact width were fabricated and characterized for comparison. With the improvement quality of the Schottky contact and the passivation layer, the devices show low leakage current up to 10 kV. The on-state characteristics from room temperature to elevated temperature (423 K) were demonstrated and compared between structures with different Schottky contact width.

Key words: Silicon carbide, high voltage, Schottky barrier height, high-temperature electrical performance

INTRODUCTION

With the development of emerging technologies for smart grid applications such as solid-state transformers (SSTs),[1] high-voltage power transistors and diodes play a key role in these technologies. Meanwhile, the development of wide-bandgap material, especially 4H-SiC has enabled single transistors and power rectifiers to block > 20 kV.[2,3] For power rectifiers with blocking voltage of more than 10 kV, most of the results published are using the PiN and junction barrier Schottky (JBS) structures,[3–6] but less based on other concepts like merged PiN/Schottky (MPS), most of which are demonstrated at lower voltage ratings.[7–9] The concept of JBS and MPS were both originally proposed by Baliga.[11,12] Though the structures look similar, the difference between the two structures is that MPS rectifiers must be engineered to inject minority carriers from the PN junction at the on state to reduce the on-resistance, while a JBS diode normally works on the unipolar mode. 4H-SiC MPS rectifiers are more difficult to fabricate than silicon MPS rectifiers, due the large built-in potential of the *P–N* junction for SiC. One approach has been demonstrated by using a hybrid concept of putting the epitaxial *p*-type region and JBS cells on one cell,[13] which will need extra epitaxial steps and masks. Previous work[10] has demonstrated that injection happens at very small Schottky contact width and high temperature. In this paper, the design and fabrication of SiC MPS rectifiers has been presented using the similar design as the previous study[10] but with improved performance, which will be demonstrated and explained in the following sections.

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DEVICE DESIGN AND FABRICATION

The schematic cross-section of the device half-cell structure is shown in Fig. 1, with the starting material of a highly doped *n*-type 4H-SiC substrate and an n-type 4H-SiC epitaxial layer purchased from Cree, with a thickness of 100 μm (tolerance ± 25%) and low doping concentration of 2.7×10^{14} cm^{-3} (tolerance ± 25%). The lifetime was measured on the wafer before processing, and the average lifetime measured by microwave photoconductance decay (μ-PCD) method on the wafer is 1.39 μs. The *p*-type region was formed by

aluminum ion implantation with a dose of 5e14/1e15/2e15/1e14 cm^{-1}, and energy of 30/70/140/300 keV at a temperature of 600°C, followed by high-temperature annealing up to 1800°C. This *p*-type region was implemented in the active cell area for the MPS structure, also in the edge termination area as multiple floating rings at the same time. The half-cell width of the Schottky contact (W_s), which was also the half-cell width between *p*-type region, was varied from 0.5 μm to 2 μm and named D1 to D4, and the half-cell width of the *p*-type region (W_p) was a 1.5-μm constant for D1 to D4, as shown in Fig. 1 and Table I. D0 is the PiN diode, in which aluminum was implanted all over the active region. D5 is the Schottky barrier diode (SBD) with the *p*-type region only at the edge termination area. All types of devices in Table I have the same active area and edge termination design. For the passivation layer, the atomic layer deposition (ALD) method was used to deposit 30 nm of silicon dioxide, followed by RTA in N_2O for 1000°C and 1 min, then another layer of silicon dioxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) with a thickness of 1 μm. The oxide deposited by ALD and the N_2O annealing can reduce the density of interface states and hence improve the device performance under reverse bias.[14,15] The backside ohmic contact was formed by evaporation of nickel and RTA at 950°C for 2 min. Then, the contact metal process was optimized by electron beam evaporation of nickel followed by RTA at 850°C and 1 min under nitrogen, and the Schottky contact on n-type SiC and the ohmic contact on ion implanted *p*-type SiC was formed with this single process.[18] This process eliminates the alignment of the contact layer to the *p*-type implantation layer, thus reducing the fabrication cost and complexity. At last, the thick metal and polyimide was patterned and deposited on top before electrical characterization.

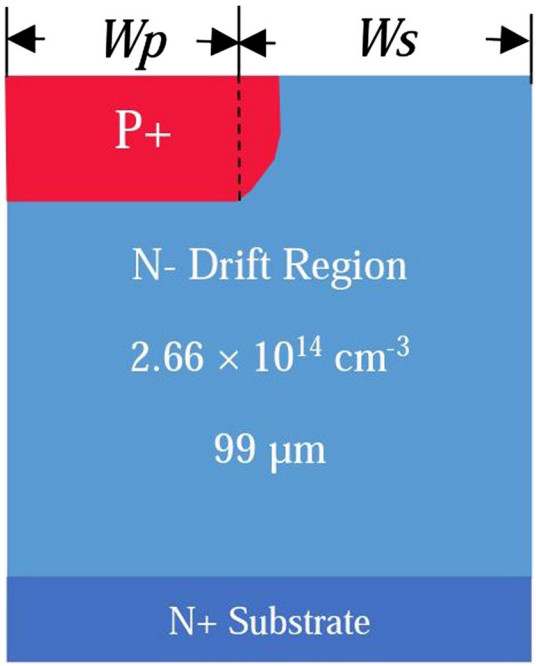

Fig. 1. Schematic half-cell cross-section of SiC MPS rectifiers.

ELECTRICAL CHARACTERIZATION RESULTS

First, the Schottky contact was evaluated through the test structures all over the wafer. The forward IV of Schottky diodes was tested with active an area of 3.36×10^{-3} cm^2, and the Schottky barrier height (SBH) and ideality factor is extracted by using the Richardson constant of 146 A cm^{-2} K^{-2} for silicon carbide. The distribution of the SBH and ideality factor is shown in Fig. 2a. Most of the test structures show an ideality factor of less than 1.1 and SBH of over 1.7 eV. The relationship between the SBH and ideality factor was also plotted in Fig. 2b, where most of the values are in a linear relationship, which implies an interface of inhomogeneous distribution of barrier heights.[16] The high SBH helps reduce the leakage current of the diodes under reverse bias,[17] and causes large potential difference between the *P–N* junction, which helps induce the injection of holes from the P region. The ohmic contact was evaluated using the TLM structures, and the average contact resistance is 1.4×10^{-4} Ω cm^2.

The forward current–voltage characteristics of D0–D5 with an active area of 6.68 mm^2 are shown in Fig. 3a. D5 has the lowest knee voltage of 1.3 V compared to other structures, and the knee voltage increases as W_s becomes smaller. D0 shows the typical PiN diode behavior with a knee voltage of 2.5 V and smaller differential resistance at higher voltage due to the minority injection. The forward current–voltage characteristics at 423 K are shown in Fig. 3b. All types of devices have non-linear characteristics, which indicates strong minority injection due to the reduced built-in potential of the *P–N* junction at higher temperature. The forward voltage at 20 A cm^{-2} at different temperature is shown in Fig. 4. D0 has continued to increase of forward voltage until 380 K, while D0 and D1 show obvious forward voltage decrease at high temperature.

The reverse current–voltage characteristics of device with area of 6.68 mm^2 are plotted in Fig. 5. No significant leakage current difference is found for different structures, and even the SBD (D5) has a very low leakage current due to the high SBH and improved quality of the interface between passivation and SiC. A much lower leakage current and higher breakdown voltage is achieved compared to previous results[19] in Fig. 6. The edge termination design, and the aluminum ion implant dose, energy and conditions in previous work is the same as in this work. The difference is the frontside Schottky contact and the passivation stack on the edge

Table I. Device types with different contact widths (W_s and W_p)

Name	W_s (μm)	W_p (μm)
D0 (PiN)	0	–
D1	0.5	1.5
D2	1	1.5
D3	1.5	1.5
D4	2	1.5
D5 (SBD)	–	0

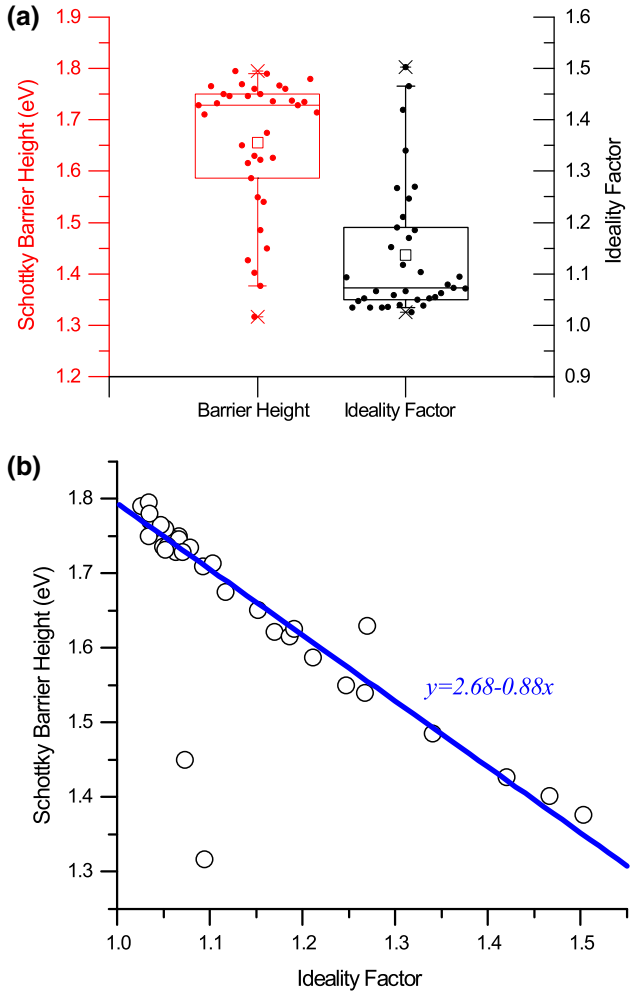

Fig. 2. (a) Distribution of extracted Schottky contact barrier height and ideality factor on a wafer. (b) Relationship between Schottky barrier height and ideality factor measured on wafer.

termination area. The SBH of the devices in previous study is 0.89 eV with an ideality factor of 2.4, which does not have an annealing process, and current work shows better quality of the Schottky contact. The passivation layer of the previous work only had one PECVD oxide layer and did not go through nitrous oxide annealing.

The edge termination is designed with multiple floating field rings, and with a constant p-type ring

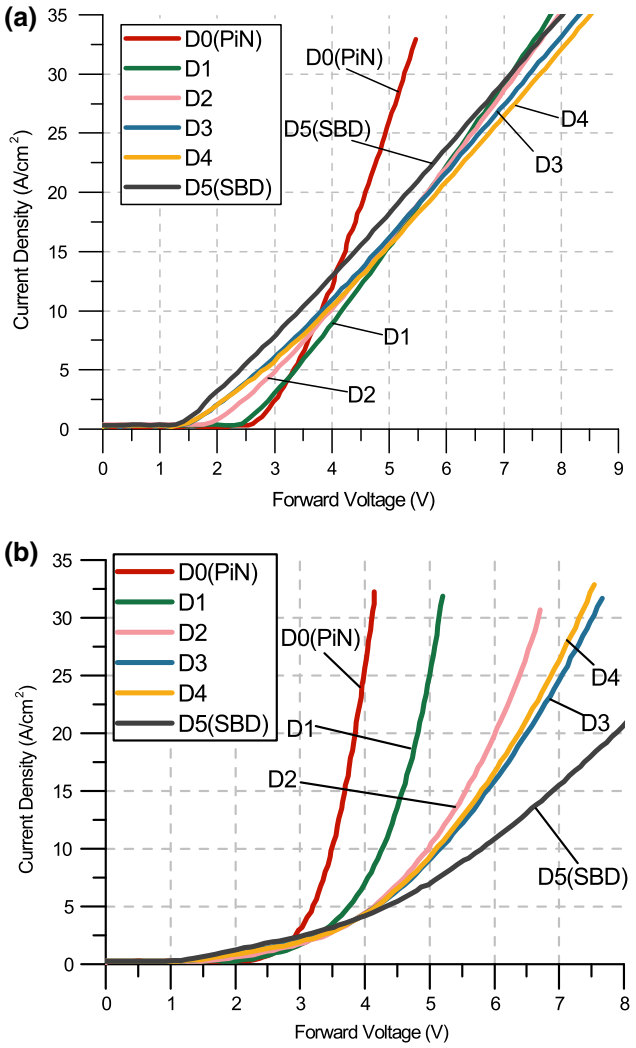

Fig. 3. (a) Forward IV of different types of diodes at room temperature. (b) Forward IV of different types of diodes at 423 K.

width of 4 μm and increasing space width as shown below:

$$S_n = S_1 + [(n-1)S_i]^2$$

The S_n means the space width between the $(N-1)$th ring and the Nth ring, and $S_1 = 1$ μm, $n = 100$. In Fig. 7, type A design means Si = 0.0175, type B design means Si = 0.0225 and type C design means Si = 0.0275. The best reverse I–V of small devices (area of 1.13 mm^2) on wafer in Fig. 7 reveals higher breakdown voltage probably due to less process and material defects, and the highest breakdown voltage achieved is 14.0 kV.

DISCUSSION

There are two main factors that are contributing to the forward current–voltage characteristics of MPS diodes. One is the mobility of electrons, which

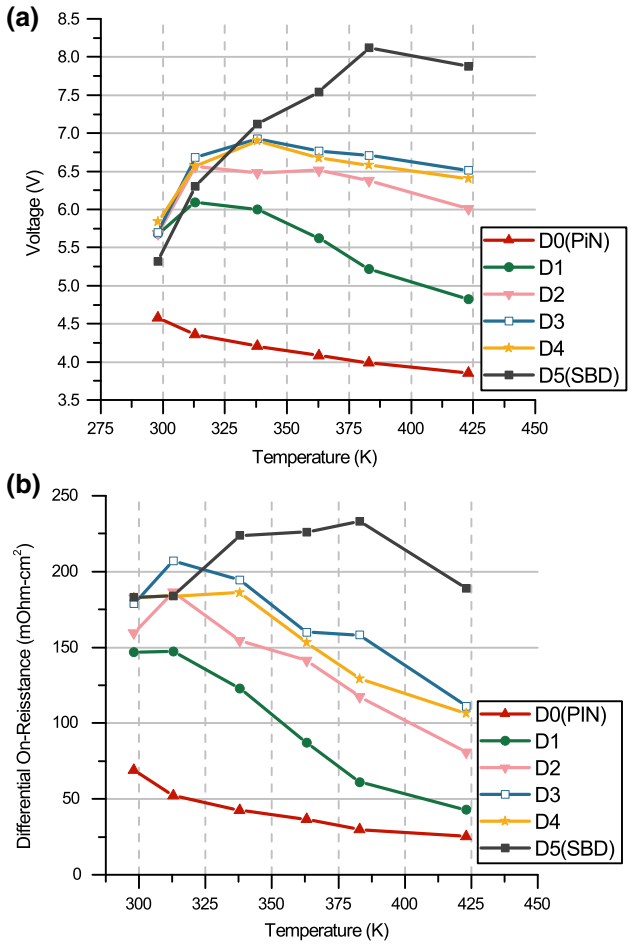

Fig. 4. (a) Forward voltage of different types of diodes at 20 A cm^{-2} at different temperatures. (b) Differential on-resistance at 20 A cm^{-2} for different types of diodes at different temperature.

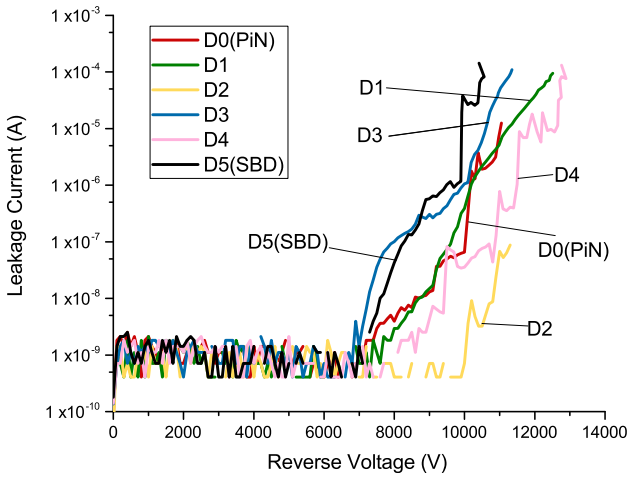

Fig. 5. Reverse IV of different types of diodes with an active area 6.68 mm^2 at room temperature.

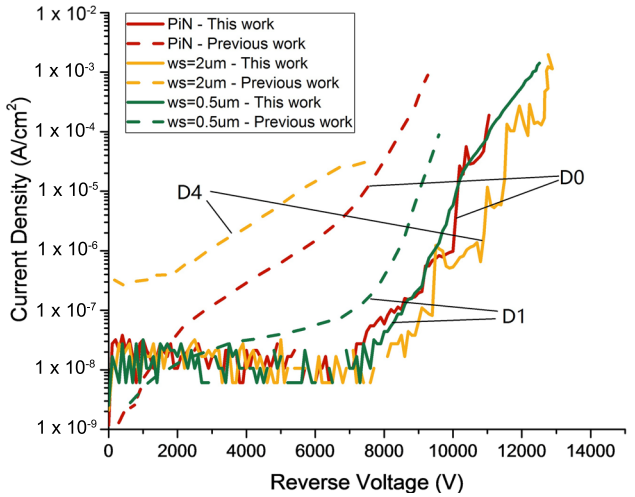

Fig. 6. Reverse IV for different types of devices compared to data from Ref. 19.

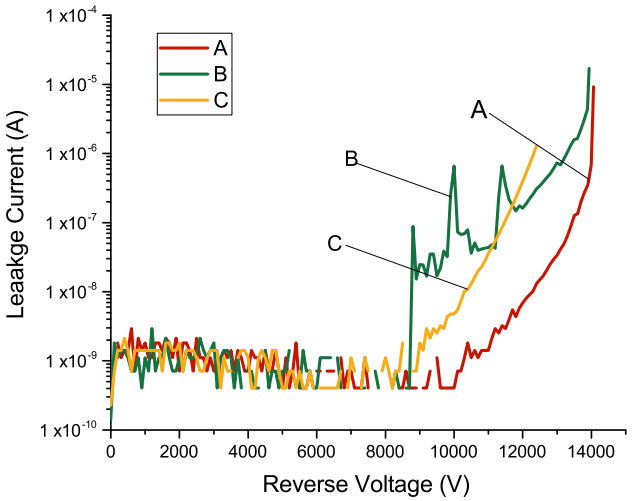

Fig. 7. Reverse IV of MPS (D1) with a small active area (1.13 mm^2) with different edge termination design.

are the majority carriers for the unipolar device with an n-type drift region. The mobility decreases with temperature, which contributes to the increased differential resistance at high temperature. Another one is the minority lifetime which is increasing with temperature and leads to decreased differential on-resistance, which has been proved by experimental results[20,21] and may be due to the increased emission rate of carriers from material defects at high temperature. For structure D5, most of the area is covered by the Schottky contact, so the majority current is taking the lead in conduction mode; thus mobility plays a key role in increasing the resistance with temperature. From D5 to D0, with the smaller width of the Schottky contact, more minority injection happens, which leads to the decreasing of resistance with temperature. It is worth noticing that even without a P region at the active region, the forward voltage of D5 decreases at 423 K. It may due to the overlap between the first p-type ring of the edge termination and the anode

contact, which will also induce hole injection at certain states.

CONCLUSION

SiC MPS diodes with different Schottky contact widths were fabricated, and the static characteristics were characterized from room temperature to high temperature (423 K). All types of devices show a low leakage current and high blocking voltages over 10 kV, which are probably due to the high SBH and the improved quality of the passivation layer with ALD oxide followed by N_2O annealing. The difference of the temperature dependence of forward *I–V* behavior with different types is due to the varied portion of current from minority carriers, which is larger for structures having narrower Schottky contact width.

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