

# A Modular and Programmable Development Platform for Capsule Endoscopy System

Tareq Hasan Khan · Ravi Shrestha · Khan A. Wahid

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**Abstract** The state-of-the-art capsule endoscopy (CE) technology offers painless examination for the patients and the ability to examine the interior of the gastrointestinal tract by a noninvasive procedure for the gastroenterologists. In this work, a modular and flexible CE development system platform consisting of a miniature field programmable gate array (FPGA) based electronic capsule, a microcontroller based portable data recorder unit and computer software is designed and developed. Due to the flexible and reprogrammable nature of the system, various image processing and compression algorithms can be tested in the design without requiring any hardware change. The designed capsule prototype supports various imaging modes including white light imaging (WLI) and narrow band imaging (NBI), and communicates with the data recorder in full duplex fashion, which enables configuring the image size and imaging mode in real time during examination. A low complexity image compressor based on a novel color-space is implemented inside the capsule to reduce the amount of RF transmission data. The data recorder contains graphical LCD for real time image viewing and SD cards for storing image data. Data can be uploaded to a computer or Smartphone by SD card, USB interface or by wireless Bluetooth link. Computer software is developed that decompresses and reconstructs images. The fabricated capsule PCBs have a diameter of 16 mm. An ex-vivo animal testing has also been conducted to validate the results.

**Keywords** Endoscopy · Field programmable gate array · Finite state machine · Compressor · Ex-vivo testing

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T. H. Khan · R. Shrestha · K. A. Wahid (✉)  
Department of Electrical and Computer Engineering, University of Saskatchewan, Saskatoon, Saskatchewan S7N5A9, Canada  
e-mail: khan.wahid@usask.ca

## Introduction

The commonly used flexible or wire endoscopes enable diagnosis inside esophagus, stomach and some part of small intestine, however, a large portion of the small intestine is still difficult to reach. The pain and discomfort caused by the flexible endoscope reduces the interest of many patients to undergo for such a procedure. The recently introduced capsule endoscopy (CE) [1, 2] technique has a major impact in the field of endoscopy as it can greatly reduce the level of patients' discomfort and also can reach the small intestine of the gastrointestinal (GI) tract. Before the introduction of CE, it was impossible for gastroenterologists to examine tissues of the small intestine without performing a surgical operation. In CE, after a one night fast, the patient ingests a vitamin-sized electronic pill, which passes through the GI tract by peristalsis. While travelling through the GI tract, the pill takes images and transmits them wirelessly to a portable data recorder unit attached to a belt, around the patient's waist. Images are captured for around eight hours and patients are free to conduct their daily activities during this time. The capsule is expected to evacuate naturally from the body after approximately 24 h. The stored data from the data recorder unit are then downloaded to a physician's workstation and images are reconstructed for analysis. The success of CE has sparked the interest among several industries and university research groups in order to advance the technology. The first commercial CE system, *PillCam*, was developed by *Given Imaging* in the year 2000 [3]. It was approved by the Food and Drug Administration (FDA) [4] in 2001. For the detection of damage or disease in esophagus, small intestine and colon, *Given Imaging* introduced *PillCam ESO*, *PillCam SB* and *PillCam COLON* namely [3]. Several other products [5, 6] also came to market recently.

In the literature, several capsule prototype works are reported based on field programmable gate array (FPGA)

and application specific integrated circuit (ASIC) technology. The work in [7] presents a development system based on FPGA that was specifically designed for testing the entire electronics to be integrated in an endoscopic capsule. The implemented compressor is based on integer version of discrete cosine transform (DCT) and it needs the buffering of the entire image frame in an external SRAM which will consume significant amount of area and power in real world implementation. In [8], a demo prototype of a wired-endoscopy is developed using a commercial CMOS image sensor connected with a FPGA board by 1.5 m cable. The prototype is then tested during ex-vivo and in-vivo experiments on a porcine model. A prototype with six camera, FPGA and flash memory is presented in [9]. The captured image data is saved in the flash memory inside the capsule instead of being transmitted outside human body wirelessly. However, the capsule may remain inside the intestine for several days (known as *capsule retention* [3]) and the collection of the image data will be difficult. In [10], an ASIC based capsule prototype is discussed. However, the work does not provide any animal testing results to evaluate the actual performance of the prototype in the real-world. In [11], an NBI image sensor for CE application is proposed. The works in [12] and [13] proposes capsule prototypes focusing on the design of a 20 Mbps RF transceiver.

Several capsule prototype works are also found based on commercial microcontrollers and other off-the-shelf components. The work in [14] discusses a basic level capsule prototype using CMOS analog video camera, a TV modulator IC, a helical antenna, and a lighting system with four white LEDs. In [15], a wireless endoscope system is developed with embedded Linux technology and the ARM microprocessors. A digital CCD image sensor (MT9D111) is used to acquire images and an image compressor (ADV202) is used to compress the acquired images to JPEG2000 format. In [16], a capsule prototype made of commercially available components such as CMOS image sensor with an integrated JPEG compression engine, ARM 32-bit Cortex™-M3 microcontroller, and an RF transceiver module is presented. In [17], a capsular endoscopy prototype with autofocus function is developed with a microcontroller (CC2430), a commercial camera (MO-S588) and an IEEE 802.15.4 compliant transceiver. A liquid lens (ARCTIC 416) is used to adjust the overall focal length. However, these microcontroller based system makes the prototype bulky and power hungry, which do not meet the key design challenges of the capsule hardware.

The paper in [18] describes a 3D endoscopic video system designed to improve visualization by increasing viewing angle and zone for multi-viewing. This enhances the ability of the surgeon to perform delicate endoscopic surgery. In [19], a non-invasive image guided biopsy marking system for gastroscopy is proposed. In this method, the position of the gastroscope relative to the stomach is acquired using an

electromagnetic tracking device and displayed in the guidance interface. The biopsy positions are recorded in computer for the use of guidance in follow-ups. In [20], a secured framework of remote access to endoscopic images has been proposed where images are uploaded in a compressed JPEG (Joint Photographic Experts Group) format. Gastroenterologists from different hospitals can access the server using internet and view these endoscopic images for diagnostic and discussion purpose. In [21], a WWW database for gastrointestinal video-scope images is designed where the images are stored using MPEG-1 compression. The database is linked with ISDN at 128 Kbps, which enables access of the images over the phone line. An automatic bleeding detection algorithm from the CE images based on semi-automated region growing and Probabilistic Neural Network (PNN) is proposed in [22]. The features of bleeding region in CE images are extracted and a PNN classifier is used to recognize these bleeding regions.

In this work, a modular and flexible CE development system platform consisting of a miniature FPGA based electronic capsule, a microcontroller based portable data recorder unit and computer software is developed. The system is intended to be used in animal trial where animal like a pig may be used to validate the performance of the system. Due to the flexible and reprogrammable nature of the system, various image processing and compression algorithms can be tested in the design without requiring any hardware change. The capsule hardware is designed using four printed circuit boards (PCBs), thus any portion of the hardware can be replaced or upgraded without affecting others boards. The developed capsule prototype supports various imaging modes including white light imaging (WLI) and narrow band imaging (NBI) [23], and communicates with the data recorder in full duplex fashion. It enables configuring the image size and imaging mode in real time during the examination. In the proposed capsule prototype, a low complexity image compression algorithm using YEF color-space (as described in [24]) is implemented to validate the performance. An ex-vivo animal trial has been conducted with the prototype. The proposed modular design will allow researchers to use image compression algorithms of various complexities. For examples, low complexity schemes such as, integer discrete cosine transform (DCT) based compressor [25], JPEG-LS based image compressor [26], and prediction-based lossless compressor [27] can be implemented simply by reprogramming the FPGA and without making any changes to the hardware design. On the other hand, high complexity algorithms, such as, compressor based on compressed sensing theory [28] and Lempel-Ziv-Welch (LZW) based data encoder [29] can also be implemented by upgrading the FPGA chip with more resources such as, memory and logic cells.

The proposed data recorder contains graphical LCD for real time image viewing and SD cards for storing image data. Data can be uploaded to a computer or Smartphone by SD card, USB interface or by wireless Bluetooth link. The computer software is developed to decompress and reconstruct images for diagnostics. The electronic capsule, the data recorder and the software have been prototyped in the laboratory.

It should be noted that in a CE system, power consumption of the electronic capsule is a key constraint. So, one has to be careful in choosing processing algorithms to be used in the capsule prototype. Algorithms for auto-detection of bleeding [22], 3-D imaging [30], CE image segmentation [31], etc. are complex in nature and may not be employed in the capsule which will consume more resource and power. However, these algorithms can be implemented in the data logger unit where more resources are available. In addition, information from other body sensors (such as, heart rate, blood pressure, etc.) could be integrated to the data logger using its input interface; this information could be analyzed in real-time to make a decision and accordingly control the parameters of the electronic capsule (such as, changing frame rate, image size, toggling between WLI and NBI modes, etc.). Moreover, localization schemes, i.e., position of the capsule, can be deployed by measuring the strength of the RF signal at various positions [32]. This can all be done using the existing prototype since it does not require any additional module or reprogramming. All one needs is to add multiple receiver nodes that will be connected to the data logger and then process it.

### Design criteria

In order to design a flexible capsule endoscopy (CE) development system, we set the following design criteria:

- The capsule should be reprogrammable, so that various image processing and compression algorithms (such as lossy and lossless) can be tested in order to find the most optimum solution, without any hardware change.
- The image sensor and the RF transceiver in the capsule should have standard interfaces enabling to test different components from different vendors.
- The capsule should support various lighting modes (such as WLI and NBI) and several types of LEDs must be present with the ability to control their intensity.
- The capsule should have an RF transceiver having sufficient bandwidth and error correction capability for proper transmission of the images. For example, for QVGA (320×240) resolution at 2 frames-per-second (FPS) and 80 % compression ratio, the required application

throughput of the wireless transceiver is estimated to be at least 722 kbps.

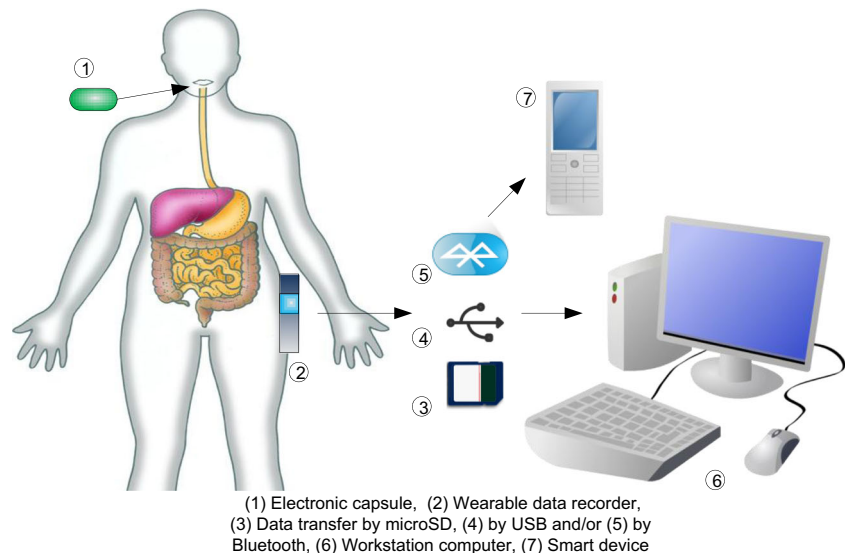
- The power consumption of the capsule must be low and should be able to work for more than 8 h.
- The hardware design of the capsule should be modular, thus one board can be modified or upgraded without requiring to change other boards.
- The size of the capsule should be small enough so that it can be swallowed or inserted in animal intestine for in-vivo or ex-vivo animal trial.
- The capsule should communicate with the data-recorder in full-duplex fashion, so that the capsule can be configured in different settings by sending commands from the data-recorder wirelessly in real-time.
- The data recorder should have sufficient capacity to store images for 8 to 10 h. For example, to store QVGA color, 24 bits-per-pixel images transmitted at 2 FPS having 80 % compression ratio for 10 h, at least 3.1 GB memory space is required.
- The data recorder should offer a display, such as graphical LCD, for real time viewing of the images.
- There should be multiple ways of data transfer from data logger to a computer or Smartphone.
- The software should be able to decompress images for diagnostics in both desktop and tablet platform.

### The capsule endoscopy system architecture

The overall architecture of the proposed capsule endoscopy system is shown in Fig. 1. The system mainly consists of three major units—the capsule, the data recorder and the workstation (such as desktop or Smartphone) software. In order to receive an image frame from the capsule, a command is sent wirelessly from the data recorder unit to the capsule. The command contains the required image size, imaging and compression mode, which can be changed at anytime during data recording by the user through a graphical user interface (GUI) of the data recorder. After receiving the command, the capsule configures its image sensor and starts to send data packets of the image frames in compressed form wirelessly. The data recorder reads the packets, stores them in SD card and if needed decompresses and displays images on its LCD in real-time. The image data from the data recorder can be transferred to a desktop computer or tablet using SD card, USB interface, or by Bluetooth link. The computer software decompresses the images so that diagnosis can be performed.

The architecture of three major units—the capsule, the data recorder and the workstation (such as computer or Smartphone) software are briefly described below.

**Fig. 1** Capsule endoscopy system architecture



### Architecture of the electronic capsule

To make the hardware modular, the capsule is divided in four boards: *Imaging board*, *FPGA board*, *RF board* and *Power board*. The components are chosen considering performance, power requirement and physical size to fit into a miniature capsule prototype. The overall block diagram of the capsule is shown in Fig. 2. A brief description of each board is given below.

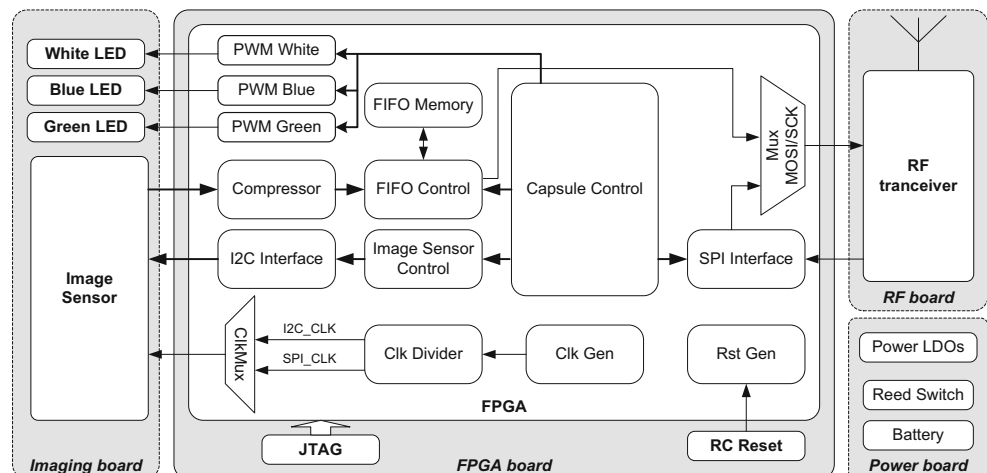
#### *Imaging board*

A commercial CMOS image sensor [33] is used in the capsule for capturing images. The image sensor sends pixel data in raster-scan fashion through a standard digital video port (DVP) parallel output interface, enabling to change the sensor with other sensors from different vendors which implements DVP interface, without major change in the design. It supports images of different size such as VGA (640×480), QVGA

(320×240), QQVGA (160×120), subQCIF (128×96) etc. The sensor can be configured through two wire *I2C interface* [34]. The physical size of the sensor is 6×6×4.5 mm and a lens with adjustable focal length is placed over the pixel array.

In order to support both WLI and NBI imaging modes, two white LEDs [35], one blue LED [36] having a peak wavelength of 405–410 nm and one green LED [37] with a peak wavelength of 520 nm are used in the design. The white LEDs are illuminated while capturing WLI images. While capturing NBI images, one frame is captured by illuminating the blue LED and the next frame is captured by illuminating the green LED; these two frames are later combined or processed to generate a high contrast NBI image. LEDs intensity is controlled by pulse width modulation (PWM) signals, which is generated by the controller. Due to the modular PCB design of the capsule, the *imaging board* can be replaced by other boards with different types of LEDs (such as infrared, ultraviolet, cool white, warm white, etc.) in order to explore and test different lighting modes.

**Fig. 2** Architecture of the electronic capsule



FPGA board

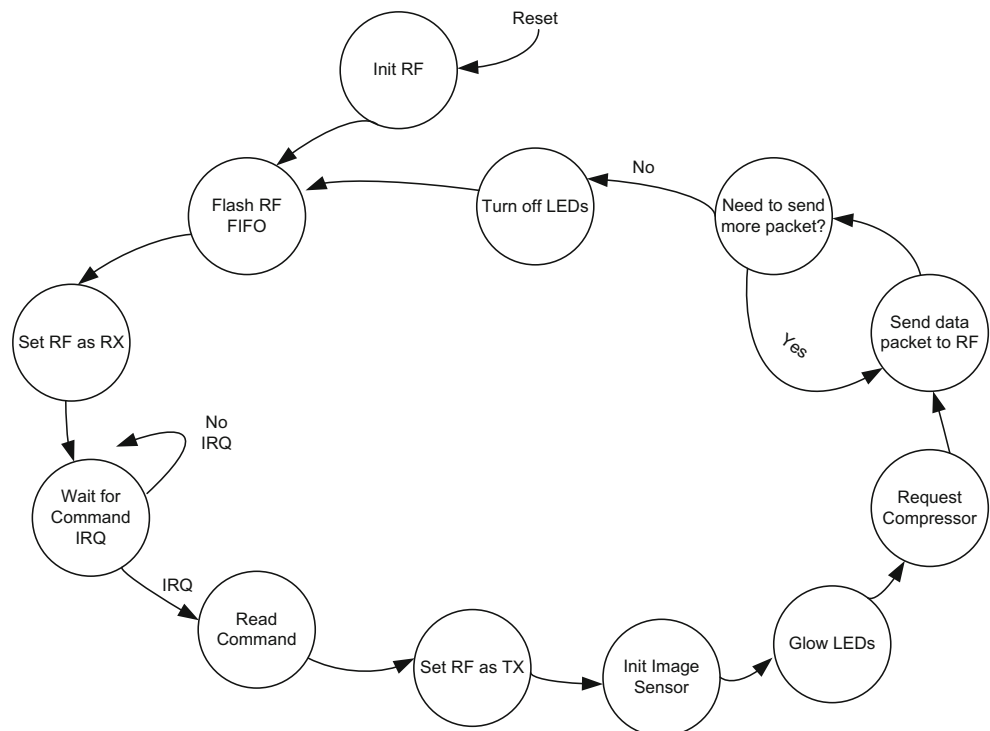
This board contains the FPGA and an RC reset circuit. The RC reset circuit generates an active low reset signal after power up for resetting the FPGA. It contains all the custom designed digital blocks needed for proper functioning of the electronic capsule. The chosen FPGA [38] has physical dimension of  $8 \times 8 \times 1.23$  mm and contains 2,112 lookup tables (LUTs), non-volatile RAM for storing configuration, built in clock generator, on-chip general purpose RAM blocks, and 104 I/O lines which makes it a suitable choice for this application. The board also contains JTAG interface for programming and debugging purpose. The digital blocks implemented inside the FPGA are briefly described below.

**Capsule control** This block controls the overall capsule operation. A finite state machine (FSM) is implemented inside this block as shown in Fig. 3. After getting reset signal, it initializes the RF transceiver parameters such as setting the data rate, channel frequency, packet size, auto-acknowledgment mode, etc. The communication with the RF transceiver is done using the SPI interface block. Then it flashes the internal fast in fast out (FIFO) buffer of both the RF transceiver and the buffer of FIFO Control block and then sets the RF transceiver in RX (i.e. receiver) mode. The state machine then waits for a command to be sent by the data recorder. After a command is received, it stores it in an internal register. The transceiver is then set in TX (i.e. transmitter) mode. Depending upon the

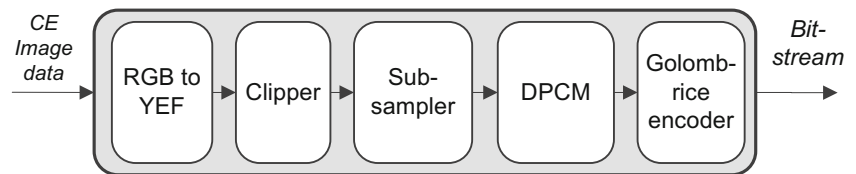
command, the image sensor is then initialized with proper frame size by the Sensor control block and proper LEDs are turned on based on the imaging mode (such as WLI or NBI). A request signal is sent to the compressor block and the compressor starts to send compressed data bits of the captured image to the FIFO control block. The state machine then requests the FIFO control block to send a complete data-packet (consists of 256 bit) to the RF transmitter directly through the MuxMOSI/SCK multiplexer. After a data packet is sent, it checks whether more packets needs to be sent for the current image frame or not. If more packets need to be sent, then it repeats the above procedure. After all packets of the current image frame is sent, it turns off all LEDs, flashes RF FIFO buffer, sets the RF transceiver in RX mode and waits for the next command.

**Image sensor control, I2C interface, PWM** These blocks are used to configure different settings of the image sensor depending on the received command from the data-recorder unit. At the *Init Image Sensor* state as shown in Fig. 3, the Capsule Control block requests the Image Sensor Control block to set the internal configuration registers which then communicates with the image sensor using the I2C Interface (master mode) [34] block. After the image sensor is configured, the clock input for these blocks are turned off by a glitch free clock gate [39] to save dynamic power. Three instances of PWM block are used in the design to adjust the light intensity of the white, blue and green LEDs. Each block takes a three bit intensity

Fig. 3 FSM inside capsule control block



**Fig. 4** Block diagram of the compression algorithm [24]



input from the *Capsule Control* block, giving the opportunity to control the light intensity at eight different levels.

**Compressor** In the proposed capsule endoscopy system, the image data are transmitted wirelessly from the ingested capsule in compressed form. Our proposed compression algorithm consists of a novel color space, YEF [24, 40], which is designed by analyzing the unique properties of endoscopic images for better compression. After converting RGB pixels to YEF color space, the compressor computes the difference of consecutive pixels using differential pulse coded modulation (DPCM) and then encodes it in variable length coding using Golomb-ric code [41]. The block diagram of the proposed compressor is shown in Fig. 4. The compressor has an average compression ratio of 80.4 % and reconstructed images quality have peak signal to noise ratio (PSNR) index of more than 43.7 dB. The hardware architecture of the compressor block can be found in [24].

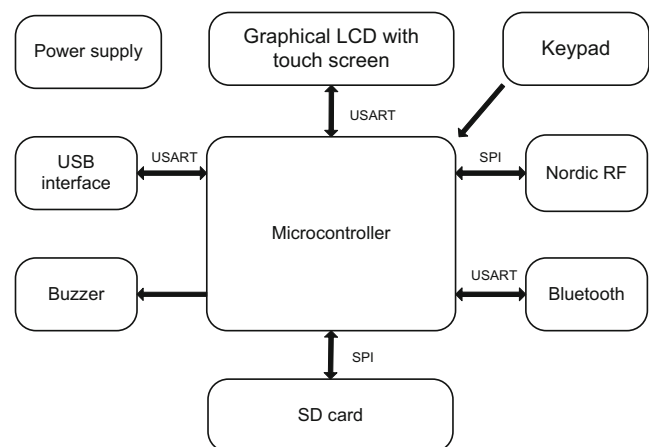
**FIFO control and memory** FIFO is used as buffering element or queuing element in a system when the rate of read operation is slower than the rate of write operation. The *Compressor* can produce bit-stream at a higher rate than the application throughput of the RF transceiver, so a FIFO is needed in the system. The *FIFO Control* block stores the compressed data bits generated by the *Compressor* block in FIFO memory and sends the data bits to RF transceiver in first-in-first-out fashion when requested by the *Capsule Control* block. The *FIFO Memory* is a dual-port memory having a word width of one bit. The memory is synthesized in the FPGA's embedded RAM blocks. The exact required size of the FIFO memory depends on the data throughput of the RF transceiver.

**Reset and clock generator** A 14 MHz built-in clock inside the FPGA is used as the primary clock source. The *Clk\_divider* block gives one clock output at 14 MHz (same as the input clock), and another at 777.76 KHz. The *Rst\_gen* block is responsible for resetting different blocks in the FPGA in proper order. The image sensor in [33] needs higher frequency clock input during initialization than the clock required for a low frame-per-second (FPS) capsule endoscopy application [42]. So, during initialization of the image sensor, the input clock frequency of the sensor is set with higher frequency clock; after the initialization, it is set to lower frequency clock. This clock switching is done by the *ClkMux* which is controlled by the *Capsule Control* block [43].

#### RF board

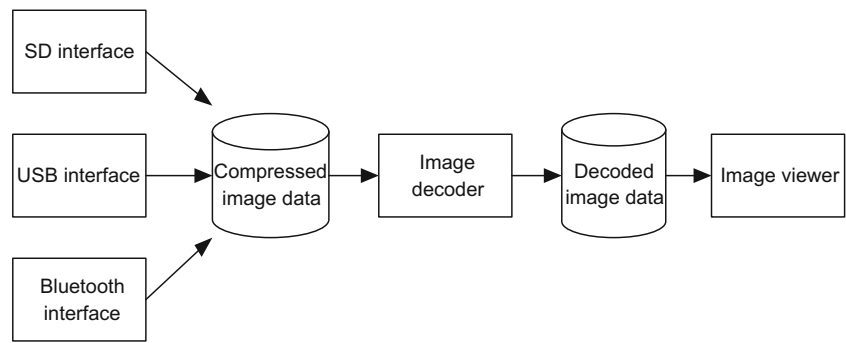
This board contains the RF transceiver with other necessary passive components. It is preferred to use a medical implantable communication service (MICS) compatible RF transceiver, which works at 402–405 MHz frequency [44]. There are two MICS compatible transceivers available from [45]—ZL70102 which has an effective data rate around 500 kbps [46] and ZL70081 whose data rate is 2.7 Mbps. The first one does not have sufficient data rate (for 2 FPS transmission) and the second one is not available for public purchase. As a result, we used an RF transceiver by Nordic [47], which works at 2.4 GHz frequency band and has a raw data-rate of 2 Mbps. It has been shown in [46, 48] that 2.4 GHz transceivers, such as Nordic, can be effectively used to get data wirelessly through animal body.

Nordic transceiver [47] contains cyclic redundancy check (CRC) based error detection and retry with auto acknowledgement feature. In auto acknowledge mode, after receiving a data packet, the receiver checks the CRC bits and detects whether there was any error during the transmission of the packet. If there was any error, then it requests the transmitter to resend the data-packet again. This process goes on until the packet is transmitted successfully. So, in *auto acknowledgement* mode, generally no data loss happens, though the number of retries can decrease the overall application throughput. The transceiver communicates with the FPGA by *SPI Interface* [34] block. The size of the transceiver is  $4 \times 4 \times 0.85$  mm and it requires a 2.4 GHz chip antenna having a dimension of  $6.5 \times 2.2 \times 1$  mm.



**Fig. 5** The hardware architecture of the data-recorder

**Fig. 6** The architecture of the workstation software



*Power board*

As power source, three silver oxide button batteries [49], each having a rated voltage of 1.55 v, current of 195 mAh and weight of 2.3 g, are used in the design. The design requires 2.8 and 1.5 v for image sensor, 1.2 v is for powering the FPGA core, and 3.3 v for RF transceiver and FPGA I/O power. These four DC voltage levels are generated using miniature low dropout regulators (LDO) [50]. A normally closed (N/C) magnetic reed switch [51] is placed between the batteries and the inputs of the power regulators in order to turn on and off power in the design from outside.

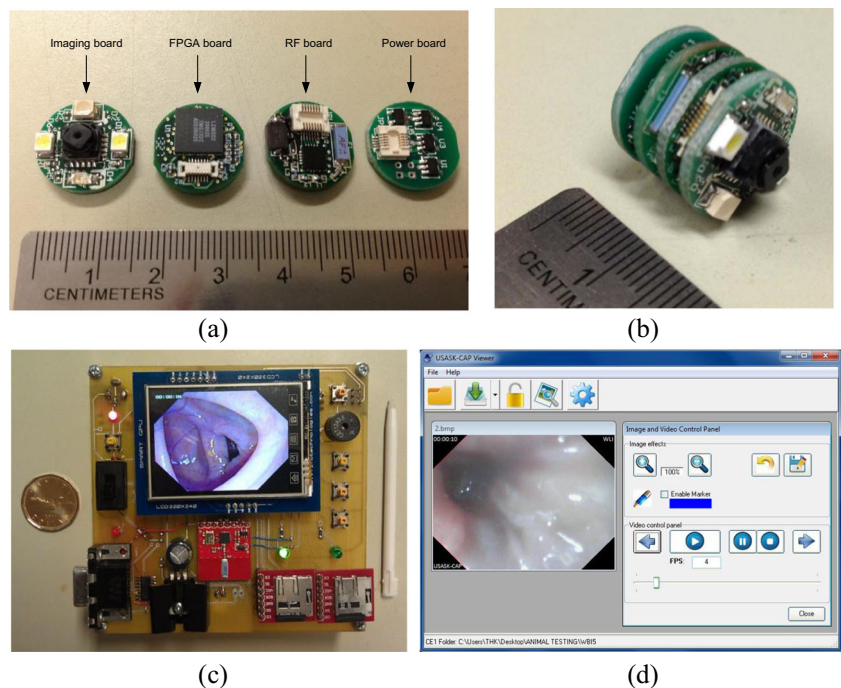
Architecture of the data recorder

The data-recorder presented in our earlier work [52] is used for storing image data. It contains a micro-controller with several peripherals connected with it as shown in Fig. 5. The data recorder is wearable and has raw data rate of

2 Mbps full-duplex wireless connectivity [47]. It also has high memory capacity of 4 GB micro secure digital (SD) card, 2.4" graphical LCD capable of displaying QVGA color images, graphs, charts in real time, with keypad and touch screen based user interface. After logging, the data can be transferred to computer using a SD card reader at a speed of up to 25 MB/s or using an USB interface. Optionally, data can also be transferred wirelessly using Bluetooth technology.

The firmware contains drivers routines for different peripherals, disk operation system (DOS), menu based graphical user interface (GUI), image decoding algorithm for real-time viewing of the compressed images, and data uploading routines. By only changing the firmware, the data-recorder can be customized for different image processing and decompression algorithm, without modifying the lower level driver and hardware layers. The size of the data-recorder prototype is 10×10×2 cm having a weight of 151 g. With one 2,000 mAh battery, the hardware can run for 11.8 h.

**Fig. 7** Photograph of the capsule endoscopy system; **a** capsule endoscopy prototype PCBs; **b** capsule PCBs stacked together; **c** the data recorder unit; **d** screenshot of the computer software



**Fig. 8** **a** Capsule prototype inserted inside pig's small intestine; **b** experimental setup showing images stored in the data recorder



#### Architecture of the computer software

The architecture of the workstation software is shown in Fig. 6. Compressed data from the data-recorder can be uploaded to the workstation by SD card, USB interface, or by Bluetooth link. The *Image decoder* decodes the compressed images and generates viewable image data. Parameters for reconstructing NBI images can be set by the user in the decoder module. The *Image viewer* contains decoded image frame navigation system and can display the image sequences as video at any given FPS.

## Results and discussion

#### The CE system prototype

The four boards for the electronic capsule, as outlined in Fig. 2, have been manufactured in circular printed circuit boards (PCB), each having a diameter of 16 mm which is suitable for animal trial. The photographs of the PCB's are shown in Fig. 7a. The PCBs are stacked together using board-to-board connectors as shown in Fig. 7b. The capsule prototype is later inserted inside a cylindrical casing. The weight of the prototype is 20 g with casing, PCBs, and three button batteries. The photograph of the developed data recorder [52]

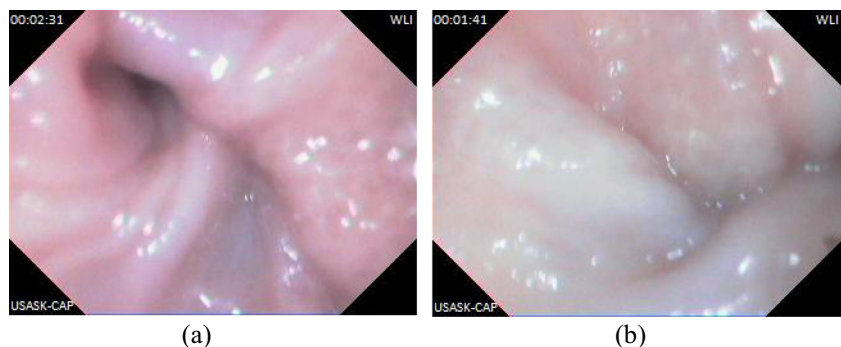
and a screenshot of the computer software are shown in Fig. 7c and d namely.

#### Animal trial

In order to evaluate the performance of the developed CE system, we have tested the system in a portion of a pig's small intestine. A pig's intestine is chosen for the experiment due to its relatively similar gastrointestinal features compared with human [53]. Before the experiment, the focal length of the lens and light intensity of the capsule are carefully adjusted. In order to test the performance of the developed CE system, the capsule prototype is inserted inside the pig's small intestine. The experimental setup is shown in Fig. 8. The trial was conducted under the ethics and protocol certificate from Animal Research Ethics Board [54].

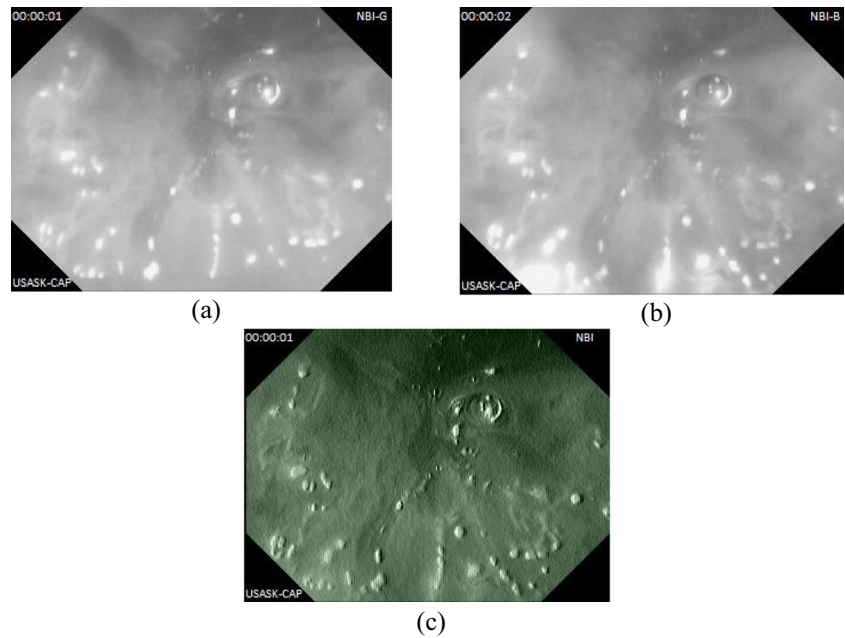
Images from the capsule are successfully transmitted to the data logger wirelessly through the pig's intestine. After the images are captured by the data logger, they are saved in SD card, decoded and shown in the LCD with time stamp. After capturing several images, the data stored in the SD card of the data logger are transferred to a computer. Using the software, the compressed data are decoded and the reconstructed images are saved in computer. In Fig. 9, two captured WLI images of QVGA size (320×240) are shown with compression ratio (CR) mentioned. In Fig. 10, captured NBI images of QVGA size are shown.

**Fig. 9** Captured QVGA size WLI images from pig's intestine: **a** CR=81.87 %; **b** CR=82.29 %





**Fig. 10** Captured NBI images from animal trial: **a** grayscale image with green light only, CR=83.95 %; **b** grayscale image with blue light only, CR=83.87 %; **c** Combined pseudo color NBI image from **a** and **b**



In the experiment, the capsule prototype is also covered by approximately 40 mm thickness of extra intestine in order to make the scenario of skin and flesh over the intestine. In this scenario, images are also successfully transmitted through the 40 mm thick tissues. During the experiment, the distance between the capsule and the data recorder is varied from 0.3 to 1 m. With varying distances, the images are transmitted successfully. The detailed features of the mucosa are visible in these images as shown in Figs. 9 and 10. The compression ratio achieved for these images in the experiment is similar to what was estimated during simulations in our previous works [40, 41].

Resource and power consumption

The digital blocks discussed earlier are modeled in VHDL and synthesized in the FPGA of the capsule prototype. The synthesis results are summarized in Table 1.

The current consumption of the entire capsule prototype in different image sizes and modes are shown in Fig. 11. For an

**Table 1** FPGA synthesis results

Resources	Usage
Number of registers	485 out of 2112 (23 %)
Number of LUT4s	957 out of 2112 (46 %)
Number of 9 Kbit block RAMs	8 out of 8 (100 %)
Number of PIO	25 out of 105 (24 %)
Max DCLK <sup>a</sup> frequency	32.5 MHz
Power consumption	12.42 mW

<sup>a</sup> Clock output from image sensor fed to the FPGA

average current consumption of 23 mA, the capsule can run for 8.5 h with three 195 mAh button batteries [49]. The total power consumption of the capsule (including LEDs, image sensor, FPGA, RF transceiver, power LDO) is approximately 100 mW.

Discussion on FPS and FIFO size

The frame rate or frame/s (FPS) of the capsule is directly proportional to the frequency of the image sensor output clock,  $f_{DCLK}$ , as expressed in (1):

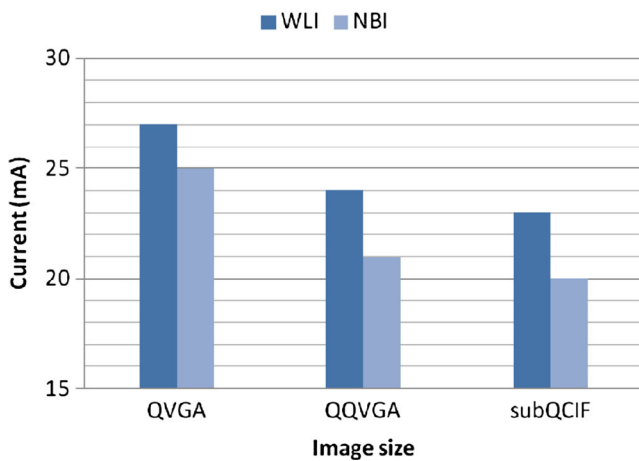
$$FPS = \frac{f_{DCLK}}{N} \tag{1}$$

where,  $N$  = Total number of DCLK cycle needed for one image frame=410,436 (for image sensor of [33], in QVGA full mode).

From Table 1, we see that the maximum DCLK frequency the FPGA can support is 32.5 MHz. From (1), the maximum supported FPS can be calculated as 79.18. However, it should be noted that the bottle-neck of the system is the application throughput of the RF transceiver,  $RF_{AT}$ , as expressed in (2).

$$W \times H \times BPP \times (1-CR\%) \times FPS \leq RF_{AT} \tag{2}$$

where,  $W$  = image width=320 (for QVGA),  $H$  = image height=240 (for QVGA),  $BPP$  = bit-per-pixel=24,  $CR$  = compression ratio=80.4 % (from [40]). For 2 FPS image transmission rate, the minimum required application throughput of the RF transceiver can be calculated from (2) as 722.53 kbps.



**Fig. 11** Current consumption of the capsule in different image transmission modes

There are several research works available in the literature about the design of low power and high data rate RF transceivers for capsule endoscopy. The work in [12, 55] proposes design of a transmitter having data rate of 20 and 15 Mbps namely. The works in [56–58] propose several designs of 2 Mbps transmitters. In [59], a design based on ultra wide band communication channel for capsule endoscopy is proposed. For instance, if the transmitter of [55] is used in our design, then QVGA images can be sent at 42 frames/second. However, these transmitters are still in the research level and not available commercially.

The *compressor* can produce bit-stream at a higher rate than the application throughput of the RF transceiver, so a FIFO is implemented for proper transmission. The required size of the FIFO,  $FIFO_{Size}$ , can be calculated from (3).

$$FIFO_{Size} = \frac{B \times f_{DCLK}}{N_r} - RF_{AT(Worst)} \quad (3)$$

where,  $B$  = data burst size = data size for one row of an image after compression =  $W \times BPP \times (1 - CR\%) = 1505$  bits,

**Table 2** Comparison with other capsule prototype works

	Design platform	Image size	FPS	Imaging mode	Real time image size and mode control	Battery life
[7]	FPGA	320×240	19	WLI	No	1.7 h <sup>b</sup>
[16]	MCU	160×160	2	WLI	–	–
[60]	MCU	640×480	0.5	WLI (grayscale)	No	–
[11]	ASIC	512×512	2	WLI and NBI	Yes (only mode)	6–8 h
[14]	MCU	–	–	WLI	No	–
[12]	ASIC	340×340	10.5	WLI	No	–
Proposed	FPGA	QVGA (320×240), QQVGA (160×120), subQCIF (128×96)	2.21 <sup>a</sup>	WLI and NBI	Yes	8.5 h

<sup>a</sup> For 800 kbps application throughput of RF transceiver

<sup>b</sup> Assuming 195 mAh battery

“–” not mentioned

$N_r$  = Total number of DCLK cycle needed for one row = 1,560 (for image sensor of [33]). At 2 FPS image transmission with  $RF_{AT} = 722.53$  kbps, the FIFO size is calculated from (3) to be 8 kB.

Depending upon the environmental condition (such as wireless interference from nearby electronic devices, distance of transmission, signal attenuation due to obstruction etc.), the transceiver’s application throughput can go much lower. Several experiments with commercial capsule in [3] revealed the fact that image transmission were not at a smooth rate of 2 FPS, rather images were sometimes sent as low as 0.1 FPS due to error in transmission.

### Comparison with other works

In Table 2, the proposed capsule prototype is compared with several other works. The works in [14, 16, 60] propose microcontroller based capsule architectures which consume significant amount of power. The battery life of these works is not reported in their papers. The work of [7] claims to have 19 frame/second referencing a research paper based RF transceiver (having data rate of 1.5 Mbps). However, the transceiver was not interfaced with their prototype for real-time experimentation and such high FPS will reduce the battery life of the system dramatically. The works in [11, 12] are developed in ASIC platform disabling programmability and flexibility of the design. The proposed capsule prototype is programmable, modular and flexible, capable of capturing both WLI and NBI images, and supports real time configuration of image resolution and imaging modes through wireless commands with a battery life of 8.5 h.

### Conclusion

In this work, a modular capsule endoscopy (CE) system is presented. The CE system is programmable in nature that

consists of an FPGA based electronic capsule, a microcontroller based data recorder and computer software. The flexible and reprogrammable nature of the system allows deployment of various image processing and compression algorithms without requiring any change in hardware. The capsule prototype is designed in four printed circuit boards (PCBs); thus any module or board can be replaced or upgraded without affecting others boards. The prototype supports both white light imaging (WLI) and narrow band imaging (NBI) imaging modes and communicates with the data recorder in full duplex mode, which enables configuring the image size and imaging modes in real time during examination. Image data can be uploaded from the data logger to a computer or Smartphone by SD card, USB interface or by wireless Bluetooth link. Computer software is developed to decompress and reconstruct images for diagnostics. The CE system is prototyped in laboratory and an ex-vivo animal testing with pig's small intestine has also been conducted to evaluate the performance.

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