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Hybrid plasmonic electro-optical modulator

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Abstract A high-performance CMOS compatible electro-optical modulator (EOM) is proposed, simulated and analyzed. The EOM is based on an asymmetric hybrid plasmonic waveguide on a silicon-on-insulator platform. Using the finite difference time domain simulation method, we obtained the transmission spectrum of the modulator. An insertion loss of 0.25 dB is achieved for a 5-μm-short modulator. The extinction ratio is optimized to be as high as 30 dB at a wavelength of 1.55 μm. Broadband operation of 600 nm is feasible since no resonator is deployed.

1 Introduction

Integration of electronic and photonic circuitries entails the design of on-chip ultra-compact electro-optical modulators. They play a significant role in optical communication systems, being responsible for the conversion of electronic signals into high bit-rate photonic data. With the ongoing progress in CMOS technology, a highly CMOS compatible compact EOM is clearly in great demand. The main challenge is to achieve high modulation efficiency, low insertion loss and small footprint. However, due to the weak nonlinear electro-optical properties of silicon and the diffraction-limited dielectric modes, silicon-based EOMs have large device footprints of millimeters order [1–4]. This implies limitations on the integration density and fabrication cost. In addition, shrinking the size of photonic modulators can lower their loading capacitance and consequently increases the modulation frequency and lowers the power consumption.

The key considerations in designing a compact EOM are: (1) having enhanced light matter interaction and (2) using materials of a high electro-optical coefficient. This makes designs based on plasmonic waveguides a good choice due to strong field confinement. As for the active material, a unity order change in the refractive index of conducting oxides has been reported [5]. However, this change in the refractive index occurs in a very thin layer of the conducting oxide. In order to make use of this refractive index change in modulation applications, the light should be concentrated in ultra-small dimensions. Incorporating conducting oxides in modulators that are based on plasmonic waveguides is a good choice due to the strong field confinement of plasmonics. Recently, conducting oxides such as indium tin oxide (ITO) have been investigated for plasmonic electro-optical modulation applications [6–9], with a 1 dB/μm extinction ratio and 1.2 dB insertion losses [6]. While showing an improvement over common silicon EOMs, those structures still have large insertion losses due to two main reasons. The first one is the propagation losses of the metal-oxide-semiconductor (MOS) mode. Secondly, there are the losses due to coupling between the MOS mode and the optical mode of the silicon waveguide.

In this work, we introduce a compact low insertion loss plasmonic modulator. The design is based on an asymmetric hybrid plasmonic waveguide (AHPW) which supports a long-range supermode. This supermode provides good tolerance to the confinement and propagation loss

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trade-off compared to MOS waveguides and other common plasmonic waveguides [10]. We have shown that the insertion loss in a 5-μm EOM can be decreased to 0.25 dB. In addition to the low-loss propagating mode, this plasmonic supermode is efficiently coupled to standard photonic silicon waveguides.

The remainder of the paper is organized as follows. Section 2 presents the indium tin oxide as the active material used for light modulation and how its properties are modified in response to applied voltage. The device structure and the modal analysis are depicted in Sect. 3. Section 4 discusses the results of the FDTD simulations, the device performance and the influence of various design parameters. Conclusions are made in Sect. 5.

2 Electro-optical active layer

Indium tin oxide is used as the optically active material in our proposed electro-absorption modulator. It has been shown that a Drude model can accurately predict the permittivity of ITO at wavelengths beyond 1 μm [11].

$$\epsilon = \epsilon_\infty - \frac{\omega_p^2}{\omega^2 + i\omega\Gamma} \tag{1}$$

where ϵ is the material permittivity, ϵ_∞ is the high frequency permittivity, ω is the angular frequency, ω_p is the plasma frequency and Γ is the relaxation frequency. The plasma frequency ω_p is given by

$$\omega_p{}^2 = \frac{Ne^2}{\epsilon_0 m^*} \tag{2}$$

where N is the free carrier concentration in the material and m^* is the effective mass of the electron.

According to (2), the ITO permittivity can be controlled by tuning the carrier concentration. The parameters we used for the thin ITO film have been measured in [6]. Plots in Fig. 1 show the change in the optical properties of the ITO due to a change in the carrier concentration from 10^{19} to 6.8×10^{20} cm^{-3}.

The modulation of the carrier concentration in the ITO is achieved by applying voltage across the structure shown in Fig. 2a. An accumulation layer is formed at the interface between the conducting oxide and silicon dioxide. Electric device simulations provide estimation to the thickness of the accumulation layer when the modulation voltage is applied. We obtained the electron concentration using both the drift-diffusion transport model and the quantum model.

The drift-diffusion transport model self-consistently solves the Poisson's equation (3) and the drift-diffusion equations (4, 5)

$$-\nabla.(\epsilon\nabla\Psi) = \rho \tag{3}$$

where ϵ is the local dielectric permittivity, Ψ is the electrostatic potential and ρ is the local space charge density.

$$J_n = q\mu_n nE + qD_n\nabla n \tag{4}$$

$$J_p = q\mu_p pE + qD_p\nabla p \tag{5}$$

where $J_{n,p}$ is the current density (A/cm^2), q is the positive electron charge, $\mu_{n,p}$ is the mobility, E is the electric field, $D_{n,p}$ is the diffusion constant and n and p are the densities of the electrons and holes, respectively. Each carrier (electron or hole) moves under the influence of two opposing processes: drift due to the applied electric field and thermal diffusion due to the gradient in the density.

The quantum treatment self-consistently solves Poisson's equation (for potential) and Schrodinger's equation (for bound state energies and carrier wave functions). The effects due to confinement of carriers associated with variations of local potential on the scale of the electron wave functions (i.e., quantum effects) was modeled in Atlas using a density gradient [12]. This model is based on the moments of the Wigner function equations of motion

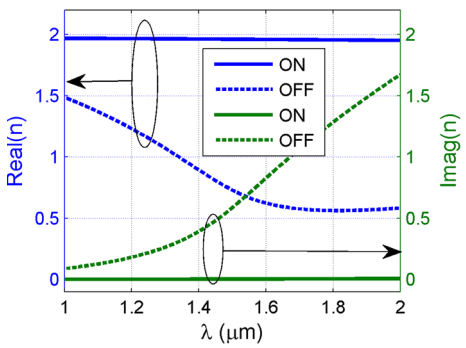

Fig. 1 The real and the imaginary part of the refractive index of the indium tin oxide in the on- and the off-states

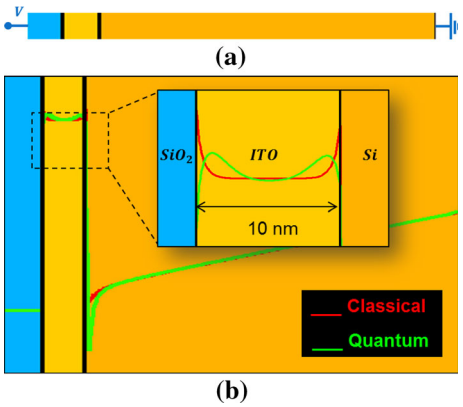

Fig. 2 **a** Structure schematic. **b** Carrier concentration modified by an applied voltage

[13]. In the density gradient model, the expression for electron current given by

$$J_n = qD_n\nabla n - qn\mu_n\nabla(\Psi - \Lambda) - \mu_n n(kT_L\nabla(\ln(n_{ie})) \quad (6)$$

Here, n_{ie} is the effective intrinsic concentration, T_L is the lattice temperature and the Λ is a quantum correction potential.

It is clear in Fig. 2b that the carrier distribution in the accumulation layer is changed by the addition of quantum mechanics models. The peak is not so high, and the electrons spread more deeply into the ITO layer. The expected permittivity change under applied voltage occurs within a ≈7-nm-thick accumulation layer according to the quantum model. This is in agreement with the results published in [5].

3 Device structure and modal analysis

Figure 3a shows the cross-section schematic of our proposed modulator. The structure consists of a silicon strip (of thickness $t_1 = 130$ nm) on a buried oxide (BOX) layer, a layer of ITO as thin as $t_{ITO} = 10$ nm and a thin metal (Gold) strip of 20 nm sandwiched between two silicon dioxide layers ($t_{upper} = t_{lower} = 20$ nm) and a silicon top layer ($t_2 = 140$ nm). The width (W) of the device is 0.5 μm.

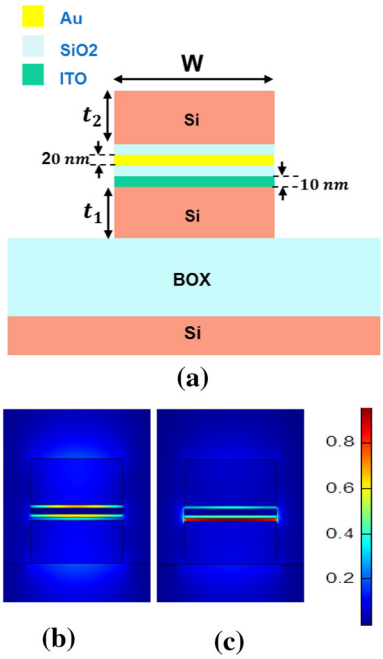

Fig. 3 **a** 2D structure, **b** on-state mode profile and **c** off-state mode profile at wavelength 1.55 μm

The proposed structure can be fabricated as follows: first, the Si waveguide is on a silicon-on-insulator (SOI) standard wafer with device layer of 340 nm over BOX. Then a thick layer of silicon is etched along the modulator section. To form a contact to the silicon, a thin layer of silicon defined by selective etching is formed at the lower part of the silicon waveguide, as shown in Fig. 4. This layer is connected to the external electrode (GND) and has a negligible effect on the mode profile. The ITO film and a silicon dioxide layer are formed the same as the standard CMOS gate oxide. Next, a thin layer of gold is deposited. The upper silicon part is formed of using plasma enhanced chemical vapor deposition at high temperature to achieve good quality silicon. This integration of photonic devices and electronic devices utilizing the already mature CMOS technology can help bring electronic and photonic functionalities together on a single chip.

3.1 On-state

For this asymmetric structure to support long-range modes, the symmetry of the field on either side of the metal should be maintained. This is achieved through careful choice of the thickness of the oxide and the ITO layer. Figure 3b shows the normalized transverse electric field component of the symmetric optical mode. The propagation loss of this mode is about 0.05 dB μm^{-1}. Another TM mode is supported by this structure. However, this mode is antisymmetric, as shown in Fig. 5. A comparison between the symmetric and the antisymmetric mode is held in Table 1. The losses of the antisymmetric mode are 40 times larger than the symmetric mode. The light is coupled to the modulator from a standard SOI waveguide, as shown in Fig. 4. Theoretically, all of the power is coupled to the low-loss symmetric mode as in Table 1.

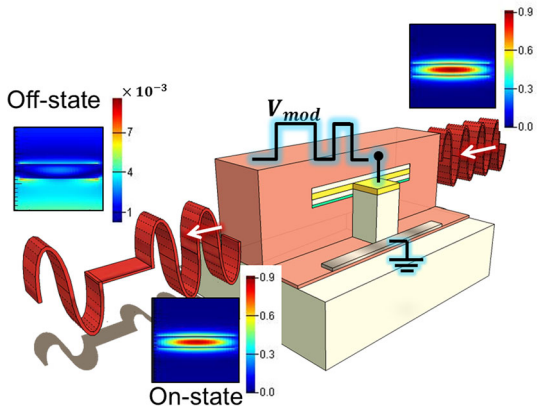

Fig. 4 3D structure of the modulator with insets showing the electric field profile (arbitrary unit) of the silicon photonic modes at the input and the output for both the on- and off-states

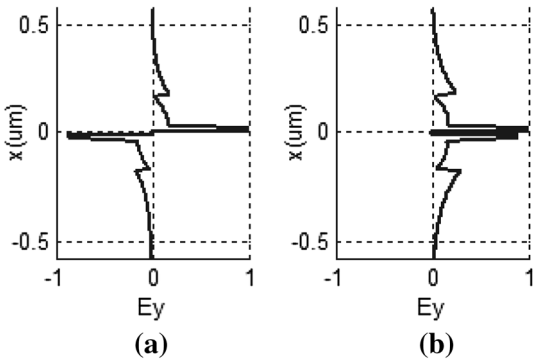

Fig. 5 **a** Antisymmetric mode and **b** symmetric mode

Table 1 Modes at $\lambda = 1.55$ μm

Mode	Antisymmetric	Symmetric
Mode index	2.6	2.05
Loss (dB/μm)	2.14	0.05
Power coupling	1e−6	100

3.2 Off-state

As the modulation voltage is applied to the thin metal, an accumulation layer is formed and the refractive index of the ITO layer is changed. As the carrier concentration is increased from 10^{19} to 6.8×10^{20} cm^{-3}, the imaginary part of the refractive index increases from about zero to 0.6 at wavelength 1.55 μm, as shown in Fig. 1. It is also worth mentioning that the real part decreases from about 2 in the on-state to 0.7 in the off-state. This increases the light matter interaction since a large part of the field becomes concentrated in the ITO layer, as shown in Fig. 3c.

It is interesting to observe the mode profiles as the wavelength increases. As shown in Fig. 6, the power of the symmetric mode becomes more concentrated in the low index ITO layer. The mode becomes less symmetric so less input power is coupled to it. When the wavelength reaches 1.55 μm, no symmetric mode exists. Both modes are asymmetric. The input power is split between those two modes almost equally. As the wavelength increases further, the symmetric mode exists again but this time with most of the field in the upper oxide layer and less power in the ITO layer. This can be explained by treating this structure as two coupled hybrid waveguides: a top HPW_u and a bottom HPW_l [10]. The symmetric mode follows the dispersion curve for HPW_l before the anti-crossing and then approaches the curve for HPW_u after the anti-crossing, as shown in Fig. 7. This means the mode loss in the off-state will increase until we reach the anti-crossing; then, it will decay because most of the power propagates through the upper hybrid waveguide.

4 Device performance

4.1 Insertion loss

We carried out finite difference time domain simulations using Lumerical Solutions to compare insertion loss of a MOS modulator of length 5 μm [6] and our proposed modulator of the same length. The results are shown in Fig. 8a. The total insertion loss is 0.3 dB. Our modal analysis already expected propagation loss of 0.05 dB/μm. So the coupling loss is estimated to be as low as 0.025 dB/coupler. This low coupling loss can be well understood from the calculation of the mode overlap integral between the TM silicon photonic mode and the symmetric mode of the AHWG section of the modulator.

$$\mathrm{MOI} = \frac{|\int H_i(x) H_m^*(x) \mathrm{d}x|^2}{\int |H_i(x)|^2 \mathrm{d}x \cdot \int |H_m(x)|^2 \mathrm{d}x} \tag{7}$$

4.2 Extinction ratio

A key performance parameter of the modulator is the ratio of the transmitted power in the on-state to that in the off-state, known as the extinction ratio (ER). In our proposed design, 2D and 3D FDTD simulations show that ER reaches 30 dB in a 5-μm modulator at the operating wavelength of 1.55 μm as in Fig. 9. Instead of focusing on the ER or IL separately, we consider a figure of merit defined as the ER/IL ratio to compare the device performance, where maximization of this ratio is the main goal. This is shown in Fig. 8b where the proposed AHPW modulator outperforms the MOS configuration across a large region of the spectrum.

The, respectively, high ER of this design suggests the feasibility of more compact EOMs with adequate modulation depth. Fig. 10 shows the transmission in the off-state as the modulator length increases from 1 to 5 μm.

It is worth noting that the maximum loss is achieved at $\lambda = 1.55$ μm which is the anti-crossing point shown in Fig. 7. Fortunately, the position of the anti-crossing point can be engineered by changing the effective index of the lower hybrid waveguide. This is feasible by changing the off value of the modulating voltage so that the number of free carriers in the accumulation layer changes accordingly. The simulation results for modulators of lengths 5 and 2 μm are shown in Fig. 11. The peak of the ER can be shifted by varying the carrier concentration. So the applied

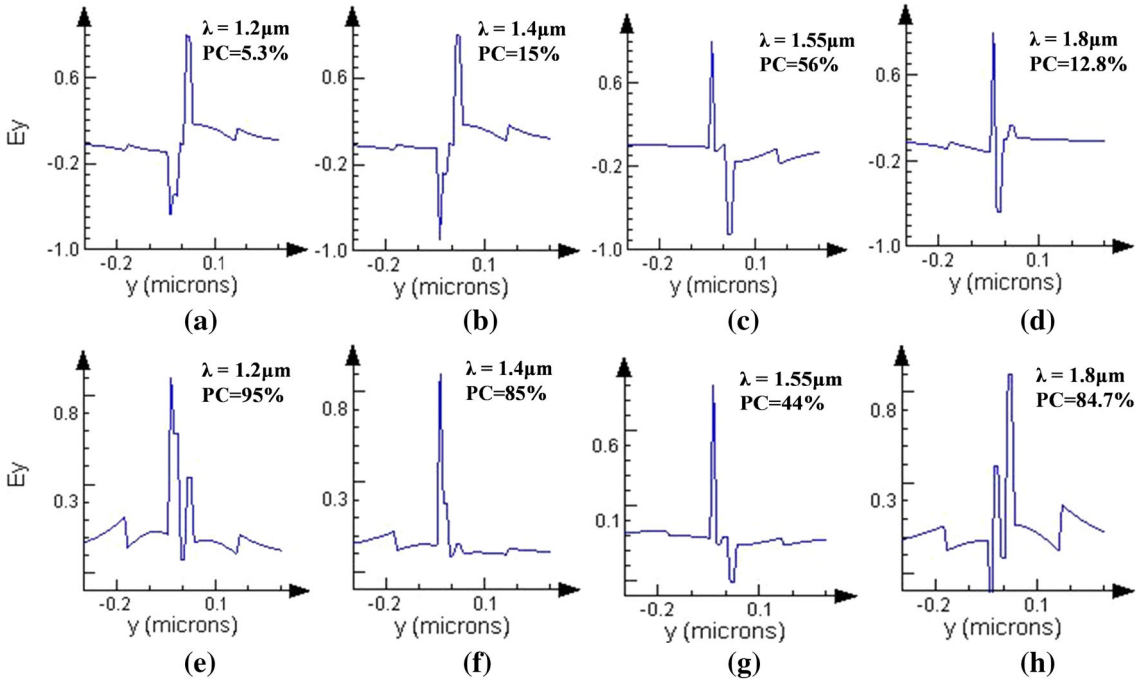

Fig. 6 Mode profiles of antisymmetric (**a**–**d**) and symmetric (**e**–**h**) modes in the off- state at different wavelengths

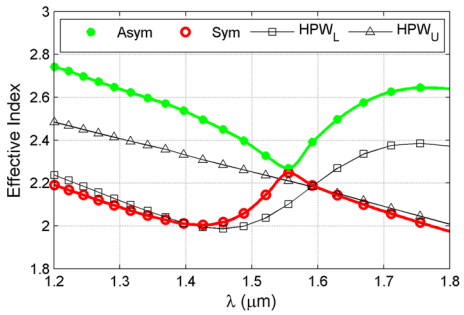

Fig. 7 Dispersion curves of the symmetric, antisymmetric, the *lower* and *upper* hybrid plasmonic waveguides

voltage can be tuned for optimum performance in the operation region.

4.3 Oxide thickness

The performance of the modulator has been simulated for different thicknesses of the silicon dioxide layer. Fig. 12 shows that as the thickness decreases, the modulator has less insertion loss and larger extinction ratio. The figure of merit can approach up to 120 for a 10-nm oxide layer. The practical fabrication of this thickness is not a great issue given the advances in the CMOS technology which makes it capable of the fabrication of ultra-thin gate oxide for the MOS transistor.

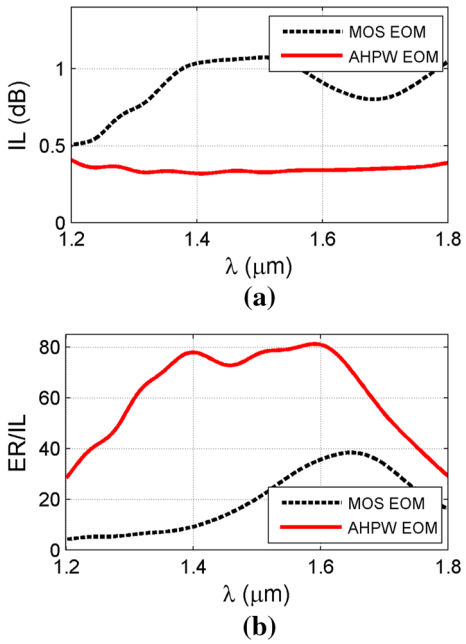

Fig. 8 Comparison between the performance parameters of the MOS and AHPW electro-optical modulators; **a** insertion loss and **b** ER/IL ratio

4.4 Silicon thickness

Another design parameter is the total thickness of the silicon waveguide. It is shown in Fig. 13 that increasing the thickness enhances the performance up to a certain value.

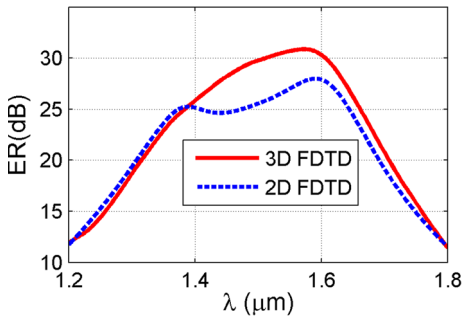

Fig. 9 2D and 3D FDTD simulations of extinction ratio of a 5-μm modulator

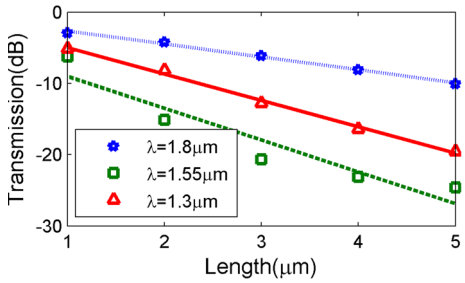

Fig. 10 Transmission of the modulator in the off-state across the modulator length

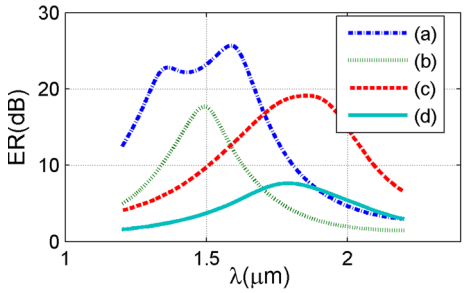

Fig. 11 Extinction ratios at two different free carrier concentrations for modulators of lengths 5 and 2 μm. *a* $L = 5\,\mu m$, $N = 6.8e20\ cm^{-3}$, *b* $L = 2\,\mu m$, $N = 6.8e20\,cm^{-3}$, *c* $L = 5\,\mu m$, $N = 4.4e20\,cm^{-3}$ and *d* $L = 2\,\mu m$, $N = 4.4e20\,cm^{-3}$

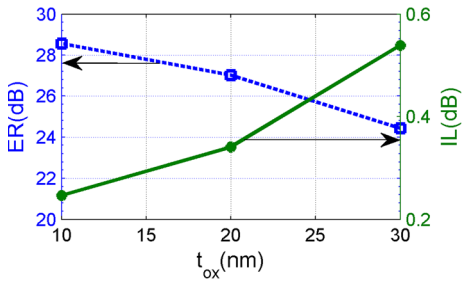

Fig. 12 Electro-optical modulator performance across the silicon dioxide thickness; extinction ratio and Insertion loss

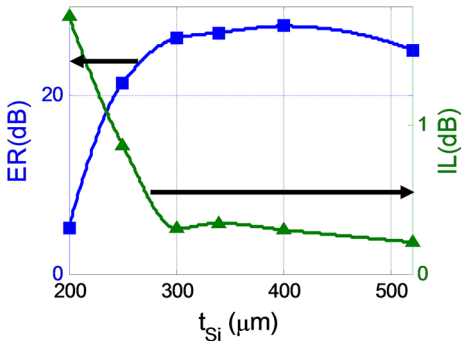

Fig. 13 Electro-optical modulator performance across the silicon thickness

Further increase in the thickness does not yield remarkable improvements. In addition, for silicon thicknesses above 340 nm the single-mode operation can hardly be sustained.

5 Conclusions

We designed and numerically verified an ultra-compact low insertion loss modulator based on a CMOS compatible waveguide. Utilizing the asymmetric hybrid waveguide, one can achieve an extinction ratio up to 5 dB/μm while maintaining the on-state loss of 0.05 dB/μm. Based on this configuration, a 2-μm modulator can achieve about 15 dB signal modulation. The small mode size and length of the modulator offers it the advantage of high switching speed due to its small capacitance. Broadband operation of the modulator is possible due to the fact that no resonance effect is employed. The level of the applied modulating voltage can be optimized for different spectral regions.

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References

1. M.R. Watts, W.A. Zortman, D.C. Trotter, R.W. Young, A.L. Lentine, Vertical junction silicon microdisk modulators and switches. Opt. Exp. **19**(22), 21 989–22 003 (2011)
2. Q. Xu, B. Schmidt, S. Pradhan, M. Lipson, Micrometre-scale silicon electro-optic modulator. Nature **435**(7040), 325–327 (2005)
3. Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, M. Lipson, 12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators. Opt. Exp. **15**(2), 430–436 (2007)
4. P. Dong, L. Chen, Y.-K. Chen, High-speed low-voltage single-drive push-pull silicon Mach-Zehnder modulators. Opt. Exp. **20**(6), 6163–6169 (2012)

5. E. Feigenbaum, K. Diest, H.A. Atwater, Unity-order index change in transparent conducting oxides at visible frequencies. Nano Lett. **10**(6), 2111–2116 (2010)
6. V.J. Sorger, N.D. Lanzillotti-Kimura, R.-M. Ma, X. Zhang, Ultra-compact silicon nanophotonic modulator with broadband response. Nanophotonics **1**(1), 17–22 (2012)
7. C. Ye, S. Khan, Z.R. Li, E. Simsek, V.J. Sorger, λ-size ITO and graphene-based electro-optic modulators on SOI. IEEE J. Sel. Top. Quant. Electron. **20**(4), 40–49 (2014)
8. J.T. Kim, Silicon optical modulators based on tunable plasmonic directional couplers. IEEE J. Sel. Top. Quant. Electron. **21**(4), 1–8 (2015)
9. H. Zhao, Y. Wang, A. Capretti, L. Dal Negro, J. Klamkin, Broadband electroabsorption modulators design based on epsilon-near-zero indium tin oxide. IEEE J. Sel. Top. Quant. Electron. **21**(4), 1–7 (2015)
10. W. Ma, A.S. Helmy, Asymmetric long-range hybrid-plasmonic modes in asymmetric nanometer-scale structures. JOSA B **31**(7), 1723–1729 (2014)
11. F. Michelotti, L. Dominici, E. Descrovi, N. Danz, F. Menchini, Thickness dependence of surface plasmon polariton dispersion in transparent conducting oxide films at 1.55 μm. Opt. Lett. **34**(6), 839–841 (2009)
12. Silvaco Inc., ATLAS users manual—Device simulator software. www.silvaco.com (2013)
13. J.-R. Zhou, D.K. Ferry, Simulation of ultra-small gaas mesfet using quantum moment equations. IEEE Trans. Electron. Devices **39**(3), 473–478 (1992)